Fremont Micro Devices

FT60E21

Data Sheet

Key Features

8−bit EEPROM based RISC MCU

Program: 1k x 14; RAM: 64 x 8; Data: 128 x 8

6 / 8 Pins

3 Timers, 4 Individual PWMs − 1 with Deadband

Low Standby, WDT and Operation Current

POR, LVR, Single Input Comparator

Selectable Source and Sink Current

High ESD, High EFT

Low V_{DD} Operation

Tunable HIRC

Rev1.01

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8−bit CPU (EEPROM)

- 37 RISC instructions: 4T
- 16 MHz / 4T ($V_{DD} \geq 2.5$)
- Up to 8 pins

Memory

- PROGRAM: 1k x 14 (R/W Protect)
- DATA: 128 x 8
- RAM: 64 x 8
- 8−level Hardware Stack
- Custom Key for hex encryption

Operation Conditions (5V, 25°C)

- V_{DD} ($V_{POR} \leq 1.9V$) V_{POR} − 5.5 V
  (Self-regulated by POR, ≤1.7V for above 0°C)
- Operation Temperature Grade $^{-}40$ – $^{+}85$ °C
- Low Standby 0.2 μA
- WDT 2.5 μA
- Normal Mode (16 MHz) 136 μA/mips

High Reliability

- 100k cycles, >20 years / 85°C storage (typical)
- ESD > 4 kV, EFT > 5.5 kV

PWM (Total 4)

- Support RUN in SLEEP
- Total 4 channels (same Period)
  - ✓ Independent: Duty Cycle, Polarity
- 1 channel (up to 2 I/O):
  - ✓ Complementary + Deadband
- Auto Fault-Breaking (I/O, LVD)
- Secondary XOR, XNOR functions
- One-Pulse mode
- Buzzer mode

Timers

- WDT (16−bit): 7−bit postscaler
- Timer0 (8−bit): 8−bit prescaler
- Timer2 (16−bit): 4−bit pre and post-scaler
- Support RUN in SLEEP
- LIRC, HIRC, 1 or 4x {Instr. Clock}

I/O PORTS (Up to 6 I/O)

- Resistive Pull-Up
- 2 I/O I_{SOURCE}: 3, 6 or 24 mA (5V, 25°C)
- 2 I/O I_{SINK}: 53 or 67 mA (5V, 25°C)
- 6 I/O: Interrupt / Wake-Up

Power Management

- SLEEP
- LVR: 2.0, 2.2, 2.5, 2.8, 3.1, 3.6, 4.1 (V)
- LVD: 1.2, 1.8, 2, 2.4, 2.7, 3, 3.3, 3.6, 4 (V)
  (LVD also functions as a single input comparator with selectable polarity.)

System Clock (SysClk)

- HIRC High Speed Internal Oscillator
  - ✓ 16MHz <±1.0% typical (2.5 − 5.5V, 25°C)
  - ✓ Tunable
  - ✓ 1, 2, 4, 8, 16, 32, 64 divider
- LIRC Low Power Internal Oscillator
  - ✓ 32 kHz or 256 kHz
- External Clock (I/O input)

Integrated Development Environment (IDE)

- On-Chip Debug (OCD), ISP
- 1 hardware breakpoints
- System-Reset, Stop, Single Step, Run

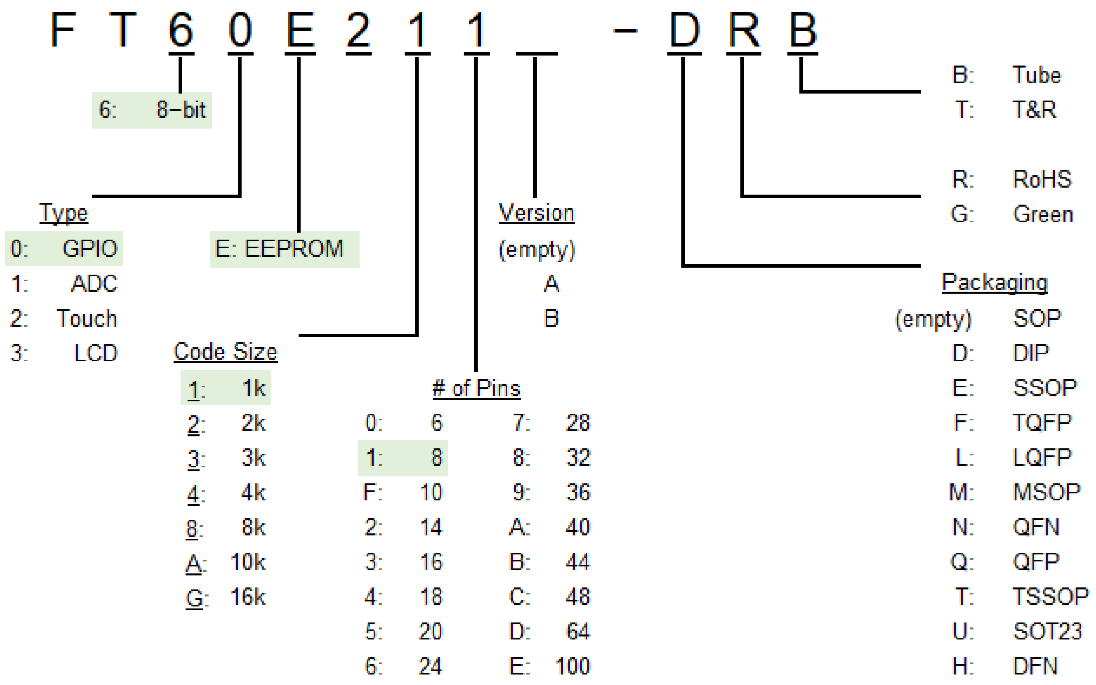
Packages

- SOT23-6 SOP8

PARTS INFORMATION AND SELECTIONS

Part #	# of I/O	Package
FT60E210−Uab	4	SOP23-6
FT60E211−ab	6	SOP8

Where a = R; RoHS b = B; Tube
= G; Green = T; T&R



MCU Part # Selections

Revision History

Date	Revision	Description
2022-08-24	1.00	Preliminary version
2022-09-21	1.01	Correct some mistakes

Table of Contents

1. BLOCK DIAGRAM AND PINOUTS

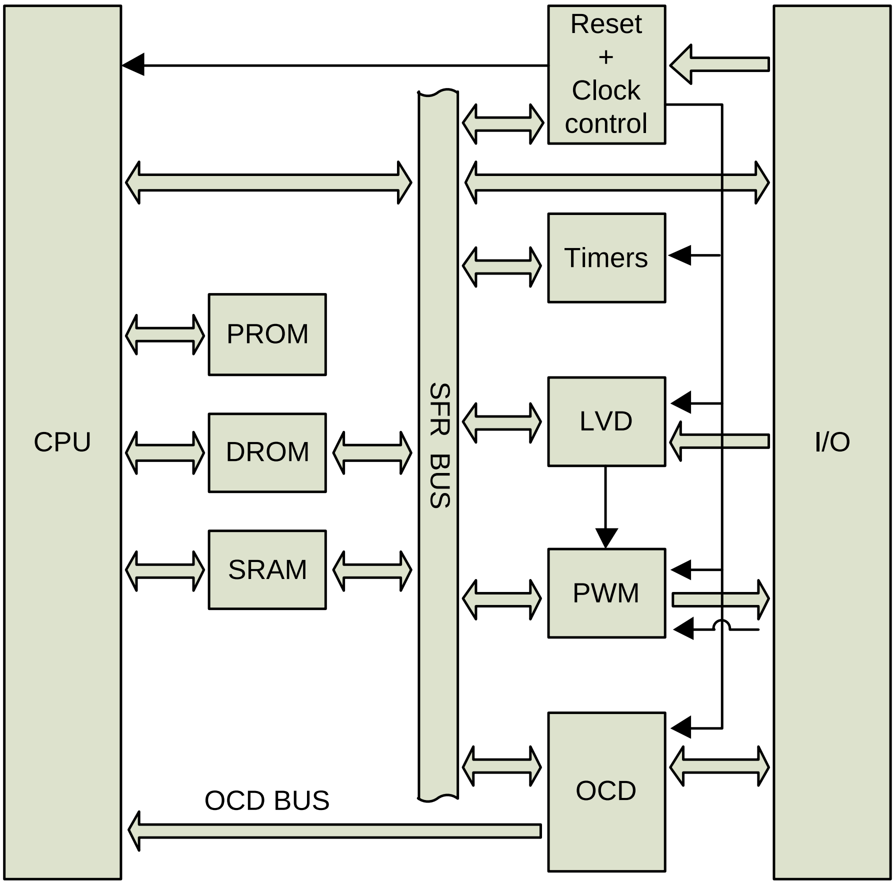


Figure 1-1 System block diagram

The list of standard abbreviation is as follows:

Abbreviation	Description
CPU	Central Processing Unit
SFR	Special Function Registers
SRAM	Static Random Access Memory
DROM	Data EEPROM
PROM	Program EEPROM
Timers	WDT, Timer0, Timer1, Timer2
PWM	Pulse Width Modulator
LVD	Low Voltage Detect / comparator
OCD	On Chip Debug
I/O	Input / Output

1. 1 Pinouts

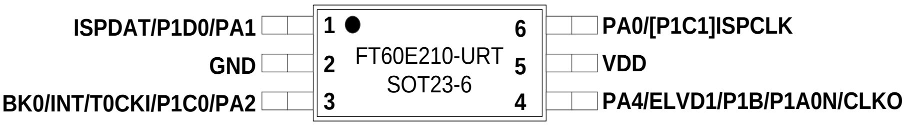


Figure 1-2 SOT23-6

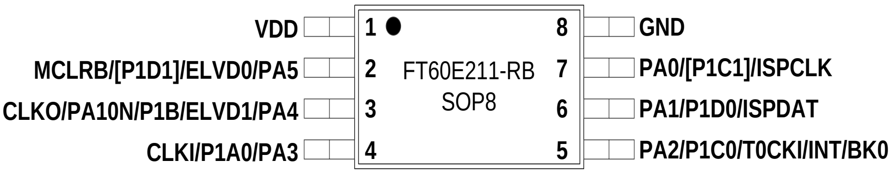


Figure 1-3 SOP8

1.2 Pin Description by Functions

Function	Description	Pin Name	GPIO equiv.	6 pins	8 pins
Power		VDD		5	1
		GND		2	8
GPIO	Pull-Up, Digital Input, Digital Output	PA5			2
		PA4		4	3
		PA3			4
		PA2		3	5
		PA1		1	6
		PA0		6	7
LVD	Input	ELVD0	PA5		2
		ELVD1	PA4	4	3
Clock	Output	CLKO	PA4	4	3
	EC Input	CLKI	PA3		4
	Timer0 Clock	T0CKI	PA2	3	5
ISP Debugger	ISP-Data	ISPDAT	PA1	1	6
	ISP-CLK	ISPCLK	PA0	6	7
Reset	Pull-up	/MCLRB	PA5		2
PA2-INT Edge		PA2-INT	PA2	3	5
PORTA Logic-Changes Interrupt	Input	PA5			2
		PA4		4	3
		PA3			4
		PA2		3	5
		PA1		1	6
		PA0		6	7
PWM1 (Deadband)		P1A0	PA3		4
	/PWM1	P1A0N	PA4	4	3
PWM2		P1B0	PA4	4	3
PWM3		P1C0	PA2	3	5
		[P1C1]	PA0	6	7
PWM4		P1D0	PA1	1	6
		[P1D1]	PA5		2
PWM Fault-Break Input		BK0	PA2	3	5

Table 1-1 Pin description by functions

2. I/O PORTS

Up to 6 I/O pins are available depending on the types of package, PORTA (6). **Table 2-1** lists the functions of all I/O pins.

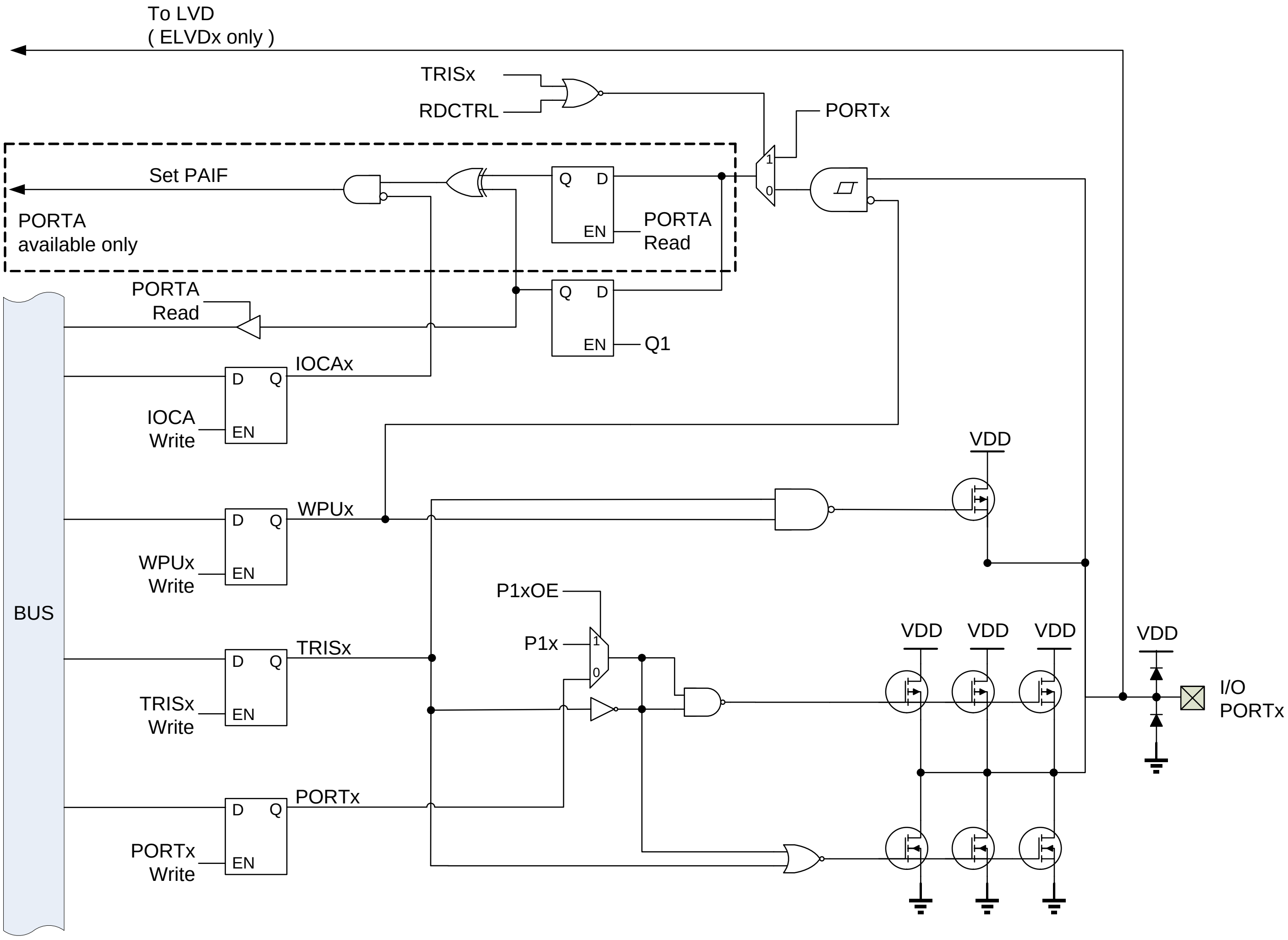


Figure 2-1 PORT block diagram

All I/O pins have the following functions (**Table 2-3**, **Table 2-4**):

- Digital Output
- Digital Input
- Weak Pull-Up

In addition some I/O’s have special functions assigned.

1. Debugger pins (ISP-Data, ISP-CLK) are hardwired and require no set-up.
2. Some special functions are configured at the IDE and loaded during BOOT (**Table 2-2**).

- External Clock IN (CLKI)
- Internal Clock OUT
- System-Reset (/MCLRB)

3. All other functions are Instruction Level assigned to the various I/O's. They are divided into 3 categories:

   a. Digital Output

      - PWM

   b. Digital Input

      - PWM Fault Break
      - Timer0 Clock Input
      - External Edge Interrupt
      - GPIO Interrupt-on-Change

   c. Analog Input

      - LVD / BOR

Name	ISP Debugger	CLK	Interrupt	LVD	PWM	Digitial I/O Pull-Up	Source Current (mA)	Sink Current (mA)
PA0	CLK		√		PWM 3	√	18	53
PA1	DATA		√		PWM 4	√	18	53
PA2		T0CKI	√+ INT		PWM 3	√	18	53
PA3		CLKI	√		PWM 1	√	18	53
PA4		Output	√	ELVD1	PWM 2 + PWM 1N	√	3, 6, 24	53, 67
PA5			√ + /MCLRB	ELVD0	PWM4	√	3, 6, 24	53, 67
Note					BK0 = PA2		V_{DD}=5, V_{DS}=0.5	

Table 2-1 I/O PORT Functions

Note: PA4−5 each has 3 configurable source current levels (see "PSRCAx" in **Table 2-4**), and 2 configurable sink current levels (see "PSINKAx" in **Table 2-4**).

2.1 Summary of I/O PORT Related Registers

Name	Function	Default
RDCTRL	READ register when TRISx = 0 (Output enabled) • Input latch • Output latch	Output
MCLRE	Reset by External I/O	disabled
FOSC	• EC external oscillator at PA3 (CLKI) (Note: set TRISA[3] = 1) • INTOSCIO mode: PA3 as I/O	INTOSCIO

Table 2-2 BOOT Level I/O related configurations

Name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset Value
TRISA	0x85	–		TRISA[5:0], PORTA Direction						−−11 1111
PORTA	0x05	–		PORTA Output Register						−−xx xxxx
WPUA	0x95	–		PORTA Weak Pull-Up						−−11 1111
PSRCA	0x88	–				PORTA Source Current Setting				−−−− 1111
PSINKA	0x97	–						PORTA sink Current		−−−− −−11
IOCA	0x96	–		IOCA[5:0]: PORTA Interrupt-on-Change						−−00 0000
OPTION	0x81	/PAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111

Table 2-3 Addresses and Reset Values of I/O related registers

Name	Status		Register	Addr.	Reset
TRISA	PORTA	PORT Digital Output (Direction) 1 = Disables 0 = Enables (Disables Pull-Up)	TRISA[5:0]	0x85	RW−11 1111
/PAPU	1 = Disables all PORTA Pull-Up 0 = WPUA settings apply		OPTION[7]	0x81	RW−1
WPUA	PORTA	Weak Pull-Up 1 = Enables 0 = Disables	WPUA[5:0]	0x95	RW−11 1111
PORTA	PORTA	Data Out Register	PORTA[5:0]	0x05	RW−xx xxxx
PSINKA	PA5	Sink Current (mA) 1 = 67 0 = 53	PSINKA[1]	0x97	RW−1
	PA4		PSINKA[0]		RW−1
PSRCA	PA5	Source Current (mA) (00) = 3 (01) = 6 / (10) = 6 (11) = 24	PSRCA[3:2]	0x88	RW−11
	PA4		PSRCA[1:0]		RW−11

Table 2-4 Instruction Level I/O related registers

2.2 Configuring the I/O

For each PORT, configures the following three modules according to their functions (**Table 2-5**).

- Weak Pull-Up
- Digital Input
- Digital Output

Functions	Digital Input	Pull-Up / Pull-Down	Digital Output	Settings
ISP-DATA	On	Off	On	(hardwired, instructions ignored)
ISP-CLK	On	Off	Off	(hardwired, instructions ignored)
/MCLRB	On	Pull-Up	Off	(BOOT set, instructions ignored)
CLOCK OUT	(don't care)	Off	On	(BOOT set, instructions ignored)
CLKI (EC)	On	(optional)	Off	(BOOT set, instructions ignored)
LVD	Off [3]	Off	Off	TRISx = 1;
Timer0 Clk	On	(optional)	Off	TRISx = 1
Interrupt-on-Change	On	(optional)	Off	TRISx = 1
PA2−INT	On	(optional)	Off	TRISx = 1
BK0	On	(optional)	Off	TRISx = 1
Digital Input	On	(optional)	Off	TRISx = 1
PWM	On	Off	On	TRISx = 0
Digital Output	On	Off	On	TRISx = 0

Table 2-5 Instruction Level I/O Configuration Flags and Registers

Notes:

1. TRISx = 0: “Digital Output” enabled, “Pull-Up” disabled (WPUx ignored).
2. TRISx = 1: “Digital Output” disabled.
3. “Digital Input”, “Pull-Up” and “Pull-Down” are automatic disabled when the PORT is an LVD input. PA4 and PA5 cannot be assigned to the LVD part time only, as cannot shut down “Digital Input” for the rest of time when LVD is not assigned to PA4 or PA5.
4. “/PAPU = 1” disables “Weak Pull-Up” for all PAx.
5. /MCLR enabled: PA5’s Weak Pull-Up enabled (WPUA[5] ignored); PORTA[5] read “0”.
6. Writing the PORTx Data Out registers will output the logic level to the corresponding I/O. Write operations are ‘Read-Modify-Write’ operations, meaning PORTx latch (output or input) are read first, then modified and written back, as up to 6 I/O share the same register.
7. Digital Output and Digital Input can be inclusive. Some applications need both enabled simultaneously.
8. The IDE can globally choose which PORT latch (output or input) to READ when TRISx = 0.
9. In Full-Reset or System-Reset PORTx will not reset, but TRISx will reset to “1”, disabling output.

See **Section 9** “Interrupts” for setting up PA2-INT and PORTA Interrupt-on-Change.

3. POWER-ON-RESET (POR)

During Power-On, V_{DD} increases from below the Power-On-Reset Voltage (V_{POR}) to above it. V_{DD} may not have completely discharged to 0V when the CPU is Power-On again.

1. The CPU is in a Full-Reset state when V_{DD} is below V_{POR}.
   a. All Calibrated Data registers are not reset. Special Function Registers (SFR) are in Reset, except TMR0, FOSCCAL, PORTx, Z, HC, C, FSR, INDF, SRAM (see **Section 14** Special Function Registers). Registers not reset, such as SRAM, will hold their values until V_{DD} drops below 0.6V (typical). Data of those resisters with V_{DD} below 0.6V are undetermined.
   b. Program Counter = 0x00, Instruction Register = “NOP”, Stack Pointer = “TOS” (Top of Stack).
2. BOOT commences when V_{DD} raises above V_{POR}.
3. Instruction execution begins with Program Counter = 0x00 after BOOT completion.

V_{POR} is ~1.6V at 25°C (typical), increasing to ~1.9V at -40°C. For $V_{DD} \geq V_{POR}$, the CPU can function at a reduced speed of 8 MHz / 4T. POR alone can safeguard against a low V_{DD} failure, giving a self-regulated wider V_{DD} operating range with temperature. This is important for battery-powered system as the CPU can function down even to ~1.6V at typical battery operating environments, greatly extending useful battery life.

Notes:

1. V_{POR} is not configurable.
2. The POR circuit is always on and will perform a Power-On-Reset any time V_{DD} voltage is below V_{POR}, not just during Power-On.

3.1 BOOT Sequence

Name	Functions	default
PWRTEB	Additional ~64ms delay after BOOT load	disabled

Table 3-1 BOOT configuration

The value of BOOT configuration is set at the IDE, not by instructions. during BOOT:

1. CPU Idles for ~4ms.
2. The BOOT Level registers are loaded from the non-volatile memory. It takes ~24us. These registers are pre-set at the IDE and not affected by instructions.
3. If Power-On-Timer (PWRT) is enabled, the CPU will idle for ~64ms.

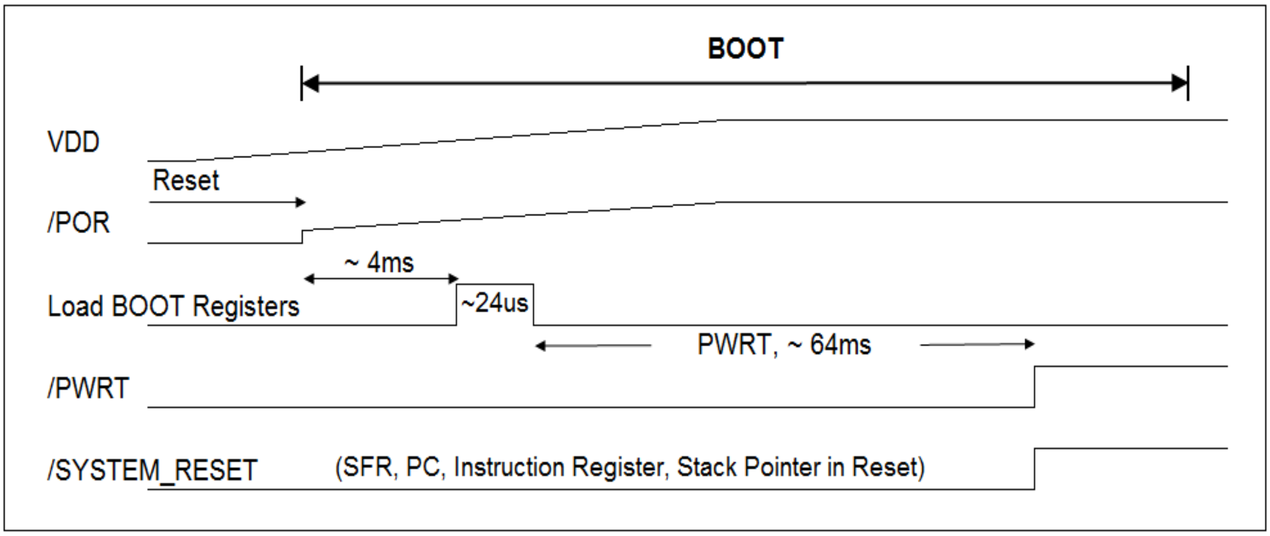


Figure 3-1 Power-On Sequence with PWRT enabled

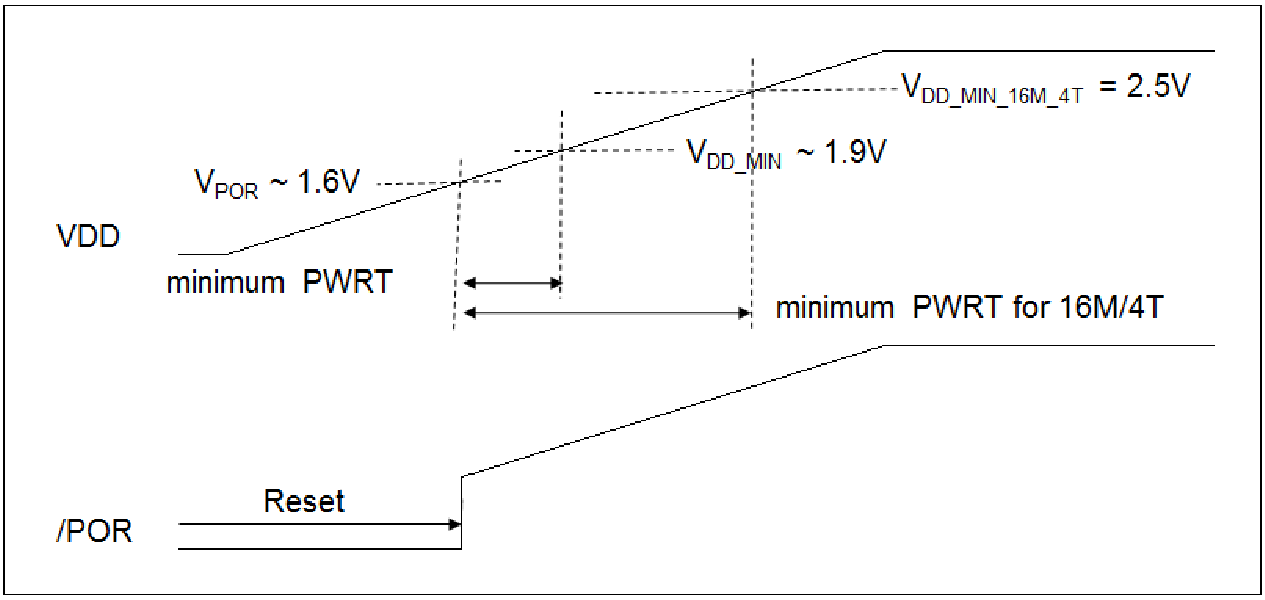


Figure 3-2 Minimum required PWRT during Power-On

V_{DD} must be higher than 2.5V by the end of BOOT if the CPU is to run at 16MHz / 4T. The total BOOT time can increase from ~4ms to ~68ms by enabling the PWRT, giving more time for the power system to stabilize.

Enables LVR with V_{BOR} ≥ 2.5V for operation at 16MHz / 4T. LVR can be set to instruction controlled to monitor V_{DD} sporadically, instead of always on (see “LVREN”, “SLVREN”) to reduce power consumption.

Notes:

1. V_{DD} should not rise too slowly. C_{VDD} ≥ 22 μF is discouraged.
2. V_{DD} capacitor of 1 to 10μF is preferred. C_{VDD} < 1μF capacitor may be too small for EFT considerations.
3. If a delay in startup is acceptable, enables PWRT to improve CPU stability.

4. SYSTEM-RESET

System-Reset differs from POR in that it is not a Full-Reset. Depending on the trigger type and configurations, CPU may or may not BOOT. BOOT will wait ~4ms, reload the BOOT registers, and further delay system start by ~64ms if PWRT is enabled. In a System-Reset

- Registers reset in POR are reset, except BOOT registers.
- Program Counter = 0x00, Instruction Register = “NOP”, Stack Pointer = “TOS” (Top of Stack).

The following 4 events besides debugger OCD can be configured to trigger a System-Reset:

1. Brown-Out (LVR / BOR) – always BOOT.
2. Illegal Instructions (always on).
3. Watch-Dog Timer (WDT).
4. External I/O (/MCLRB) – BOOT if “MBTEB” is set.

Note: If a longer system restart time is acceptable, enable BOOT will improve system stability.

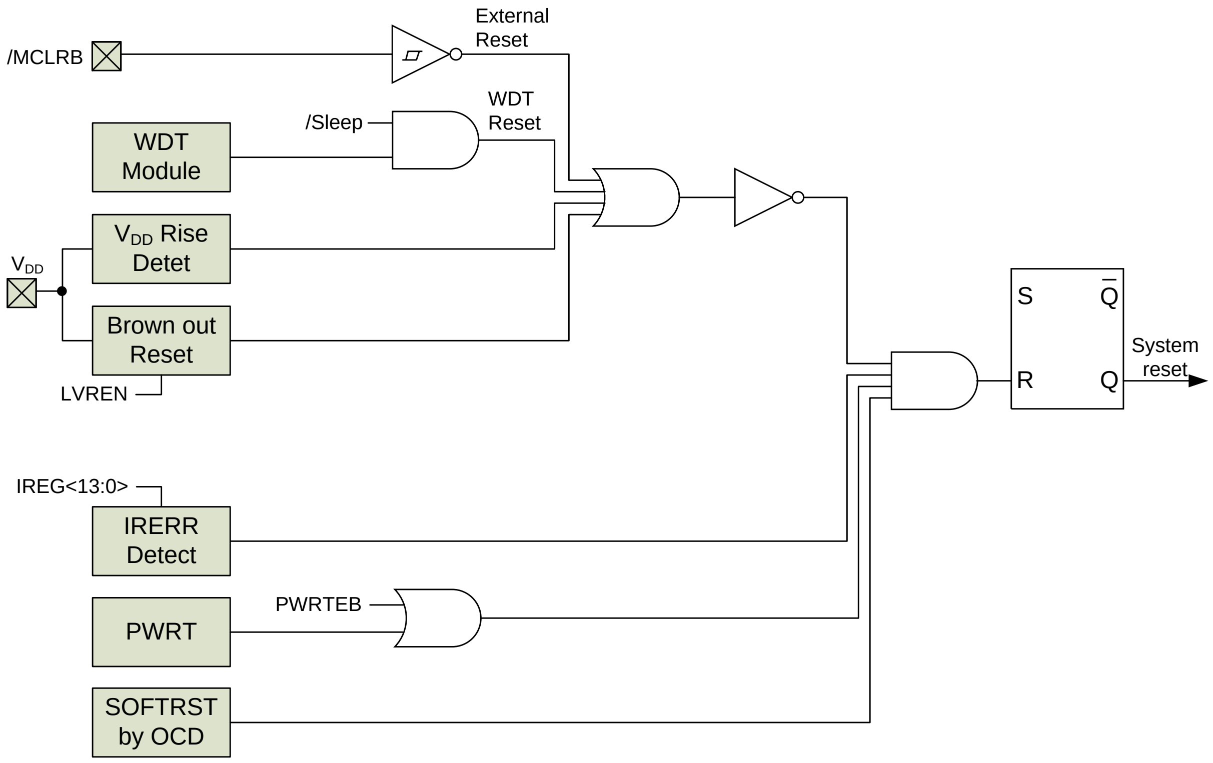


Figure 4-1 Reset circuit block diagram

4.1 Summary of SYSTEM-RESET Related Registers

Most settings for System-Reset are configured at the IDE, and cannot be changed by instructions.

Name	Functions	default
LVRS	7 V_{BOR} Voltage levels (V): 2.0 / 2.2 / 2.5 / 2.8 / 3.1 / 3.6 / 4.1	2.5
LVREN	LVR - Enabled - Disabled - Instruction controlled (SLVREN)	disabled
WDTE	WDT - Enabled (overrides instructions disable) - Instruction controls (SWDTEN)	SWDTEN control
MCLRE	Reset by External I/O	disabled
MBTEB	BOOT on MCLRE Reset	disabled

Table 4-1 BOOT Level RESET related configurations

4.2 Brown-Out Reset (LVR / BOR)

Brown-Out occurs when V_{DD} falls below a pre-configured Brown-Out Voltage (V_{BOR}) for a time longer than T_{BOR}. T_{BOR} takes 3 to 4 LIRC clock cycles (~94 – 125µs, LIRC will turn on automatically if not already). CPU System-Reset as long as $V_{DD} \le V_{BOR}$. Once $V_{DD} > V_{BOR}$ CPU will BOOT.

While V_{POR} is fixed, V_{BOR} can be set to 2.0, 2.2, 2.5, 2.8, 3.1, 3.6, 4.1V (see "LVRS" in **Table 4-1**).

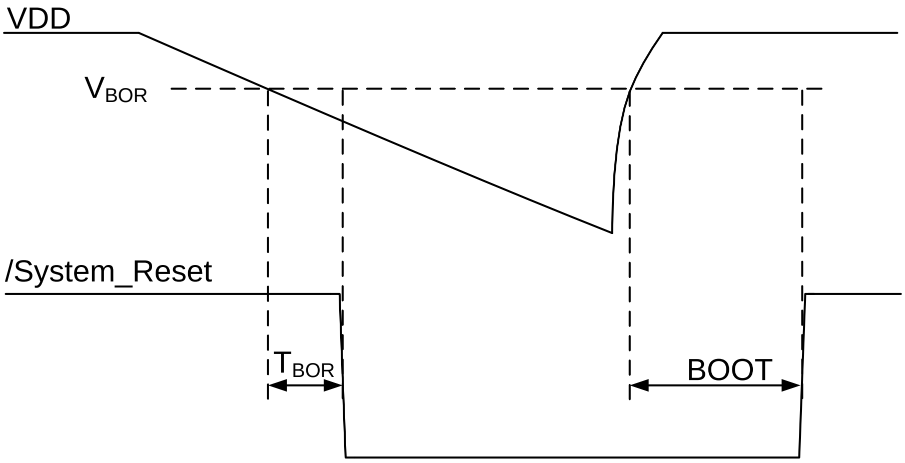


Figure 4-2 LVR BOOT Timing Diagram

LVR function can have three different settings configured by BOOT (see “LVREN” in **Table 4-1**).

1. LVR enabled.
2. LVR disabled.
3. Let instructions enable or disable LVR (SLVREN, see **Table 4-2**).

Note: LVR can be instructions disabled in SLEEP to reduce power consumption. The CPU should wake up and enable LVR periodically to monitor V_{DD} if system V_{DD} is unstable.

Name	Status	Register	Addr.	Reset
SLVREN	Applies only when LVREN cedes control to SLVREN 1 = Enables LVR 0 = Disables LVR	MSCON0[3]	0x1B	RW-0

Table 4-2 Instruction Level LVR registers

4.3 Illegal Instruction Reset

There are many reasons a CPU fetches an instruction incorrectly, with interference and V_{DD} instability the most common. When such an event occurs System-Reset.

Illegal instruction reset circuit is always on. Although there is no dedicated Reset instruction, any deliberate illegal instruction is equivalent to a Reset instruction.

4.4 Watch Dog Timer (WDT) Reset

WDT overflows during SLEEP will result in a Wake-Up.

WDT overflows not during SLEEP will trigger a System-Reset. This can reset a hanged CPU. Clear WDT from time to time in the program to avoid false reset.

For details on WDT operation and setting see **Section 7.1** Watch Dog Timer (WDT).

4.5 External System-Reset /MCLRB

The CPU can be reset by a low voltage applied to the /MCLRB (PA5) pin if so configured by BOOT. The /MCLRB pin is usually soft pullup to V_{DD} with a resistor instead of directly, as shown in **Figure 4-3**. The external RC network also provides glitches filtering and over-current protection.

The choice to BOOT or not after a /MCLR System-Reset is made at the IDE (see “MBTEB” in **Table 4-1)**.

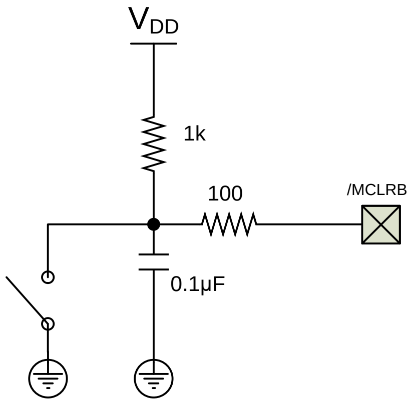


Figure 4-3 /MCLRB reset circuit

4.6 Detecting the Type of Reset Last

Four status flags /POR, /BOR, Time Out (/TF), Power Down (/PF) together can trace the type of last System-Reset, except between “/MCLR System-Reset during normal operation” and “Illegal Instruction Reset”. Use instructions to set the flags to “1”. In a Reset, the corresponding flag(s) latches to “0”.

Reset Source	/POR	/BOR	/TF	/PF
	PCON[1]	PCON[0]	STATUS[4]	STATUS[3]
	0x8E		0x03, 0x83	
POR	0	(unknown)	1	1
LVR	–	0	1	1
WDT overflows while not in SLEEP (Reset)	–	–	0	–
WDT overflows while in SLEEP (Resume)	–	–	0	0
/MCLR Reset during SLEEP	–	–	1	0
/MCLR Reset during normal operation	–	–	–	–
Illegal Instruction	–	–	–	–
On-Chip Debugger (OCD)	–	–	–	–

Table 4-3 Reset Related Status Flags (“–“ no change)

5. LOW VOLTAGE DETECT / COMPARATOR (LVD)

LVD works similarly to a LVR except for the followings:

- None of the control and setting parameters are set by BOOT. They are set by instructions.
- I/O must be set appropriately: TRISx = 1; (PA4 and PA5 may have Digital Input module leakage if not connected to LVD input full time and pad voltage is not V_{DD} or GND.)
- It will write LVDW instead of /BOR.
- It can be instructions configured to Interrupt. It will not trigger System-Reset.
- LVDDEB enables debouncing. Debouncing Time (T_{LVD}) takes 3 to 4 LIRC clock cycles (~94 – 125μs, LIRC will turn on automatically if not already).
- The input to the LVD module can be configured to V_{DD} or other I/O (PA4, PA5). The latter allows the LVD to function as a single input comparator to one of the nine LVDL levels.
- The polarity of LVD can be set, such that the LVD can be a “High” or a “Low” comparator to $V_{LVD\text{-}REF}$.

Note: The external reset function (/MCLRB) of PA5 takes precedence over the LVD input function. When PA5 is configured as an external reset pin, the LVD detection will be ignored.

5.1 Summary of LVD Related Registers

Name	Status		Register	Addr.	Reset
LVDEN	LVD	1 = Enables 0 = Disables	PCON[3]	0x8E	RW−0
LVDL	$V_{LVD-REF}$	0000 = 1.8 0001 = 2.0 0010 = 2.4 0011 = 2.7 0100 = 3.0 0101 = 3.3 0110 = 3.6 0111 = 4.0 1xxx = 1.2	PCON[7:4]		RW−0000
LVDW	LVD triggered?	If LVDP = 0: 1 = Detect voltage < $V_{LVD-REF}$ (no latch) 0 = Detect voltage > $V_{LVD-REF}$ If LVDP = 1: 1 = Detect voltage > $V_{LVD-REF}$ (no latch) 0 = Detect voltage < $V_{LVD-REF}$ Note: when LVDP = 1 and LVDEN = 0, both LVDW and LVDIF are 1.	PCON[2]		RO−x
LVDP	LVDW Polarity	1 = antiphase 0 = non antiphase	WDTCON[7]	0x18	RW−0
LVDDEB	LVD debouncing	1 = Enables 0 = Disables	LVDCON[2]	0x8D	RW−1
LVDM	LVD input	00 = VDD 01 = PA5 10 = PA4 11 = Retention	LVDCON[1:0]		RW−00
LVDIE	LVD Interrupt	1 = Enables 0 = Disables	PIE1[5]	0x8C	RW−0
LVDIF	LVD Interrupted?	1 = Yes 0 = No, or cleared	PIR1[5]	0x0C	RW−0

Table 5-1 Instruction Level LVD Settings and Flags

6. OSCILLATORS and SYSCLK

Instruction chooses whether SysClk is the internal oscillator HIRC, internal oscillator LIRC, or the external oscillator EC, which is determined by BOOT level "FOSC" (**Table 6-1**). Instructions also select the frequency step down divider for internal oscillator (see IRCF in **Table 6-2**). SysClk is used to derive the Instruction Clock:

Instruction Clock = SysClk / N; N = 4 for 4T.

Timers have their own oscillators. More than one oscillator can be active simultaneously.

Oscillators will turn on automatically when the Timers using them are enabled. They will remain active as long as the corresponding Timers are active. The oscillators can be configured to shutdown or be active in SLEEP. By keeping the corresponding oscillator active in SLEEP, Timer functions and PWM can also be active in SLEEP.

As instructions are halted in SLEEP, so will Instruction Clock. Any peripherals using Instruction Clock will also halt in SLEEP.

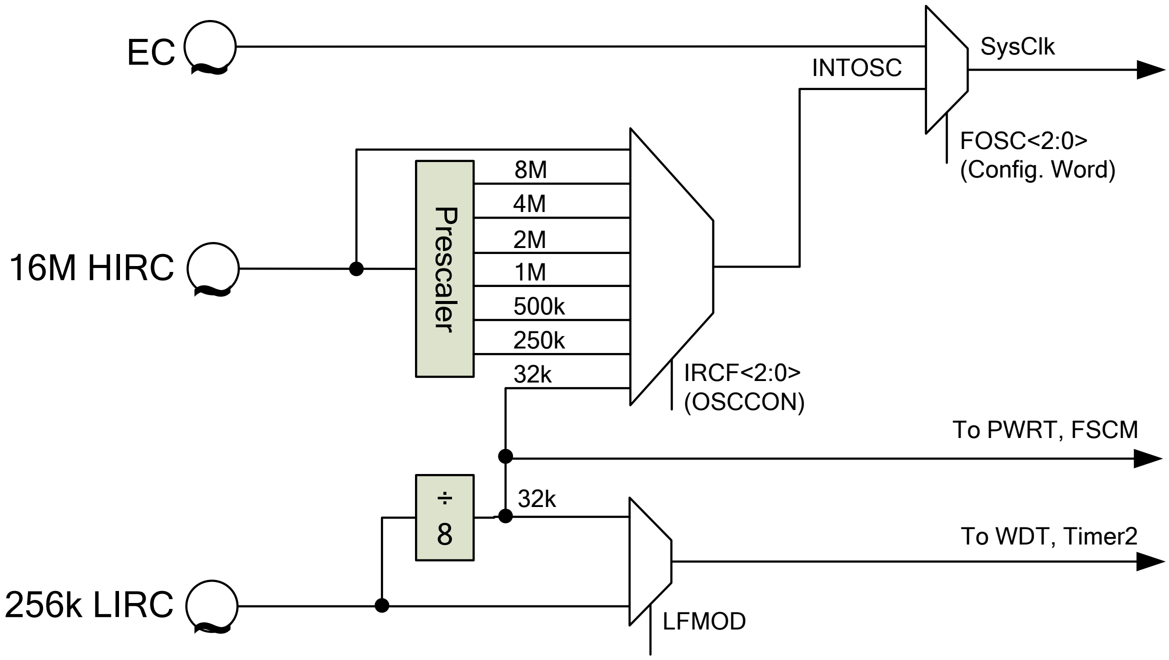


Figure 6-1 Clock source block diagram for SysClk

6.1 Summary of Oscillator Modules Related Registers

Name	Functions	default
FOSC	• EC external oscillator at PA3 (CLKI) (Note: set TRISA[3] = 1) • INTOSCIO mode: PA3 as I/O	INTOSCIO

Table 6-1 BOOT Level FOSC and 2-speed Start-Up configurations

SysClk Source			configuration	
			IRCF	LFMOD
			OSCCON[6:4]	OSCCON[7]
			0x8F	
			RW-100	RW-0
External	EC		-	-
Internal	HIRC	16 MHz	111	-
		8 MHz	110	-
		4 MHz	101	-
		2 MHz	100	-
		1 MHz	011	-
		500 kHz	010	-
		250 kHz	001	-
	LIRC	256 kHz [1]	000	1
		32 kHz [2]	000	0

Table 6-2 Instruction Level SysClk source setup

Name	Status		Register	Addr.	Reset
HTS	HIRC ready (latched)?	1 = Yes 0 = No	OSCCON[2]	0x8F	RO−0
LTS	LIRC ready (latched)?	1 = Yes 0 = No	OSCCON[1]		RO−0
CKMAVG	4x averaging for LIRC and HIRC Cross Calibration	1 = Enables 0 = Disables	MSCON[2]	0x1B	RW−0
CKCNTI	Initiate LIRC and HIRC Cross Calibration 1 = Start 0 = Finished (auto-cleared)		MSCON[1]		RW−0
SOSCPR	LIRC Period Calibrated by # of HIRC clocks		SOSCPR[11:0]	0x1D[3:0] 0x1C	RW−FFF
FOSCCAL	Internal HIRC frequency tunable register		FOSCCAL[5:0]	0x0D	RW−xx xxxx

Table 6-3 Oscillators Control/Status

[1] 256 kHz LIRC is used only for WDT (see WCKSRC and LFMOD in **Table 7-4)** and Timer2 (see T2CKSRC and LFMOD in **Table 7-7**).

[2] Sysclk source (IRCF=000), LIRC and HIRC Cross Calibraion, PWRT and FSCM all use the 32kHz LIRC, regardless of the LFMOD value.

Name	Status	Register	Addr.	Reset
GIE	Global Interrupt 1 = Enables (PEIE, CKMIE applies) 0 = Global Disables (Wake-Up not affected)	INTCON[7]	0x0B 0x8B	RW−0
PEIE	Master Peripheral Interrupt 1 = Enables (CKMIE applies) 0 = Disables (no Wake-Up)	INTCON[6]		RW−0
CKMIE	LIRC Calibration Completed Interrupt 1 = Enables 0 = Disabled (no Wake-Up)	PIE1[6]	0x8C	RW−0
CKMIF	LIRC Calibration completed? 1 = Yes (latched) 0 = No	PIR1[6]	0x0C	RW−0

Table 6-4 Oscillators Interrupt Enable and Status Bits

6.2 Internal Clock Modes (HIRC and LIRC)

Internal high frequency clock (HIRC) is factory calibrated to 16 MHz @ 2.5V/25°C. Typical die to die variation is < ±2.5% at 2.5 − 5.5V, 25°C. The typical temperature variation from $^{-}$40 − $^{+}$85 °C is ±4.0%.

HIRC is calibrated at the wafer level. Packaging may cause the HIRC frequency to drift. There is an option at the downloader to re-calibrate the HIRC. The HIRC frequency trimmed value is stored in the “FOSCCAL” register. Users can change HIRC from the default 16 MHz (tuning). Trimming steps are non-linear (~130 kHz). A rough estimation is as follows:

$$\text{FOSCCAL}[5:0] \pm N \approx 16000 \pm N * 130$$

Internal low frequency clock (LIRC) is factory calibrated to 256 kHz. Typical die to die variations is <±8.5% at 2.5 − 5.5V, 25°C. The temperature variation from $^{-}$40 − $^{+}$85 °C is < ±2.0%.

LIRC and HIRC can be used to cross calibrate each other – A build in hardware uses Timer2 to measure the number of Instruction Clocks (set SysClk to HIRC at 16MHz) in one LIRC period (32 kHz). Since LIRC has a lower temperature coefficient, the HIRC can be calibrated to the LIRC when the temperature fluctuates, thereby achieving the same ±2% temperature coefficient.

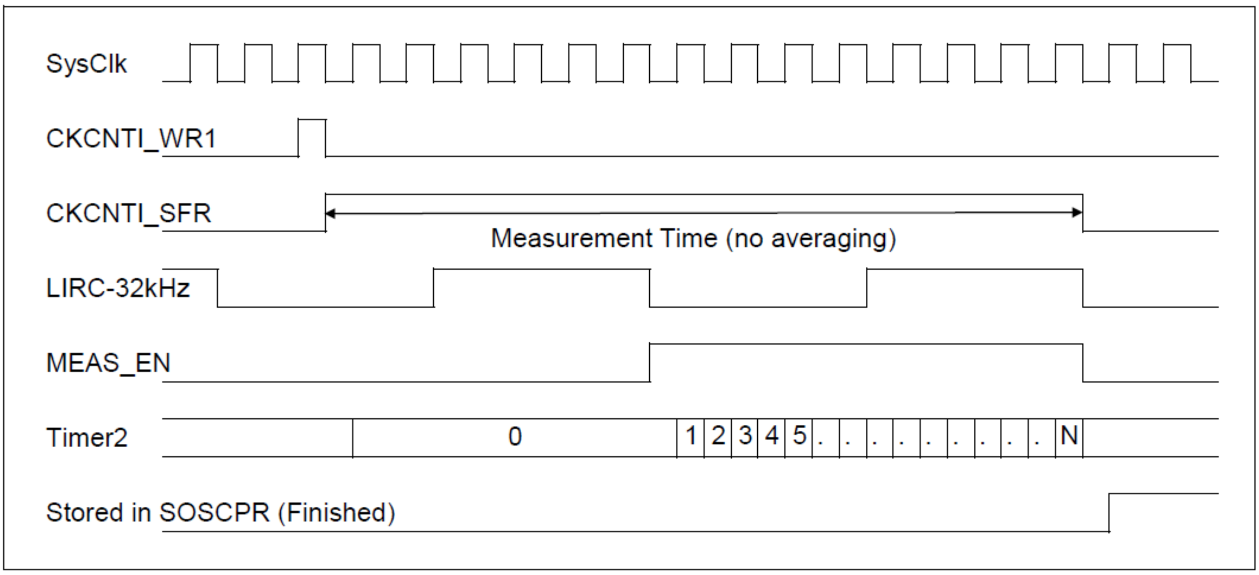

SysClk
CKCNTI_WR1
CKCNTI_SFR
Measurement Time (no averaging)
LIRC-32kHz
MEAS_EN
Timer2
0
1 2 3 4 5 . . . . N
Stored in SOSCPR (Finished)

Figure 6-2 Single measurement timing diagram

To enable LIRC and HIRC Cross Calibration:

1. Set IRCF = 111, SCS = 1 ; select SysClk at 16MHz HIRC (other settings will have a lower accuracy).
2. Set CKMAVG = 1 ; 4 times averaging, choose 0 for no averaging.
3. Set TMR2ON = 1 ; enable Timer2.
4. Set CKCNTI = 1 ; start calibration, automatically Timer2 prescaler = 1, postscalar = 1, T2CKSRC = SysClk
5. At the end of the calibration “CKCNTI =0”, “CKMIF = 1” automatically.
6. Measured value is stored at SOSCPR;
7. LIRC is 32kHz and CPU is running at 16MHz / 4T, the ideal matching number is 500.

Notes：

- Do not write SOSCPRH/L during LIRC and HIRC Cross Calibration.
- Timer2 cannot be used by other peripherals during LIRC and HIRC Cross Calibration.
- LIRC and HIRC Cross Calibration is incompatible with Single Step Debugger mode.

6.3 External Clock Mode (EC)

External digital signal connected to CLKI (PA3) is the clock source. There is no set up or transition time delay when EC is used for SysClk after a POR or a wake-up from sleep.

Note: Set TRISA[3] = 1 when PA3 is used as the external clock input.

6.4 HIRC, LIRC and EC inter-switching

Figure 6-3 shows the timing during inter-switching. If either HIRC or LIRC is shutdown prior to switching (to save power) there is an extra oscillator setup delay time, HTS and LTS indicate the status of the corresponding oscillator respectively.

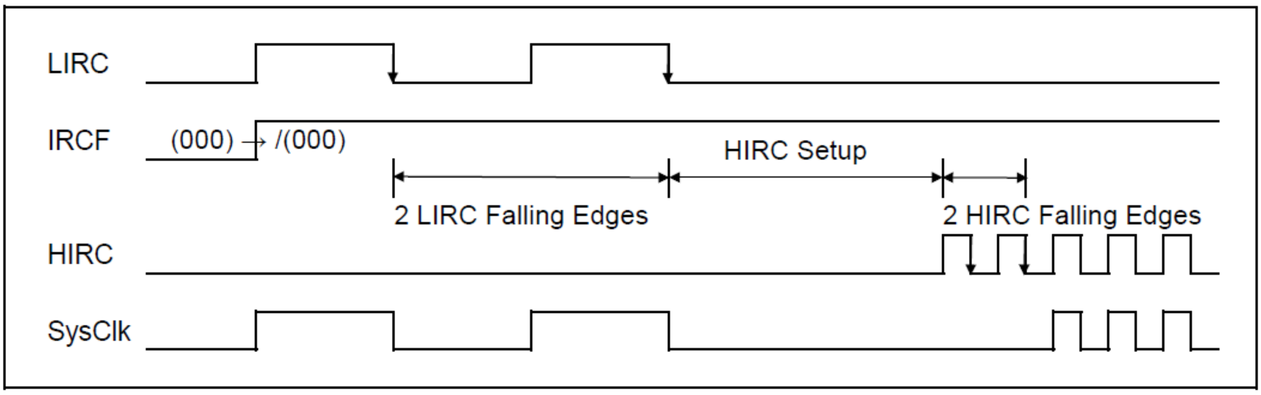


Figure 6-3 Switching from LIRC to HIRC (same principle applies switching among EC, LIRC, HIRC)

6.5 SysClk Output (CLKO)

The SysClk can be output to PA4 by setting SCKEN and SCKOE. When writing SCKCFG, the instruction sequence below must be followed:

```
LDWI 34H
STR EECON1                    ; Set “WREN3, WREN2, WREN1” = “1, 1, 1”
BSR SCKCFG, 7                 ;Set SCKEN = 1
BSR SCKCFG, 1                 ;Set SCKOE = 1, output SysClk to CLKO (PA4)
CLRR EECON1                   ;Clear “WREN3, WREN2, WREN1” = “0, 0, 0”
```

Notes:

1. Clear SCKEN and SCKOE according to the above sequence to disable the SysClk output.
2. Read operation do not require to follow this sequence.
3. Except bit7 and bit1, prohibit writing 1 to other bits of the SCKCFG register.

Name	Status	Register	Addr.	Reset
SCKEN	SysClk Output [SCKEN:SCKOE] : 0x = Disable 10 = Disable 11 = Enable	SCKCFG[7]	0x98	RW−0
SCKOE		SCKCFG[1]		RW−0

Table 6-5 SysClk output (CLKO) control register

7. TIMERS

There are 3 Timers including the Watch Dog Timer (WDT).

	WDT	Timer0	Timer2
Prescaler (bit)	–	8 (WDT shared)	4 (1x, 4x, 16x)
Counter (bit)	16	8	16
Postscaler (bit)	7 (Timer0 shared)	–	4 (1 − 16x)
Clock Sources	• HIRC • LIRC	• HIRC • Instruction Clock • PA2/T0CKI (transition counter)	• HIRC • Instruction Clock • 4x Instruction Clock • LIRC

Table 7-1 Timers' Resources

Notes: If a Timer's clock is not the instruction Clock, set "TMRxON = 0" before changing TMRx.

Any Timer enabled will turn on its clock source automatically. Instruction Clock is disabled at SLEEP so it cannot be used for WDT.

WDT postscaler and Timer0 prescaler shares the same hardware. The hardware is Instruction Level assigned to one, but not both. The Timer not assigned the scaler will have a scaler value of "1".

In a POR or System-Reset, all Timers' counter, prescaler, postscalar are reset except Timer0 counter. The followings will also reset a Timer's counter and scaler(s):

	WDT	Timer0	Timer2
Prescaler	–	• TMR0 write • PSA switching	• TMR2ON = 0 • LIRC and HIRC Cross Calibration start • T2CON0, TMR2L/H write
Counter	• WDT overflow • Enters/Exits SLEEP • CLRWDT • WDTCON write • WDTCON =0 & SWDTEN = 0	• Timer0 overflows	• TMR2 = PR2 (matches)
Postscaler	• All Above except WDTCON write • PSA switching	–	• All Above except (TMR2ON = 0)

Table 7-2 Events reseting a Timer's Counter and Scaler(s)

Timer2 Counter, Prescaler and Postscaler will stop incrementing upon a PWM break, for as long as the Break condition remains. It will resume after the PWM Break condition no long exist.

The end of a PWM Single Pulse will set "TMR2ON = 0". Restart by setting "TMR2ON = 1".

7.1 Watch Dog Timer (WDT)

WDT is used to “Wake-Up from SLEEP” or “System-Reset if the CPU stalls”. WDT counts the number of clock cyles to a pre-set number until overflow.

- In SLEEP mode, a WDT overflow will trigger a Wake-up. The CPU will resume operation from where it is before SLEEP. This is not an Interrupt nor System-Reset event.
- In non-SLEEP mode, a WDT overflow will trigger a System-Reset (see **Section 4** System-Reset).

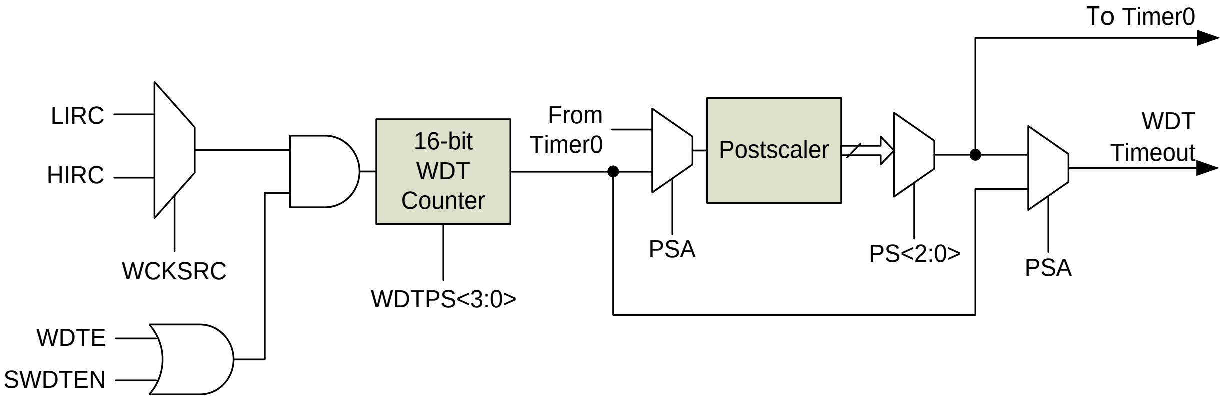


Figure 7-1 Block diagram of WDT

The WDT will overflow after a WatchDog-Time: WDT-Period x WDT-Postscaler / WDT Clock Frequency.

For a given Clock Source, WatchDog-Time step doubles successively due to the binary nature of the WDT Postscalar. Using LIRC as clock source, the maximum settable time before WDT overflows is

$$2^{16} \text{ x } 2^{7} \text{ / 32kHz = ~262 seconds.}$$

7.1.1 Summary of WDT Related Registers

Name	Functions	default
WDTE	WDT • Enabled (overrides Instructions disable) • Instruction controlled (SWDTEN)	SWDTEN control

Table 7-3 BOOT Level WDT Selectors

<table>
<tr><th>Name</th><th colspan="5">Status</th><th>Register</th><th>Addr.</th><th>Reset</th></tr>
<tr><td>WCKSRC</td><td colspan="5">WDT Clock Source
0 = LIRC
1 = HIRC</td><td>WDTCON[5]</td><td rowspan="3">0x18</td><td>RW−0</td></tr>
<tr><td>WDTPS</td><td colspan="5">WDT Period
0000 = 32
0001 = 64
0010 = 128
0011 = 256
0100 = 512 (Default)
0101 = 1,024
0110 = 2,048
0111 = 4,096
1000 = 8,192
1001 = 16,384
1010 = 32,768
1011 = 65,536
11xx = 65,536</td><td>WDTCON[4:1]</td><td>RW−0100</td></tr>
<tr><td>SWDTEN</td><td colspan="5">1 = WDT Enables
0 = WDT Disables, if WDTE choosed SWDTEN control</td><td>WDTCON[0]</td><td>RW−0</td></tr>
<tr><td>LFMOD</td><td colspan="5">1: LIRC = 256 kHz
0: LIRC = 32 kHz</td><td>OSCCON[7]</td><td>0x8F</td><td>RW−0</td></tr>
<tr><td>PSA</td><td colspan="5">1 = Scalar assigned as WDT Postscalar
0 = Scalar assigned as Timer0 Prescalar</td><td>OPTION[3]</td><td rowspan="4">0x81</td><td>RW−1</td></tr>
<tr><td rowspan="3">PS</td><td></td><td colspan="2">WDT Postscalar</td><td colspan="2">Timer0 Prescalar</td><td rowspan="3">OPTION[2:0]</td><td rowspan="3">RW−111</td></tr>
<tr><td>000
001
010
011
100
101
110
111</td><td>(PSA=1)</td><td>1
2
4
8
16
32
64
128</td><td>(PSA=0)</td><td>2
4
8
16
32
64
128
256</td></tr>
<tr><td>xxx</td><td>(PSA =0)</td><td>1</td><td>(PSA =1)</td><td>1</td></tr>
</table>

Table 7-4 Instruction Level WDT Related Registers

7.1.2 Setting up and using the WDT

WDTE (BOOT Level) and/or SWDTEN (Instruction Level) enable the WDT.

WCKSRC (and LFMOD if the LIRC is selected) chooses the WDT clock source. WDTPS, PSA and PS together set the Postscalers. Clock source will turn on automatically when the WDT using it is enabled, and will remain active in SLEEP mode.

To stop a WDT overflow, the WDT must be cleared before time expires. Refer to **Table 7-2** for events that will clear the WDT. Counting continues after WDT is cleared.

7.1.3 Switching scaler between Timer0 and WDT

As a result of having the same scaler assigned to either Timer0 or the WDT, it is possible to generate an unintended System-Reset when switching scaler between Timer0 and WDT.

When switching scaler assignment from Timer0 to WDT, the instruction sequence below must be followed.

```
BANKSEL TMR0                    ; Can skip if already in TMR0 bank
CLRWDT                          ; Clear WDT
CLRR TMR0                       ; Clear TMR0 and scaler
BANKSEL OPTION
BSR OPTION, PSA                 ; Select WDT
LDWI b'11111000'                ; Mask scaler bits (PS2-0)
ANDWR OPTION, W
IORWI b'00000101'               ; Set WDT scaler bits to 32 (or any value desired)
STR OPTION
```

When switching scaler assignment from WDT to Timer0, the instruction sequence below must be followed.

```
CLRWDT                          ; Clear WDT and scaler
BANKSEL OPTION                  ;
LDWI b'11110000'                ; Mask TMR0 select and scaler bits (PSA, PS2-0)
ANDWR OPTION, W
IORWI b'00000011'               ; Set Timer0 scale to 16 (or any value desired)
STR OPTION
```

7.2 TIMER0

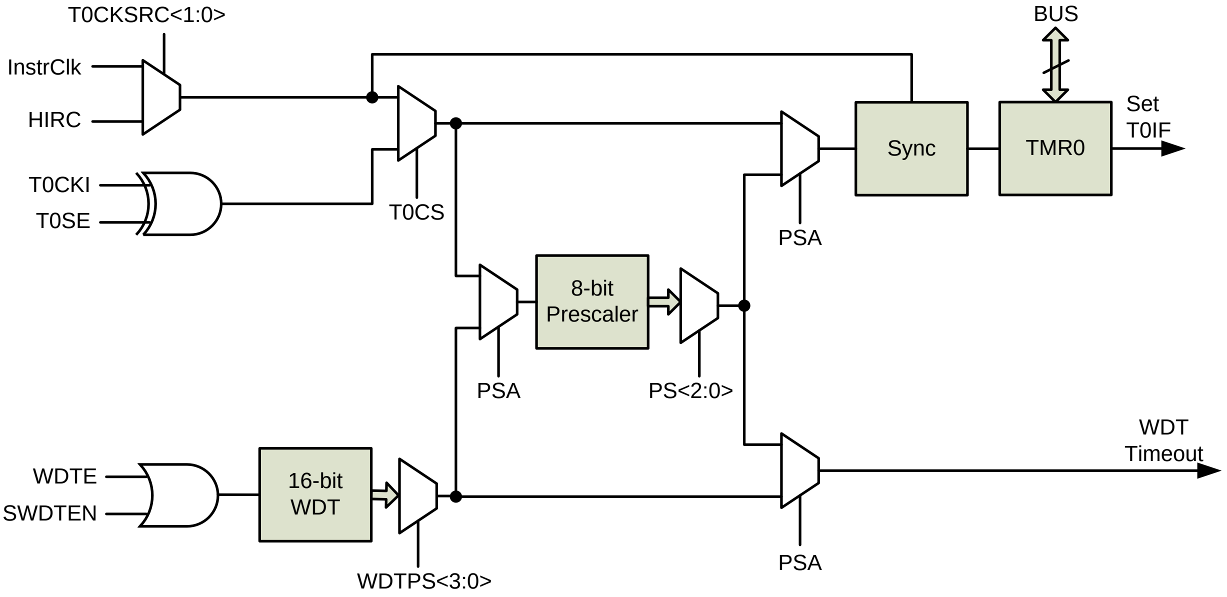


Figure 7-2 Block diagram of Timer0

Timer0 is used to count transitions at an I/O “PA2−T0CKI”, or as a timer to keep time (see T0CKSRC).

Timer0 counts and overflows upon reaching a time = *TMR0[7:0] * Timer0_Prescaler*

An Interrupt flag (T0IF) is set. Depends on the enable controls (T0IE and GIE) it may result in an AWAKE from SLEEP and/or Interrupt.

Notes:

1. Timer0 stops for two instruction cycles immediately following writing TMR0.
2. To be able to Wake-Up from SLEEP, set “T0CKRUN = 1” and “T0CKSRC ≠ 00” so Timer0 will not use Instruction Clock and be active in SLEEP. Or Timer0 will retain the value before entering SLEEP.
3. If Timer0 is used to count T0CKI, there are minimum period, high and low pulse width requirements relative to Timer0. However unless T0CKI is very fast and T_{T0CK} is very slow, the restrictions will usually be satisfied.

T0CKI	Minimum	Units	Conditions
High or Low Pulse Width	$0.5 * T_{T0CK} + 20$	ns	no Prescaler
	10	ns	with Prescaler

Period	maximum(20, $(T_{T0CK}+40)/N$)	ns	N = 1, 2, 4, …, 256 (with Prescaler)
			N = 1 (no Prescaler)

4. See **Section 7.1.3** regarding “Switching scaler between Timer0 and WDT modules”

7.2.1 Summary of Timer0 Related Registers

Name	Status					Register	Addr.	Reset
T0ON	Timer0	1 = Enables 0 = Disables				T0CON0[3]	0x1F	RW−1
T0CKRUN	T0CK run in SLEEP	1 = Yes (if not Instr. Clock) 0 = No				T0CON0[2]		RW−0
T0CKSRC	Timer0 Clock Source (T0CS = 0) 00 = Instruction Clock 01 = HIRC 1x = Retention					T0CON0[1:0]		RW−00
T0CS	Timer0 Input Source	1 = PA2/T0CKI (Counter) 0 = T0CKSRC (Timer)				OPTION[5]	0x81	RW−1
T0SE	Counter Trigger	1 = Falling Edge 0 = Rising Edge				OPTON[4]		RW−1
PSA	1 = Scalar assigned as WDT Postscalar 0 = Scalar assigned as Timer0 Prescalar					OPTION[3]		RW−1
PS		WDT Postscalar		TIMER0 Prescalar		OPTION[2:0]		RW−111
	000		1		2			
	001		2		4			
	010		4		8			
	011	(PSA=1)	18	(PSA=0)	16			
	100		16		32			
	101		32		64			
	110		64		128			
	111		128		256			
	xxx	(PSA =0)	1	(PSA =1)	1			
TMR0[7:0]	Timer0 Count Value					TMR0[7:0]	0x01	RW−xxxx xxxx

Table 7-5 Instruction Level Timer0 Related Control Registers

Name	Status		Register	Addr.	Reset
GIE	Global Interrupt	1 = Enables (T0IE applies) 0 = Global Disables (Wake-Up not affected)	INTCON[7]	0x0B 0x8B	RW−0
T0IE	Timer0 Overflow Interrupt	1 = Enables 0 = Disables (no Wake-Up)	INTCON[5]		RW−0
T0IF	Timer0 Overflow Interrupt?	1 = Yes (latched) 0 = No	INTCON[2]		RW−0

Table 7-6 Timer0 Interrupt Enable and Status Bits

7.3 TIMER2

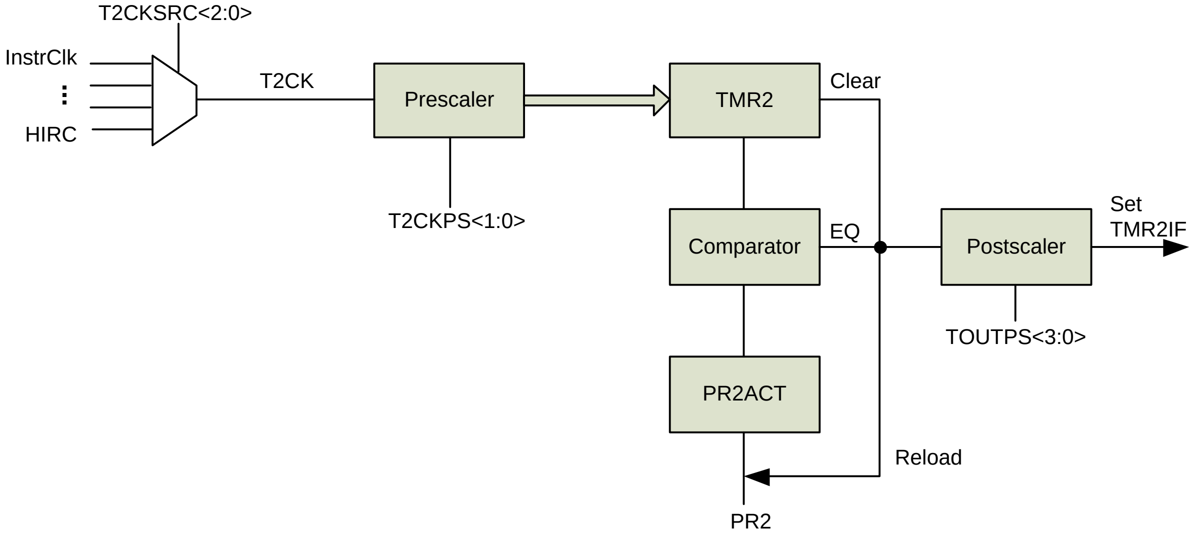


Figure 7-3 Timer2 block diagram

Timer2 is used as a timer. It is also for generating the PWM (without Postscalar, see **Section 10** PWM), and for LIRC and HIRC Cross Calibration counting (CKCNTI=1). Counter matches and postscalar overflows function can be used simultaneously.

T2CKSRC (and LFMOD if the LIRC is selected) chooses the Timer2 clock source. Timer2 clock is fed into Timer2 Prescaler (options of 1, 4 or 16). The Prescaler output increments TMR2 from 0x00 until it matches PR2. Upon matching:

1. TMR2 resets to 0x00 on the next increment cycle
2. Timer2 Postscaler increments.
3. Timer2 overflows when Timer2 post-scaler output is equal to the post-scaler setting (1, 2 …. 15 or 16).
4. Interrupt flag TMR2IF is set to 1. Depends on the enable controls (GIE, PEIE and TMR2IE) it may result in an AWAKE from SLEEP and/or Interrupt.

Notes:

1. TMR2 is not cleared when T2CON0 is written.
2. Both TMR2 and PR2 are R/W. They are 0x0000 and 0xFFFF respectively when reset.
3. If (“TMR2ON = 1”, “T2CKRUN = 1”, “T2CKSRC ≠ 000”), Timer2 will run in SLEEP.

7.3.1 Summary of Timer2 Related Registers

Name	Status	Register	Addr.	Reset
T2CKRUN	T2CK run in SLEEP 1 = Yes (if not Instruction Clock) 0 = No	MSCON0[0]	0x1B	RW−0
PR2U	New Period and Duty Cycle effective immediately 1 = PR2ACT and P1xDTyACT update from PR2/P1xDTy buffer immediately 0 = Normal update after end of a period	T2CON0[7]	0x12	RW1−0
TOUTPS	Timer2 Post-scaler 0000 = 1 0100 = 5 1000 = 9 1100 = 13 0001 = 2 0101 = 6 1001 = 10 1101 = 14 0010 = 3 0110 = 7 1010 = 11 1110 = 15 0011 = 4 0111 = 8 1011 = 12 1111 = 16	T2CON0[6:3]		RW− 0000
TMR2ON	Timer2 (clear in PWM One-pulse mode) 1 = Enables 0 = Disables	T2CON0[2]		RW−0
T2CKPS (T1CKPS)	Timer2/Timer1 Prescaler 00 = 1 1x = 16 01 = 4	T2CON0[1:0]		RW−00
T2CKSRC	Timer2 Clock Source 000 = Instruction Clock 100 = HIRC 001 = 4 x Instruction Clock 101 = LIRC 01x = Retention 11x = Retention	T2CON1[2:0]	0x9E	RW−000
LFMOD	1: LIRC = 256kHz 0: LIRC = 32kHz	OSCCON[7]	0x8F	RW-0
PR2L	LSB of PR2 period register	PR2L[7:0]	0x91	RW−1111 1111
PR2H	MSB of PR2 period register	PR2H[7:0]	0x92	RW−1111 1111
TMR2L	LSB of TMR2 count register	TMR2L[7:0]	0x11	RW−0000 0000
TMR2H	MSB of TMR2 count register	TMR2H[7:0]	0x13	RW−0000 0000

Table 7-7 Instruction Level Timer2 Related Control Registers

Name	Status	Register	Addr.	Reset
GIE	Global Interrupt 1 = Enables (PEIE, TMR2IE applies) 0 = Global Disables (Wake-Up not affected)	INTCON[7]	0x0B 0x8B	RW−0
PEIE	Master Peripheral Interrupt 1 = Enables (TMR2IE applies) 0 = Disables (no Wake-Up)	INTCON[6]		RW−0
TMR2IE	Timer2 matched PR2 Interrupt 1 = Enables 0 = Disables (no Wake-Up)	PIE1[1]	0x8C	RW−0
TMR2IF	Timer2 matched PR2 Interrupt? 1 = Yes (latched) 0 = No	PIR1[1]	0x0C	RW−0

Table 7-8 Timer2 Interrupt Enable and Status Bit

7.3.2 R/W Operation of Timer2 register

TMR2H and TMR2L cannot be READ or WRITE simultaneously. Latches solves this problem. The following Read and Write sequences must be followed.

- To READ TMR2, read TMR2L first. Latches will latch TMR2H to a buffer TMR2H_buf, which is read next. If Timer2 clock is not Instruction Clock, set “TMR2ON =0”, execute a NOP before reading TMR2.
- To WRITE TMR2, write TMR2H first. It will be stored in a TMR2H_buffer. Writing TMR2L next will update both TMR2H and TMR2L simultaneously. To avoid racing between writing and counting, TMR2 should be stopped prior to writing by setting “TMR2ON = 0”.

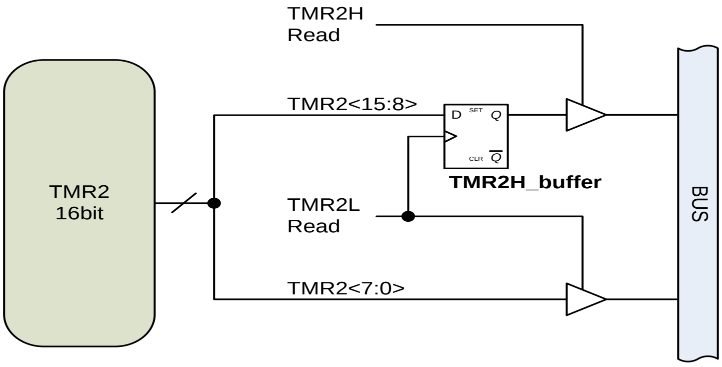


Figure 7-4 TMR2 Read Block Diagram

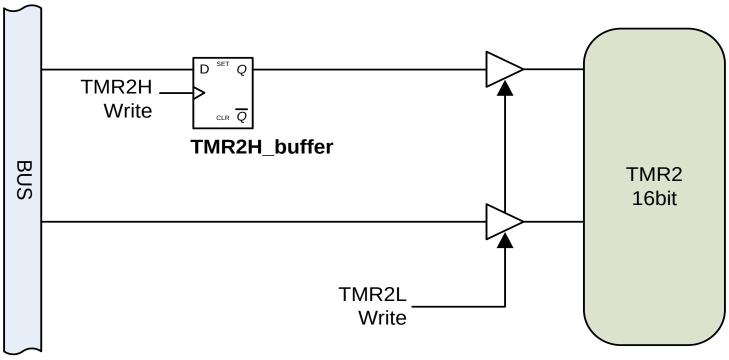


Figure 7-5 TMR2 Write Block Diagram

8. SLEEP (POWER-DOWN)

During SLEEP Instruction Clock is inactive and instructions execution is halted. Most modules are powered down to conserve power. As listed in **Table 8-1**, FT60E21x can selectively turn on individual modules in SLEEP so that functions, LVR, LVD, WDT, Timers and PWM, can be maintained during SLEEP if desired without instruction interventions. Some modules can configure automatic power down upon SLEEP to save the need to turn them off by instructions.

	Condition in SLEEP	
	RUN	Auto-Shutdown?
Instruction Clock	(always power down)	Yes
LVR (Configure the LVREN)	Enabled or Instruction controlled (SLVREN=1)	No
LVD	LVDEN = 1	No
WDT	WDTE or SWDTEN	No
TIMER0	T0CKRUN = 1 & T0CKSRC ≠ 00 & T0ON = 1	T0CKRUN=0
TIMER2	T2CKRUN = 1 & T2CKSRC ≠ 000 & TMR2ON = 1	T2CKRUN=0
PWM	(follows TIMER2)	
HIRC / LIRC / EC	(follow peripherals that are using them)	
I/O	(maintain their states before SLEEP unless PWM SLEEP enabled)	

Table 8-1 All except Instruction Clock can remain active in SLEEP if so desired

8.1 Entering into SLEEP

A SLEEP command puts the CPU to SLEEP.

1. If WDT is enabled, it will clear its Postscalar (if assigned) and counter, and start counting.
2. Time Out Flag (/TF) = 1
3. Power Down Flag (/PF) = 0
4. Clock sources
   - Instruction Clock shuts down automatically.
   - HIRC, LIRC, external oscillators (EC, LP, XT) are active if the Timer that uses them remains active. If a certain Timer auto-shutdown in SLEEP, its clock source will auto-shutdown too unless it is used by another Timer that remains active.
   - Instruction Clock will stop, and therefore output will not update anymore even if configured so.
5. I/O PORTS
   - PWM output continue if Timer2 is active in SLEEP. PWM auto-shutdown if Timer2 auto-shutdown.
   - For other digital outputs, they will maintain the state before SLEEP ((Tri-state, “0” or “1”)

For more information about how peripherals work in SLEEP please refer to the corresponding chapters.

8.2 Waking-Up from SLEEP

There are 2 general principles to Wake-up from sleep:

- Time based, in which the CPU wakes up after a certain amount of time. LIRC is the clock choice for keeping time as it has lower power consumption than HIRC.
- Events based that triggers POR, System-Reset, Wake-up without Interrupt, and Interrupts, such as LVD, Interrupt-on-change, PA2-INT.

The situations Wake-up from sleep as follows:

1. Watchdog Timer Wake-up if enabled (see **Section 7.1** Watchdog Timer).
2. Full-Reset and System-Reset
    - POR Full-Reset (cannot be disabled)
    - External System-Reset by the /MCLR if enabled
    - LVR Reset if enabled
3. Enabled Interrupts (Disabling the “Global Interrupt Enable” will not stop Wake-up). Please see **Section 9** Interrupts.

Notes:

1. Waking up will also clear WDT.
2. SLEEP must be followed by NOP

   In Wake-up from SLEEP not preceeded by execution of the “Interrupt Service Routine”, such as WDT wakeup, or attempted Interrupts with Global Interrupt Enable (GIE) disabled, the next instruction will be executed twice. To avoid duplicate execution NOP must follow SLEEP.

```
SLEEP
NOP          // harmless NOP will execute twice if Interrupt Service Routine not executed.
```

9. INTERRUPTS

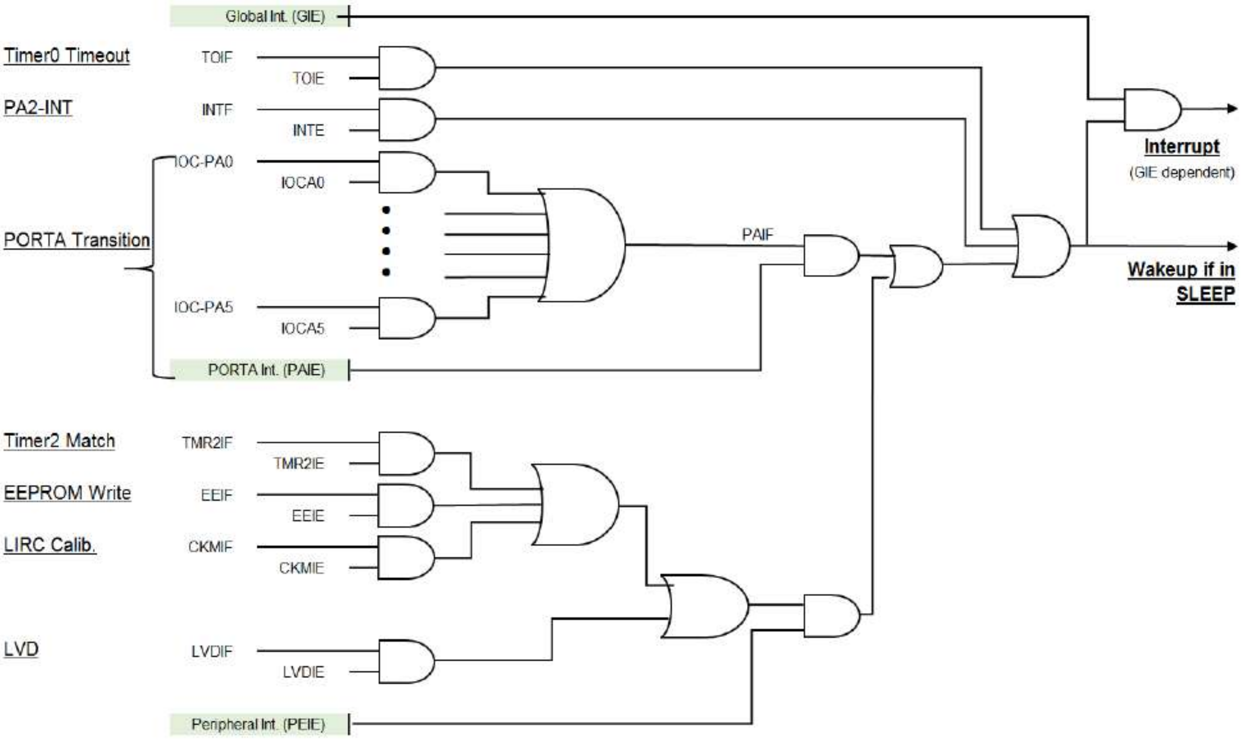


Figure 9-1 Interrupt Block Diagram

The CPU supports 7 sources of Interrupt in 2 groups:

1) Non-Peripherals (Timer0 and I/O)

- Timer0 Overflows
- PA2−INT (automatic rising or falling edge interrupt)
- PORTA Interrupt-on-Change (software controlled)

2) Peripherals

- Timer2 Postscalar overflows
- DATA EEPROM Write Completion
- LIRC and HIRC Cross Calibration Completion
- LVD condition matches

WDT overflows, unlike other Timers, will not result in an Interrupt. For other interrupts besides external I/O interrupts please see the corresponding chapters.

In an Interrupt the PC jumps to and executes the "Interrupt Service Routine (ISR)". There are multiple levels of Interrupt Disable/Enable.

- Each interrupt source has a local interrupt enable: T0IE, INTE, IOCAx, TMR2IE, EEIE, CKMIE, LVDIE
- The 6 PAx Interrupt Inputs have a group PORT interrupt enable: PAIE (PORTA Interrupt Enable)
- The Peripheral interrupts has a master interrupt enable: PEIE (PEripheral Interrupt Enable).
- All controls above, if disabled, will not execute a Wake-Up from SLEEP.
- All interrupts are controlled by a global enable: GIE (Global Interrupt Enable). This enable differs from the others by allowing a Wake-Up from SLEEP even when disabled.
- Disabling the interrupts does not affect the setting of the interrupt flags.

The following sequences occur upon an Interrupt:

- Automatic set "GIE = 0", disabling further interrupts.
- The return address is pushed onto the stack and the PC (program counter) is loaded with 0x0004.
- Jump to the "Interrupt Service Routine" 1 – 2 instruction cycles after the interrupt.
- "Return from Interrupt (RETI)" instruction exits ISR. Prior to RETI must clear the interrupt flag currently being processed.
- At the completion of the ISR, the PC returns to the address before the interrupt, which in SLEEP, is the address immediate after SLEEP.
- Automatic set GIE = 1 upon executing RETI, enabling future interrupts.

Note: Only the return PC is saved on the stack during an interrupt. Users desiring to have other registers (e.g., W and STATUS) saved must use instructions to write them into temporary registers explicitly. Use the last 16 bytes of SRAM for temporary storages as they are common to all banks and do not require bank swithing.

9.1 Summary of Interrupt Related Registers

Name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset (RW)
INTCON	0x0B	GIE	PEIE	T0IE	INTE	PAIE	T0IF	INTF	PAIF	0000 0000
PIE1	0x8C	EEIE	CKMIE	LVDIE	–	–	–	TMR2IE	–	000- --0-
PIR1	0x0C	EEIF	CKMIF	LVDIF	–	–	–	TMR2IF	–	000- --0-
OPTION	0x81	/PAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
TRISA	0x85	–		PORTA direction select						--11 1111
IOCA	0x96	–		Interrupt on PORTA Logic-Changes						--00 0000

Table 9-1 Interrupt Related Register Addresses and Default

Name	Status		Register	Addr.	Reset
GIE	Global Interrupt	1 = Enables (PEIE, local settings applies) 0 = Global Disables (Wake-Up not affected)	INTCON[7]	0x0B 0x8B	RW−0
PEIE	Master Peripheral Interrupt	1 = Enables (local settings applies) 0 = Disables (no Wake-Up)	INTCON[6]		RW−0
T0IE	Timer0 Overflow Interrupt	1 = Enables 0 = Disables (no Wake-Up)	INTCON[5]		RW−0
INTE	PA2−INT External Interrupt		INTCON[4]		RW−0
PAIE	PORTA Interrupt-on-Change		INTCON[3]		RW−0
T0IF	Timer0 Overflow Interrupt?	1 = Yes (latched) 0 = No	INTCON[2]		RW−0
INTF	PA2−INT External Interrupt?		INTCON[1]		RW−0
PAIF	PORTA Interrupt-on-Change?		INTCON[0]		RW−0

Table 9-2 INTCON register

Name	Status		Register	Addr.	Reset
EEIE	EE Write Completed Interrupt	1 = Enables 0 = Disabled (no Wake-Up)	PIE1[7]	0x8C	RW−0
CKMIE	LIRC Calibration Completed Interrupt		PIE1[6]		RW−0
LVDIE	LVD Interrupt		PIE1[5]		RW−0
TMR2IE	Timer2 matched PR2 Interrupt		PIE1[1]		RW−0

Table 9-3 PIE1 register

Name	Status		Register	Addr.	Reset
EEIF	EEPROM Write operation completed?	1 = Yes (latched) 0 = No	PIR1[7]	0x0C	RW−0
CKMIF	LIRC Calibration completed?		PIR1[6]		RW−0
LVDIF	LVD interrupt?		PIR1[5]		RW−0
TMR2IF	Timer2 matching PR2 interrupt?		PIR1[1]		RW−0

Table 9-4 PIR1 register

Name	Status	Register	Addr.	Reset
/PAPU	PORTA Pull-Up 1 = Global Disables 0 = Enables WPUA settings	OPTION[7]	0x81	RW−1
INTEDG	PA2 Interrupt Edge 1 = Rising 0 = Falling	OPTION[6]		RW−1
TRISA	PORTA I/O Digital Output (Direction) 1 = Input (Disables Digital Output) 0 = Disables Pull-Up	TRISA[5:0]	0x85	RW−111111
IOCA	PORTA Interrupt-on-Change 1 = Enables 0 = Disables	IOCA[5:0]	0x96	RW−000000

Table 9-5 OPTION, TRISA and IOCA registers

9.2 PA2-INT and PORTA Interrupt-on-Change

Name	PA2-INT	PORTA Logic-Changes
Channel(s)	PA2 only	PA0 – PA5 (up to 6 channels)
I/O Setup	TRISA[2] = 1	TRISA[x] = 1
Other settings	INTEDG, INTE, GIE, INTF	IOCA, PAIE, GIE, PAIF
Trigger	either Rising or Falling, not both	0 → 1 or 1 → 0
Software Monitoring?	No	Required

Table 9-6 Differences between PA2-INT and PORTA Interrupt-on-Change

PA2-INT and PORTA Interrupt-on-Change are the external I/O interrupts. PA2 can be as both. PA2-INT will run unsupervised in the backgroup once setup properly. PORTA Interrupt-on-Change will need continuous software monitoring. For PORTA Interrupt-on-Change:

1. Latches Input Register into an Interrupt-On-Change latch (READ PORTA).
2. When input logic level changes, the difference in Input Register and latched data will set PAIF.
3. Latching Input Register will update compare reference, and if done immediately after PAIF is set have the effect of removing the Interrupt-On-Change trigger condition. PAIF can be instruction cleared when the Interrup-On-Change condition is no longer valid.

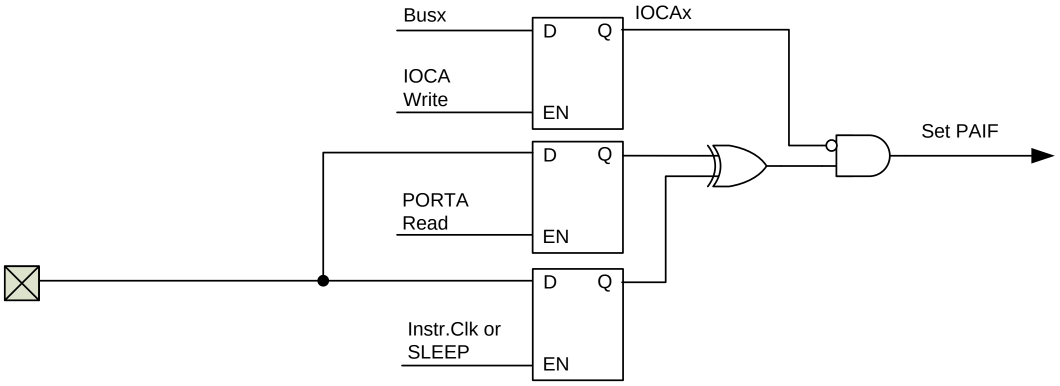


Figure 9-2 PORTA Transition interrupts

10. PWM

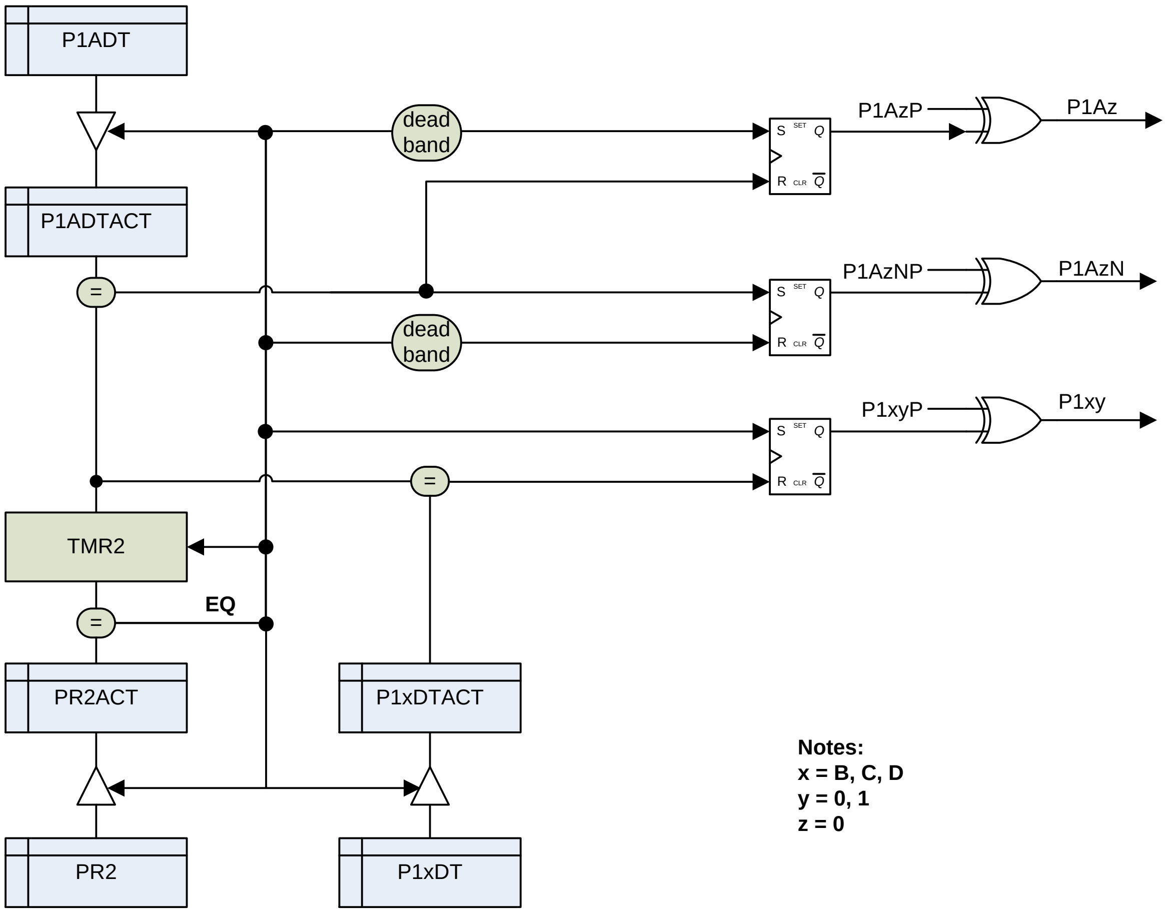


Figure 10-1 PWM block diagram

PWM features:

- 4 PWM channels with independent Duty Cycles: P1A, P1B, P1C, P1D
- All 4 channels are controlled by Timer2 with a same Period.
- Channel 1 with complementary output /P1A
- Channel 1 with Deadband control: P1A, /P1A
- 16−bit resolution ratio
- Independent polarity control for each PWM channel
- Multiple Break options with selectable Auto Resume
- PWM3 and PWM4 can map out to 2 I/O each.
- XOR/XNOR secondary output functions
- Buzzer Mode
- One-pulse output mode.
- Period and Duty Cycle registers Double buffered read and write.

PWM Operation during SLEEP – PWM will keep running as long as it is enabled and Timer2 is running (see **Section 7.3** Timer2), SLEEPING or not. If Timer2 auto-shutdown at SLEEP, then PWM outputs will be frozen at the states before SLEEP. Timer2 clock source cannot be the Instruction Clock during SLEEP.

10.1 Summary of PWM Related Registers

	Timer2 Period		Timer2 Counter		Duty Cycle		Deadband time
	MSB	LSB	MSB	LSB	MSB	LSB	
PWM1	PR2H	PR2L	TMR2H	TMR2L	P1ADTH	P1ADTL	P1DC
/PWM1							
PWM2					P1BDTH	P1BDTL	–
PWM3					P1CDTH	P1CDTL	–
PWM4					P1DDTH	P1DDTL	–

Name	Address	bit 7	bit 6 - 0	Reset (RW)
PR2H	0x92	PR2 Period MSB		1111 1111
PR2L	0x91	PR2 Period LSB		1111 1111
TMR2H	0x13	Timer2 counter MSB		0000 0000
TMR2L	0x11	Timer2 counter LSB		0000 0000
P1ADTH	0x14	P1A duty cycle MSB		0000 0000
P1ADTL	0x0E	P1A duty cycle LSB		0000 0000
P1BDTH	0x15	P1B duty cycle MSB		0000 0000
P1BDTL	0x0F	P1B duty cycle LSB		0000 0000
P1CDTH	0x1A	P1C duty cycle MSB		0000 0000
P1CDTL	0x10	P1C duty cycle LSB		0000 0000
P1DDTH	0x09	P1D duty cycle MSB		0000 0000
P1DDTL	0x08	P1D duty cycle LSB		0000 0000
P1CON	0x16	P1AUE	P1DC (deadband time)	0000 0000

Table 10-1 PWM Timing Setup

	Channel Assignments		Output		Polarity
	Ch 0	Ch 1	Ch 0	Ch 1	Ch 0
PWM1	PA3	–	P1A0OE	–	P1A0P
/PWM1	PA4	–	P1A0NOE	–	P1A0NP
PWM2	PA4	–	P1BOE	–	P1BP
PWM3	PA2	PA0	P1COE	P1CALT	P1CP
PWM4	PA1	PA5	P1DOE	P1DALT	P1DP

Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Addr	Reset (RW)
P1BR1	P1DSS [1:0]		P1D2SS [1:0]		P1CALT	P1DALT	P1CSS [1:0]		0x19	0000 0000
P1OE	P1COE	P1BOE	P1DOE	–	P1C2SS[1:0]		P1A0NOE	P1A0OE	0x90	000– 0000
P1POL	P1CP	P1BP	P1DP	–	–	–	P1A0NP	P1A0P	0x99	000– ––00

Table 10-2 PWM Output Polarities (1 = reversed, 0 = normal) and Enables (1 = Enables, 0 = Disables)

	Disabled = 0, Enabled = 1		**XOR = 0, XNOR = 1**		Secondary Functions
	Ch 0	Ch 1	Ch 0	Ch 1	
PWM1	–	–	–	–	N/A
/PWM1	–	–	–	–	N/A
PWM2	–	–	–	–	N/A
PWM3	–	–	–	–	N/A
PWM4	–	P1DF2E	–	P1DF2	P1B xor/xnor P1C

Name	Address	bit 7 ~ bit 2	bit 1	bit 0	Reset (RW)
P1AUX	0x1E	–	P1DF2E	P1DF2	00

Table 10-3 PWM Secondary Functions

Name	Control affecting all 4 PWMs	Register	Addr.	Reset
PR2U	New Period and Duty Cycle effective immediately 1 = PR2ACT and P1xDTyACT update from PR2/P1xDTy buffer immediately 0 = Normal update after end of a period	T2CON0[7]	0x12	RW1−0
P1OS	1 = One pulse mode 0 = Normal Continous mode	T2CON2[4]	0x9E	RW−0
P1BZM	1 = Buzzer mode at 50% duty cycle 0 = Normal PWM mode	T2CON2[3]		RW−0

Table 10-4 PWM Control Functions affecting all 4 PWMs

Name	Control	Register	Addr.	Reset
P1BKS	PWM Fault 000: Disables Fault-break 001: BK0 = 0 010: BK0 = 1 011: LVDW =1 100: LVDW = 1 or BK0 = 0 101: LVDW = 1 or BK0 = 1 11x: Fault-Break function disable	P1BR0[6:4]	0x17	RW−0
P1AUE	PWM auto resume 1 = PWM auto resume, P1BEVT clears upon exiting Fault-Break 0 = PWM resume after P1BEVT cleared by instructions	P1CON[7]	0x16	RW−0

Table 10-5 PWM Fault Source and Auto Resume

Name	Status	Register	Addr.	Reset
P1BEVT	PWM Fault-Break? 1 = Yes (latches until clear) 0 = No	P1BR0[7]	0x17	RW−0

Table 10-6 PWM Fault-Break Status

Name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset(RW)
P1BR0	0x17	P1BEVT	P1BKS [2:0]			P1BSS		P1ASS		0000 0000
P1BR1	0x19	P1DSS		P1D2SS		P1CALT	P1DALT	P1CSS		0000 0000
P1AUX	0x1E	–						P1DF2E	P1DF2	---- --00

	Output State at Fault		Notes	
	Ch 0	Ch 1		
PWM1	P1ASS		00 = High impedance; 01 = logic “0” 1x = logic “1”; *logic “0” = 0 if p1xxp = 0* *logic “0” = 1 if p1xxp = 1*	[1] 00 = High impedance; 01 = 0 1x = 1
/PWM1				
PWM2	P1BSS			
PWM3	P1CSS	*P1C2SS*[1]		
PWM4	P1DSS	*P1D2SS*[1]		

Table 10-7 PWM Output State at Fault-Break

10.2 Clock Sources

Timer2 is the dedicated timer for all 4 PWMs. It can choose among 4 clock sources:

- 1x or 4x Instruction Clock
- HIRC
- LIRC

Please see **Section 7.3** Timer2 on how to set it up.

10.3 Period

Timer2 PR2 (PR2H + PR2L) register determine the PWM period, by **Equation 10-1**

Equation 10-1 $PWM\ Period = (PR2 + 1)*T_{T2CK}*(TMR2\ Prescaler\ value)$

When Timer2 counter TMR2 is equal to PR2:

- Timer2 period and duty cycle register (PR2ACT and P1xDTACT) are updated.
- “TMR2 = 0”.
- P1Ax, P1Bx, P1Cx, P1Dx outputs logic High.

10.4 Duty Cycle

Each of the 4 PWM has individual duty cycle as set by corresponding 2 x 8−bit registers (P1xDTH, P1xDTL). P1xDTH is the MSB and the P1xDTL the LSB. P1xDTH and P1xDTL registers can be update at any time because the double buffered design.

The PWM pulse width and duty cycle are calculated by **Equation 10-2** and **Equation 10-3** respectively.

Equation 10-2 $Pulse\ width = P1xDT*T_{T2CK}*(TMR2\ prescaler\ value)$

Equation 10-3 $Duty\ cycle = P1xDT \div (PR2+1)$

10.5 Deadband-Time

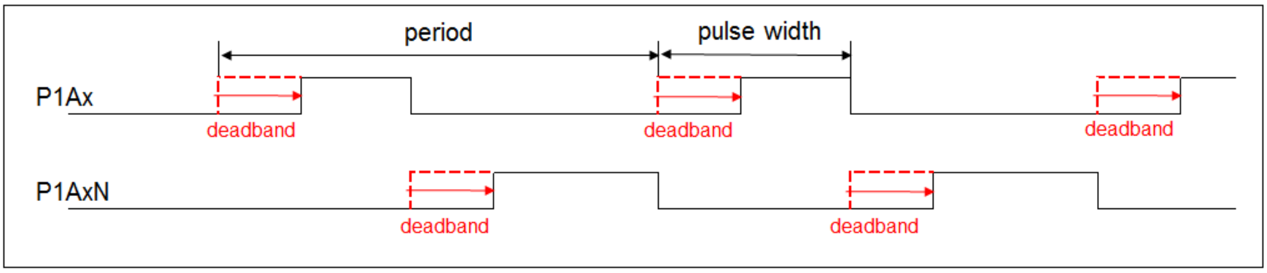


Figure 10-2 PWM dead-time diagram

If P1DC ≠ “00 0000”, P1Ax and P1AxN delay their low to high transition by a "deadband" time. The effective pulse width and duty cycle are also be reduced corresponding. Deadband Timer uses the Timer2 clock.

10.6 Fault-Break Function

All 4 PWMs support Fault-Break function. Upon a Fault-Break event, PWM will output a preset condition according to its setting. The PWM will be in this condition as long as the break condition is valid. TMR2ON is not affected. Fault-Break criteria can be one of the followings:

- BK0 = 0
- BK0 = 1
- LVDW = 1 (LVDDEB enables debouncing filter for LVDW)
- LVDW = 1, BK0 = 0
- LVDW = 1, BK0 = 1

Note: P1BEVT is the Fault-Break status bit. LVDW is not latched and reflects the real time comparison result of LVD.

Output during Fault-Break – During a Fault-Break P1x output can be Input (High Impediance), Logic High or Low. Notice that P1C1, P1D1 Fault-Break output behavior are different from the other I/O.

Clearing a Fault-Break – P1BEVT cannot be cleared by instructions as long as the Fault-Break condition is active. When that condition no longer exists, P1BEVT is cleared by instructions.

Auto-Resume Mode – During a Fault-Break event, the Timer2 is on hold. After the Fault-Break event is over the Timer2 will resume from where it left off. The 4 PWM outputs can be simultaneously configured to Auto-Resume. Otherwise PWM outputs must be resumed by instructions.

10.7 Changing the Period and Duty Cycle

The Period and corresponding Duty Cycle registers can be updated anytime. The changes will not be effective until the beginning of the next period, unless using PR2U to force changes immediately.

Note: PR2 and P1xDTL, P1xDTH is read by instructions, but not the xxxACT register.

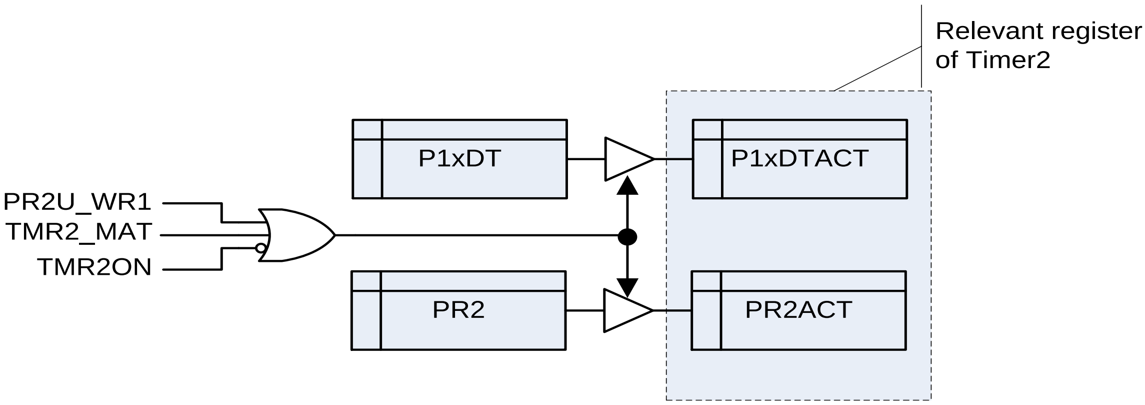


Figure 10-3 Update of Timer2 Register

The double-buffered design of the Period and Duty Cycle registers ensure glitch less PWM operation in most cases. If the registers were updated near the end of a Period (especially if the frequency of Timer2 is faster than SysClk), an unexpected situation might happen and generate an unexpected value in the xxxACT register.

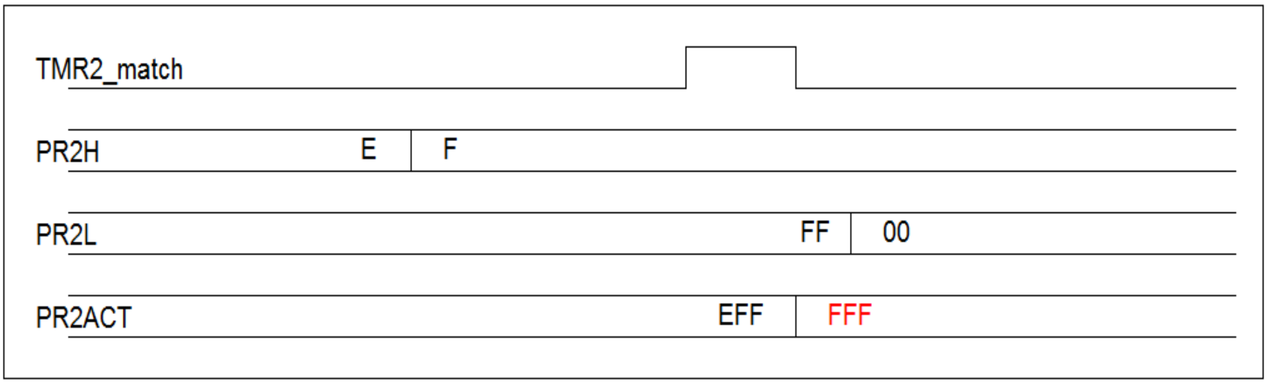


Figure 10-4 PR2ACT updated to FFF (expected value is F00)

It is strongly recommended that PR2 and xxxDTx update right after the beginning of a new period.

10.8 PWM Output

Mapping – The 4 independent duty cycle PWM channels P1A, P1B, P1C, P1D, can be mapped to different I/O. Up to two I/O can be mapped to the PWM3 and 4 channel, and 1 I/O for PWM1 and 2.

Buzzer Mode – The period is (2*(PR2+1)*T_{T2CK} *(TMR2 Prescaler). 50% Duty Cycle square waves for P1A, P1B, P1C and P1D are output.

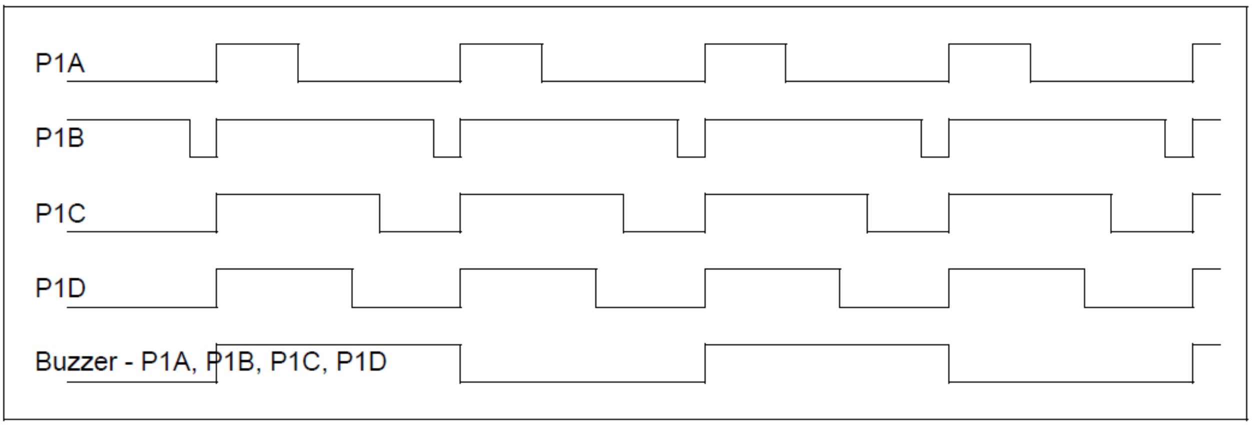


Figure 10-5 Buzzer mode output diagram

One-Pulse Output – P1A, P1B, P1C and P1D will generate a corresponding single pulse only.

Note: Not applicable to [P1C1] and [P1D1].

10.9 Secondary Output Functions of (P1B, P1C)

PA5 = P1B xor P1C (or its complementary, see “P1DF2E” in **Table 10-3**).

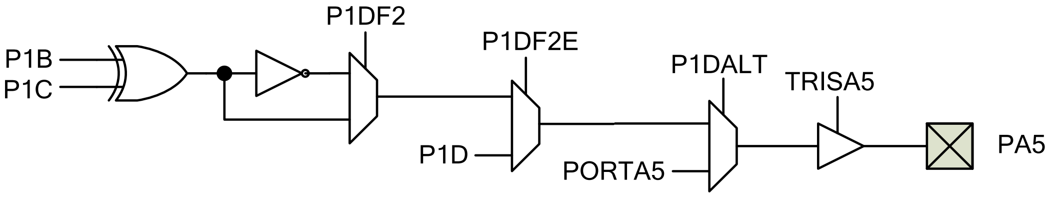


Figure 10-6 Secondary Output Functions Block Diagram

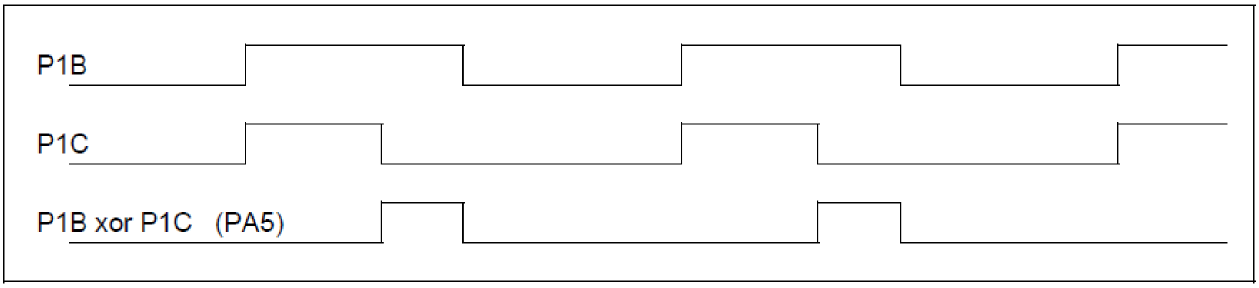


Figure 10-7 Secondary functions of P1B and P1C timing diagram

11. DATA EEPROM

FT60E21x has a 128 x 8−bit non-volatile DATA EEPROM memory array separately from the main program. The array has a typical R/W endurance of 100k cycles. It is R/W accessible by instructions. One byte (8−bit) is written or read. There is no page mode. Erase/program is self-timed, eliminating instruction queries and saving limited code space. This allows WRITE to take place in the background while the CPU runs unhindered, or even to enter SLEEP.

READ takes two instruction clock cycles, whereas WRITE takes $T_{\text{WRITE-EEPROM}}$ (3 ~ 5 ms). There is an on-chip charge pump so there is no need to supply an external high voltage for erase and program. An interrupt flag is set when WRITE finishes.

There is no sequential READ or sequential WRITE. The address must be updated every time.

Any voltage above V_{POR}, which can be as low as 1.5V from die to die and at high temperature, will be able to run the CPU at 8MHz, 4T. The $V_{\text{DD-WRITE}}$ for writing DATA EEPROM is higher. Minimum $V_{\text{DD-WRITE}}$ is 1.9V and 2.2V for Temperature Grade 2 and Grade 1 respectively. Reading DATA EEPROM has no such minimum V_{DD} restriction (see $V_{\text{DD-READ}}$).

11.1 Summary of DATA EEPROM Related Registers

Name	Status	Register	Addr.	Reset
EEDAT	DATA EEPROM data	EEDAT[7:0]	0x9A	RW−0000 0000
EEADR	DATA EEPROM address	EEADR[6:0]	0x9B	RW− 000 0000
WREN3	DATA EEPROM Write Enable (bit 3) 111 = Enables, reset to 000 after finished (others) = Disables	EECON1[5]	0x9C	RW−0
WREN2	DATA EEPROM Write Enable (bit 2)	EECON1[4]		RW−0
WRERR	DATA EEPROM Write Error? 1 = Premature terminated (MCLR or WDT Reset) 0 = No	EECON1[3]		RW−x
WREN1	DATA EEPROM Write Enable (bit 1)	EECON1[2]		RW−0
RD	DATA EEPROM Reading? 1 = Yes (remains for 4 SysClk cycles, then = 0) 0 = No	EECON1[0]		RW−0
WR	DATA EEPROM Write Busy? 1 = Programming (reset to 0 after finished) 0 = Finished	EECON2[0]	0x9D	RW−0

Table 11-1 Instruction Level EEPROM Related Control Registers

Name	Status		Register	Addr.	Reset
GIE	Global Interrupt	1 = Enables (PEIE, EEIE applies) 0 = Global Disables (Wake-Up not affected)	INTCON[7]	0x0B 0x8B	RW−0
PEIE	Master Peripheral Interrupt	1 = Enables (EEIE applies) 0 = Disables (no Wake-Up)	INTCON[6]		RW−0
EEIE	EEPROM program finished Interrupt	1 = Enables 0 = Disables (no Wake-Up)	PIE1[7]	0x8C	RW−0
EEIF	EEPROM program finished Interrupt?	1 = Yes (latched) 0 = No	PIR1[7]	0x0C	RW−0

Table 11-2 EEPROM Interrupt Enable and Status Bits

11.2 Writing DATA EEPROM

1. Set “GIE = 0”;
2. If “GIE = 1”, then repeat (1);
3. Write target address to EEADR;
4. Write target data EEDAT;
5. Set “WREN3, WREN2, WREN1” = “1, 1, 1” and maintain throughout the programming.
6. Must immediate set “WR = 1” to initiate write (otherwise will abort).
7. After programming completed (see $T_{WRITE\text{-}EEPROM}$ for write time), “WR = 0” and “WREN3, WREN2, WREN1” = “0, 0, 0” set automatically;

Program Example:

```
BCR INTCON, GIE
BTSC INTCON, GIE
LJUMP $-2
BANKSEL EEADR
LDWI 55H
STR EEADR                   ; address is 0x55
STR EEDAT                   ; data is 0x55
LDWI 34H
STR EECON1                  ; set WREN3/2/1 at the same time
BSR EECON2, 0               ; start writing
BSR INTCON, GIE             ; set GIE
```

Note:

1. Writing data into a byte involves two steps: a byte erase automatically followed by a byte program.
2. Data EEPROM Read while the array is still in programming will yield an incorrrect result.
3. If any one of WREN3, WREN2 or WREN1 clears before programming is finished, EEIF flag should be

cleared before the next programming.

11.3 Reading DATA EEPROM

Set EEADR register, then initiate read (“RD = 1”). Data will be available in the EEDAT register at the next instruction cycle. The EEDAT will be unchanged until the next READ or WRITE instruction.

The following is an example on how to read the DATA EEPROM:

```
BANKSEL EEADR
LDWI dest_addr
STR EEADR
BSR EECON1, RD
LDR EEDAT, W
```

12. MEMORY READ / PROGRAM PROTECTON

The PROGRAM CODE and DATA EEPROM can be Array Read Protected. These protections selected at the IDE.

Name	Functions	default
CPB	PROM and DROM All Sectors Read Protection	disabled

Table 12-1 BOOT Level Memory Read and/or Program Protection

13. INSTRUCTION SET

Assembly Syntax	Function	Operation	Status
NOP	No operation	None	NONE
SLEEP	Enter SLEEP mode	0 → WDT; Stop OSC	/PF, /TF
CLRWDT	Clear WDT	0 → WDT	/PF, /TF
LJUMP N	Long JUMP Address	N → PC	NONE
LCALL N	Long CALL Subroutine	N → PC; PC + 1 → Stack	NONE
RETI	Return from Interrupt	Stack → PC; 1 → GIE	NONE
RET	Return from Subroutine	Stack → PC	NONE
BCR R, b	Bit Clear	0 → R(b)	NONE
BSR R, b	Bit Set	1 → R(b)	NONE
CLRR R	Clear Register	0 → R	Z
LDR R, d (MOVF)	Load Register to d	R → d	Z
COMR R, d	Complement Register	/R → d	Z
INCR R, d	Increment Register	R + 1 → d	Z
INCRSZ R, d	Increment Register, Skip if 0	R + 1 → d	NONE
DECR R, d	Decrement Register	R − 1 → d	Z
DECRSZ R, d	Decrement Register, Skip if 0	R − 1 → d	NONE
SWAPR R, d	Swap Halves Register	R(0-3)R(4−7) → d	NONE
RRR R, d	Rotate Right Register	R(0) → C; R(n) → R(n−1); C → R(7);	C
RLR R, d	Rotate Left Register	R(7) → C; R(n) → R(n+1); C → R(0);	C
BTSC R, b	Bit Test, Skip if 0	Skip if R(b)=0	NONE
BTSS R, b	Bit Test, Skip if 1	Skip if R(b)=1	NONE
CLRW	Clear Working Register	0 → W	Z
STTMD	Store W to OPTION	W → OPTION	NONE
CTLIO R	Control I/O Direction Register	W → TRISr	NONE
STR R (MOVWF)	Store W to Register	W → R	NONE
ADDWR R, d	Add W and Register	W + R → d	C, HC, Z
SUBWR R, d	Subtract W from Register	R − W → d	C, HC, Z
ANDWR R, d	AND W and Register	R & W → d	Z
IORWR R, d	OR W and Register	W | R → d	Z
XORWR R, d	XOR W and register	W ^ R → d	Z
LDWI I (MOVLW)	Load Immediate to W	I → W	NONE
ANDWI I	AND W and imm	I & W → W	Z
IORWI I	OR W and imm	I | W → W	Z
XORWI I	XOR W and imm	I ^ W → W	Z
ADDWI I	Add imm to W	I + W → W	C, HC, Z
SUBWI I	Subtract W from imm	I − W → W	C, HC, Z
RETW I	Return, Place imm to W	Stack → PC; I → W	NONE

Table 13-1 37 RISC Instruction Commands

Field	Descriptions
R(F)	SFR/SRAM Address
W	Working Register
b	Bit address within the 8−bit Register / RAM
I / Imm (k)	Immediate data
X	Don’t’ care, may be 0 or 1
d	Destination select 1 = Store result in Register / RAM 0 = Store result in W
N	Immediate program address
PC	Program Counter
/PF	Power-Down Flag
/TF	Time-Out Flag
TRISr	SFR TRISr, r can be A
C	Carry bit
HC	Half Carry
Z	Zero Flag

Table 13-2 OpCode Field

Name	Status	Register	Addr.	Reset
Z	Zero Bit: Result of an arithmetic or logic operation is zero? 1 = Yes 0 = No	STATUS[2]	0x03 0x83	RW−x
HC	Half Carry (ADDWR, ADDWI, SUBWI, SUBWR): Digit Carry-Over or Borrow from the 4th low-order bit of the result? 1 = Carry-Over, Yes; Borrow, No 0 = Carry-Over, No; Borrow, Yes	STATUS[1]		RW−x
C	Carry (ADDWR, ADDWI, SUBWI, SUBWR): Digit Carry-Over or Borrow from MSB of the result? 1 = Carry-Over, Yes; Borrow, No 0 = Carry-Over, No; Borrow, Yes	STATUS[0]		RW−x

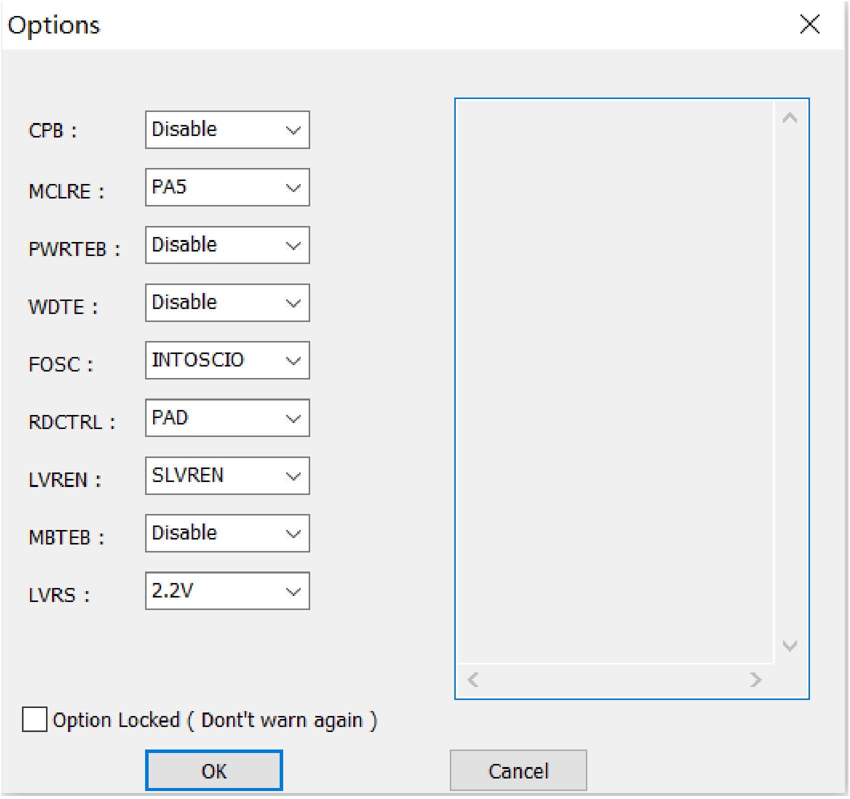
Table 13-3 Computational Status Flags

14. SPECIAL FUNCTION REGISTERS

There are two types of Special Function Registers (SFR).

- BOOT level registers are set at the Integrated Development Environment (IDE);
- Instruction level registers;

14.1 Boot Level Registers



CPB : Disable

MCLRE : PA5

PWRTEB : Disable

WDTE : Disable

FOSC : INTOSCIO

RDCTRL : PAD

LVREN : SLVREN

MBTEB : Disable

LVRS : 2.2V

□ Option Locked (Don't warn again)

Figure 14-1 Boot Selectables in the IDE

Name	Functions	default
CPB	PROM and DROM All Sectors Read Protection	disabled
MCLRE	Reset by External I/O	disabled
PWRTEB	Power-Up Timer (PWRT), Additional ~64ms delay after BOOT load	disabled
WDTE	WDT • Enabled (overrides instructions disable) • Instruction controls (SWDTEN)	SWDTEN control
FOSC	• EC external oscillator at PA3 (CLKI) (Note: set TRISA[3] = 1) • INTOSCIO mode: PA3 as I/O pin	INTOSCIO
RDCTRL	READ register when TRISx = 0 (Output enabled) • Input latch • Output latch	Output
LVREN	LVR • Enabled • Disabled • Instruction controlled (SLVREN)	disabled
MRBTE	BOOT on MCLRE Reset	disabled
LVRS	7 V_{BOR} Voltage levels (V): 2.0 / 2.2 / 2.5 / 2.8 / 3.1 / 3.6 / 4.1	2.5

Table 14-1 Boot Level Registers (selected at IDE)

14.2 Instruction Set Registers

Instruction set Speical Function Registers (SFR) are stored in two banks. The corresponding bank must be selected before the registers inside can be accessed.

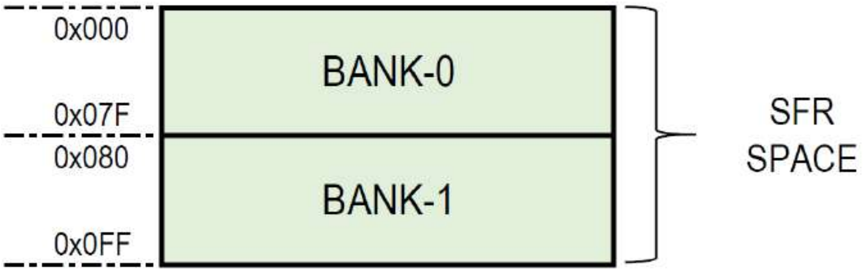


Figure 14-2 Indirect addressing

Since extra instructions are involved in switching BANK, some often-used SFR are stored in all two banks to minimize switching. Registers common to all two BANKS are synchronized.

ADDR	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Reset
0, 80	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
2, 82	PCL	Program Counter's (PC) least Significant Byte								0000 0000
3, 83	STATUS	–	–	PAGE	/TF	/PF	Z	HC	C	0001 1xxx
4, 84	FSR	Indirect Data Memory Address Pointer								xxxx xxxx
A, 8A	PCLATH	–	–	–	Write Buffer for upper 5 bits of Program Counter					−−−0 0000
B, 8B	INTCON	GIE	PEIE	T0IE	INTE	PAIE	T0IF	INTF	PAIF	0000 0000
0x70 − 0x7F 0xF0 − 0xFF	COMMON BANK SRAM									xxxx xxxx

Table 14-2 Registers common to all two banks

ADDR	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	reset
0	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
1	TMR0	Timer0 counter								xxxx xxxx
2	PCL	Program Counter’s (PC) least Significant Byte								0000 0000
3	STATUS	–	–	PAGE	/TF	/PF	Z	HC	C	0001 1xxx
4	FSR	Indirect Data Memory Address Pointer								xxxx xxxx
5	PORTA	–	–	PA5	PA4	PA3	PA2	PA1	PA0	--xx xxxx
6	–	–								–––– ––––
7	–	–								–––– ––––
8	P1DDTL	Least significant byte of P1D duty cycle register								0000 0000
9	P1DDTH	Most significant byte of P1D duty cycle register								0000 0000
A	PCLATH	–	–	–	Write Buffer for upper 5 bits of Program Counter					–––0 0000
B	INTCON	GIE	PEIE	T0IE	INTE	PAIE	T0IF	INTF	PAIF	0000 0000
C	PIR1	EEIF	CKMIF	LVDIF	–	–	–	TMR2IF	–	0000 0000
D	FOSCCAL	–	–	FOSCCAL [5:0]						--xx xxxx
E	P1ADTL	Least significant byte of P1A duty cycle register								0000 0000
F	P1BDTL	Least significant byte of P1B duty cycle register								0000 0000
10	P1CDTL	Least significant byte of P1C duty cycle register								0000 0000
11	TMR2L	TMR2 [7:0], Least significant byte of TMR2								0000 0000
12	T2CON0	PR2U	TOUTPS [3:0]				TMR2ON	T2CKPS [1:0]		0000 0000
13	TMR2H	TMR2 [15:8], Most significant byte of TMR2								0000 0000
14	P1ADTH	Most significant byte of P1A duty cycle register								0000 0000
15	P1BDTH	Most significant byte of P1B duty cycle register								0000 0000
16	P1CON	P1AUE	P1DC [6:0]							0000 0000
17	P1BR0	P1BEVT	P1BKS [2:0]			P1BSS [1:0]		P1ASS [1:0]		0000 0000
18	WDTCON	LVDP	–	WCKSRC	WDTPS [3:0]				SWDTEN	–000 1000
19	P1BR1	P1DSS [1:0]		P1D2SS [1:0]		P1CALT	P1DALT	P1CSS [1:0]		0000 0000
1A	P1CDTH	Most significant byte of P1C duty cycle register								0000 0000
1B	MSCON	–	–	–	–	SLVREN	CKMAVG	CKCNTI	T2CKRUN	–––– 0000
1C	SOSCPRL	SOSCPR [7:0]								1111 1111
1D	SOSCPRH	–	–	–	–	SOSCPR [11:8]				–––– 1111
1E	P1AUX	–	–	–	–	–	–	P1DF2E	P1DF2	–––– ––00
1F	T0CON0	–	–	–	–	T0ON	T0CKRUN	T0CKSRC [1:0]		–––– 1000
20–3F	–									xxxx xxxx
40–7F	SRAM BANK0, (64 Bytes) Physical address 0x40–0x7F									xxxx xxxx

Table 14-3 SFR, BANK 0

ADDR	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	reset
80	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
81	OPTION	/PAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
82	PCL	Program Counter's (PC) least Significant Byte								0000 0000
83	STATUS	−	−	PAGE	/TF	/PF	Z	HC	C	−−01 1xxx
84	FSR	Indirect Data Memory Address Pointer								xxxx xxxx
85	TRISA	−	−	TRISA [5:0]						−−11 1111
86	TKCON	−	TKCHGS[1:0]		TKEN	TKCHE[3:0]				−000 0000
87	−	−								−−−− −−−−
88	PSRCA	−				PSRCA5[1:0]		PSRCA4[1:0]		−−−− 1111
89	−	−								−−−− −−−−
8A	PCLATH	−	−	−	Write Buffer for upper 5 bits of Program Counter					−−−0 0000
8B	INTCON	GIE	PEIE	T0IE	INTE	PAIE	T0IF	INTF	PAIF	0000 0000
8C	PIE1	EEIE	CKMIE	LVDIE	−	−	−	TMR2IE	−	000− −−0−
8D	LVDCON	−					LVDDEB	LVDM[1:0]		−−−− −100
8E	PCON	LVDL [3:0]				LVDEN	LVDW	/POR	/BOR	0000 0xqq
8F	OSCCON	LFMOD	IRCF [2:0]			−	HTS	LTS	−	0101 −00−
90	P1OE	P1COE	P1BOE	P1DOE	−	P1C2SS[1:0]		P1A0NOE	P1A0OE	000− 0000
91	PR2L	PR2 [7:0], Least significant byte of Timer2 period register								1111 1111
92	PR2H	PR2[15:8], Most significant byte of Timer2 period register								1111 1111
93	−	−								−−−− −−−−
94	−	−								−−−− −−−−
95	WPUA	−	−	WPUA [5:0]						−−11 1111
96	IOCA	−	−	IOCA [5:0]						−−00 0000
97	PSINKA	−	−	−	−	−	−	PSINKA [1:0]		−−−− −−00
98	SCKCFG	SCKEN	−	−	−	−	−	SCKOE	−	0−−− −−0−
99	P1POL	P1CP	P1BP	P1DP	−	−	−	P1A0NP	P1A0P	000− −−00
9A	EEDAT	EEDAT [7:0]								0000 0000
9B	EEADR	−	EEADR [6:0]							−000 0000
9C	EECON1	−	−	WREN3	WREN2	WRERR	WREN1	−	RD	−−00 x0−0
9D	EECON2	−	−	−	−	−	−	−	WR	−−−− −−−0
9E	T2CON1	−	−	−	P1OS	P1BZM	T2CKSRC [2:0]			−−−0 0000
9F	−	−								−−−− −−−−
A0–EF	−									xxxx xxxx
F0–FF	SRAM, address BANK0's 0x70–0x7F									xxxx xxxx

Table 14-4 SFR, BANK 1

Notes:

1. INDF is not a physical register;
2. Gray parts indicate not used;
3. Do not write the unused register bits.

14.3 STATUS Register

Name	Status	Register	Addr.	Reset
PAGE	Register Bank Select 0 = Bank 0 (0x00h – 0x7Fh) 1 = Bank 1 (0x80h – 0xFFh)	STATUS[5]	0x03 0x83	RW−0
/TF	Time-out? 1 = CLRWDT or SLEEP instruction after Power-up 0 = WDT time-out occurred	STATUS[4]		RO−1
/PF	Power-down? 1 = After power-up or by the CLRWDT instruction 0 = By execution of the SLEEP instruction	STATUS[3]		RO−1
Z	Zero: Result of an arithmetic or logic operation is zero? 1 = Yes 0 = No	STATUS[2]		RW−x
HC	Half Carry: Digit Carry-Over or Borrow from the 4th low-order bit of the result? 1 = Carry-Over, Yes; Borrow, No 0 = Carry-Over, No; Borrow, Yes	STATUS[1]		RW−x
C	Carry: Digit Carry-Over or Borrow from MSB of the result? 1 = Carry-Over, Yes; Borrow, No 0 = Carry-Over, No; Borrow, Yes	STATUS[0]		RW−x

Table 14-5 Status Register

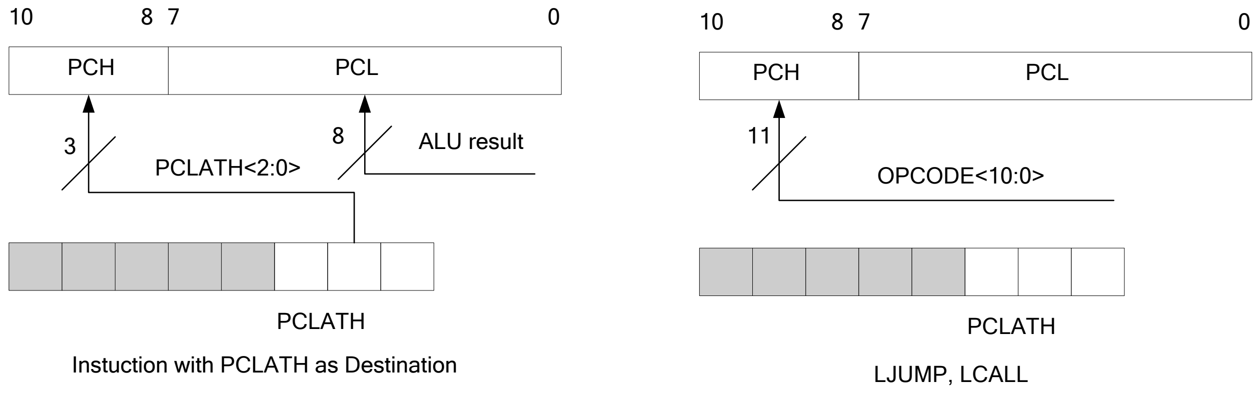
Notes:

1. The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, HC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.
2. It is recommended, therefore, that only BCR, BSR, SWAPR and STR instructions are used to alter the STATUS register.

14.4 PCL and PCLATH

The program array has only one Page (1kW). At the end of the Page (0x3FF) it will roll over to the beginning of Page (0x000). The address width of a command is 11 bits, and can address 2kW. For LJUMP and LCALL commands that jump from one page to another, no need to set PCLATH.

The Program Counter (PC) is 11 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte PC[10:8] is not directly readable or writable and comes from PCLATH. On any Reset, PC clears. **Figure 14-3** shows the two situations for the loading of the PC.



Instuction with PCLATH as Destination

LJUMP, LCALL

Figure 14-3 Loading of PC in different situations

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC[10:8] bits to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by first writing the desired upper 3 bits to the PCLATH register

A computed JUMP is accomplished by adding an offset to the program counter (ADDWR PCL). Care should be exercised when jumping into a look-up table or program branch table (computed JUMP) by modifying the PCL register. Assuming that PCLATH is set to the table start address, if the table length is greater than 255 instructions or if the lower 8 bits of the memory address rolls over from 0xFF to 0x00 in the middle of the table, then PCLATH must be incremented for each address rollover that occurs between the table beginning and the target location within the table .

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 0x000. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected).

15. ELECTRICAL SPECIFICATIONS

15.1 Absolute Maximum Ratings

Operation temperature Grade…………….………………………………………...………..	$^{-}$40 – $^{+}$ 85°C
Storage temperature…………………………..…………………….….……………….…..	$^{-}$40 – $^{+}$125°C
Junction operation temperature (Tj) …………..……………………..….……………….…..	$^{-}$40 – $^{+}$150°C
Power supply voltage…………………...…………………………...……………….	V_{SS}-0.3V – V_{SS}+6.0V
PAD input voltage………………………...……………………..…………...………	V_{SS}-0.3V – V_{DD}+0.3V

Notes:

1. Stresses above "Absolute Maximum Ratings" may cause permanent damages to the device.
2. All characterizations are at 25°C, V_{DD} =1.9 – 5.5V unless otherwise stated.
3. Values and ranges indicated are from characterizations, and are not indicative of the final shipping criteria.
4. Prodution test are at 25°C unless otherwise stated. Performance at temperature outside of above operation temperature are not guaranteed as high temperature screening is not part of normal production procedure.
5. Typical unstressed memory data retention @ 150° C > 10 years.

15.2 Operation Characteristics

Parameters		Min	Typical	Max	Units	Conditions
Fsys (SysClk)	4T	–	–	8	MHz	-40 – 85°C, V_{DD} = 1.9 – 5.5V
		–	–	16	MHz	-40 – 85°C, V_{DD} = 2.5 – 5.5V
Instruction Period ($T_{INSTRCLK}$)	4T	–	250	–	ns	SysClk = HIRC
	4T	–	122	–	μs	SysClk = LIRC
T0CKI High or Low Pulse Width		0.5 * T_{T0CK} + 20	–	–	ns	no Prescaler
		10	–	–	ns	with Prescaler
T0CKI Input Period		Max. 20 and (T_{T0CK}+40)/N	–	–	ns	N = 1, 2, 4, …, 256 (Prescaler)
Power-On-Reset hold time (T_{DRH})		–	8	–	ms	25°C, PWRT disable
Ext. Reset pulse width (T_{MCLRB})		2000	–	–	ns	25°C
WDT period (T_{WDT})		–	1	–	ms	Prescaler = 1:32

Note: T_{T0CK} is the period dictated by T0CKSRC.

15.3 POR, LVR, LVD

Power-On-Reset (POR)

Parameters	Min	Typical	Max	Units	Conditions
I_{POR} Operating Current	–	0.14	–	µA	25°C , V_{DD} = 3.3V
V_{POR}	–	1.65	–	V	25°C

Low Voltage Reset (LVR)

Parameters	Min	Typical	Max	Units	Conditions
I_{LVR} Operating Current	–	17.3	–	µA	25°C, V_{DD} = 3.3V
V_{LVR}, LVR threshold	1.94	2.0	2.06	V	25°C
	2.13	2.2	2.27		
	2.42	2.5	2.58		
	2.72	2.8	2.88		
	3.01	3.1	3.19		
	3.49	3.6	3.71		
	3.98	4.1	4.22		
LVR delay	94	–	125	µs	25°C, V_{DD} = 1.9 – 5.5V

Low Voltage Detect (LVD)

Parameters	Min	Typical	Max	Units	Conditions
I_{LVD} Operating Current	–	21.4	–	µA	25°C, V_{DD} = 3.3V
V_{LVD}, LVD threshold	1.16	1.2	1.24	V	25°C
	1.75	1.8	1.85		
	1.94	2.0	2.06		
	2.33	2.4	2.47		
	2.62	2.7	2.78		
	2.91	3.0	3.09		
	3.20	3.3	3.40		
	3.49	3.6	3.71		
	3.88	4.0	4.12		
LVD delay	94	–	125	ns	25°C, V_{DD} = 1.9 – 5.5V

15.4 I/O PORTS

Parameters			Min	Typical	Max	Units	Conditions
V_{IL}			0	–	0.3* V_{DD}	V	
V_{IH}			0.7* V_{DD}	–	V_{DD}	V	
Leakage current			-1	–	1	μA	V_{DD} = 5V
Source current	PA4–5	L0	–	-3	–	mA	25°C, V_{DD} = 5V, V_{OH} = 4.5V
	PA4–5	L1	–	-6	–		
	PA0–3	L2	–	-18	–		
	PA4–5	L3	–	-24	–		
Sink Current	PA0–5	L0	–	53	–	mA	25°C, V_{DD} = 5V, V_{OL}= 0.5V
		L1	–	67	–		
Pull-up resistance			–	20	–	kΩ	–

15.5 Operation Current (I_{DD})

Parameters	SysClk	Typical @V_{DD}			Units
		2.0V	3.0V	5.5V	
Normal mode (4T) - I_{DD}	16 MHz	–	0.519	0.542	mA
	8 MHz	0.266	0.390	0.405	
	4 MHz	0.222	0.324	0.336	
	2 MHz	0.201	0.290	0.300	
	1 MHz	0.190	0.274	0.284	
	32 kHz	0.117	0.175	0.182	
Sleep Mode (~~WDT OFF~~, ~~LVR OFF~~), I_{SB}	–	0.077	0.099	0.112	μA
Sleep Mode (WDT ON, ~~LVR OFF~~)	32 kHz	1.163	2.464	2.574	
Sleep Mode (~~WDT OFF~~, LVR ON)	–	12.116	17.318	22.299	
Sleep Mode (WDT ON, LVR ON)	32 kHz	13.094	19.494	24.505	
Sleep Mode (~~WDT OFF~~, ~~LVR OFF~~, LVD ON)	–	18.454	21.402	24.840	

Note: Sleep mode I_{SB} is measured with all I/O in input mode and external pull-down to GND.

15.6 Internal Oscillators

Internal Low Frequency Oscillator (LIRC)

LIRC is set at 32 kHz during measurement (LFMOD=0).

Parameters	Min	Typical	Max	Units	Conditions
Range	30.4	32	33.6	kHz	25°C, V_{DD} = 2.5V
temperature dependence	-2.0%	−	2.0%	−	-40 – 85°C, V_{DD} = 2.5V
supply voltage variation	-3.5%	−	2.0%	−	25°C, V_{DD} = 1.9 – 5.5V
I_{LIRC} Operating Current	−	2.0	−	µA	25°C, V_{DD} = 3.0V
Start up Time	−	4.6	−	µs	25°C, V_{DD} = 3.0V

Internal High Frequency Oscillator (HIRC)

Parameters	Min	Typical	Max	Units	Conditions
Range	15.76	16	16.24	MHz	25°C, V_{DD} = 2.5V
temperature dependence	-8.5%	±4.0%	6.5%	−	-40 – 85°C, V_{DD} = 2.5V
supply voltage variation	-1.0%	−	1.0%	−	25°C, V_{DD} = 1.9 – 5.5V
I_{HIRC} Operating Current	−	51	−	µA	25°C, V_{DD} = 3.0V
Start up time	−	2.5	−	µs	25°C, V_{DD} = 3.0V

15.7 Program and Data EEPROM

Parameters		Min	Typical	Max	Units	Conditions
$V_{DD\text{-}READ}$	Program/Data EE read voltage	V_{POR}	–	5.5	V	-40 ~ 85°C
$V_{DD\text{-}WRITE}$	Program EE write voltage	2.5	–	5.5	V	-40 ~ 85°C
	Data EE write voltage	1.9	–	5.5		
N_{END}	Program EE erase/write cycles	100 k	–	–	cycle	25 °C
		40 k	–	–		85 °C
	Data EE erase/write cycles	100 k	–	–		25 °C
		40 k	–	–		85 °C
T_{RET}	Program EE data retention	20	–	–	year	after 1k cycles @ 85 °C
	Data EE data retention	20	–	–		after 10k cycles @ 85 °C
T_{WRITE}	Data EE write time	–	4.0	–	ms	–
I_{PROG}	Data EE programming current	–	300	–	μA	25 °C, V_{DD} = 3 V

15.8 EMC characteristics

ESD

Parameters		Min	Typical	Max	Units	Conditions
V_{ESD}	HBM	4000	–	–	V	MIL-STD-883H Method 3015.8
V_{ESD}	MM	200	–	–	V	JESD22-A115

Latch-up

Parameters	Min	Typical	Max	Units	Conditions
LU, static latch-up	200	–	–	mA	EIA/JESD 78

EFT

Parameters	Min	Typical	Max	Units	Conditions
V_{EFT}	5.5	–	–	kV	1μF Cap applied on V_{DD} (5V)

Note: EMC tests are performed at 25°C unless otherwise stated.

16. Characterization Graphs

Note: The characterization graphs are for reference only, not guaranteed by production test.

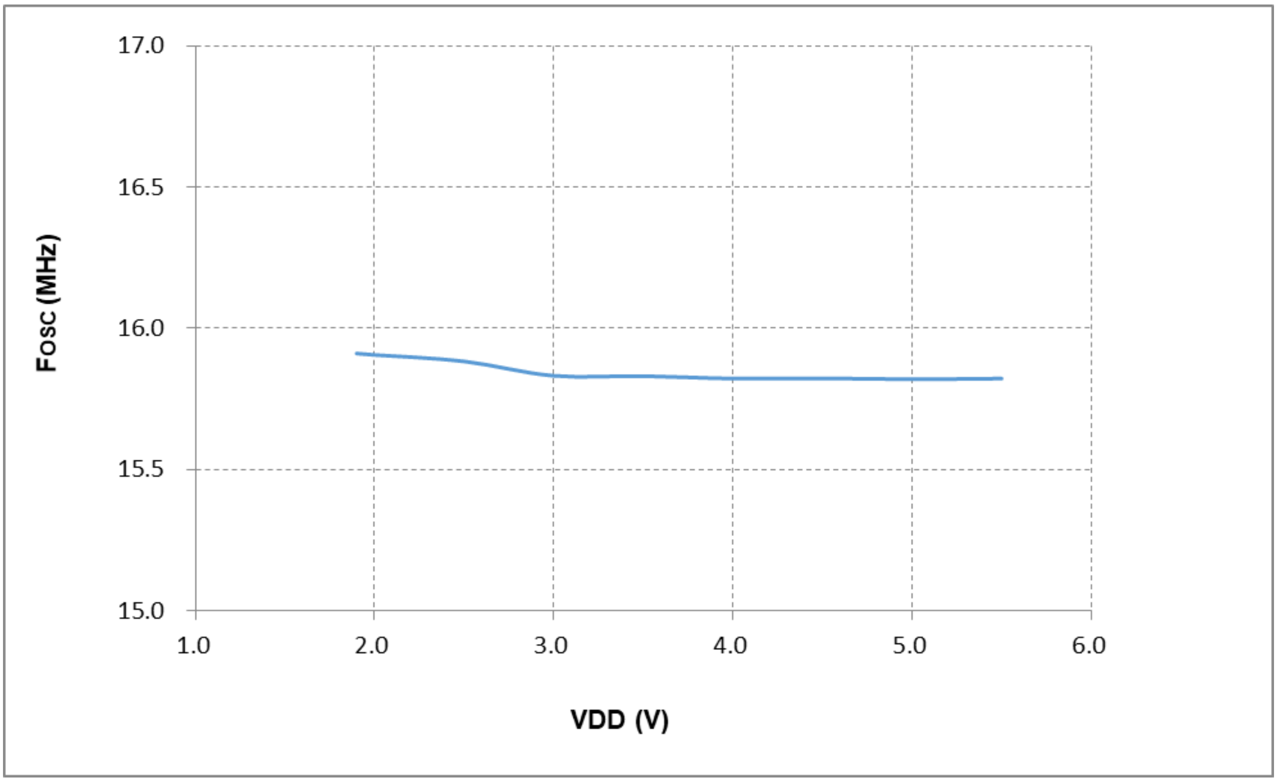


Figure 16-1 HIRC vs. V_{DD} (T_A = 25°C)

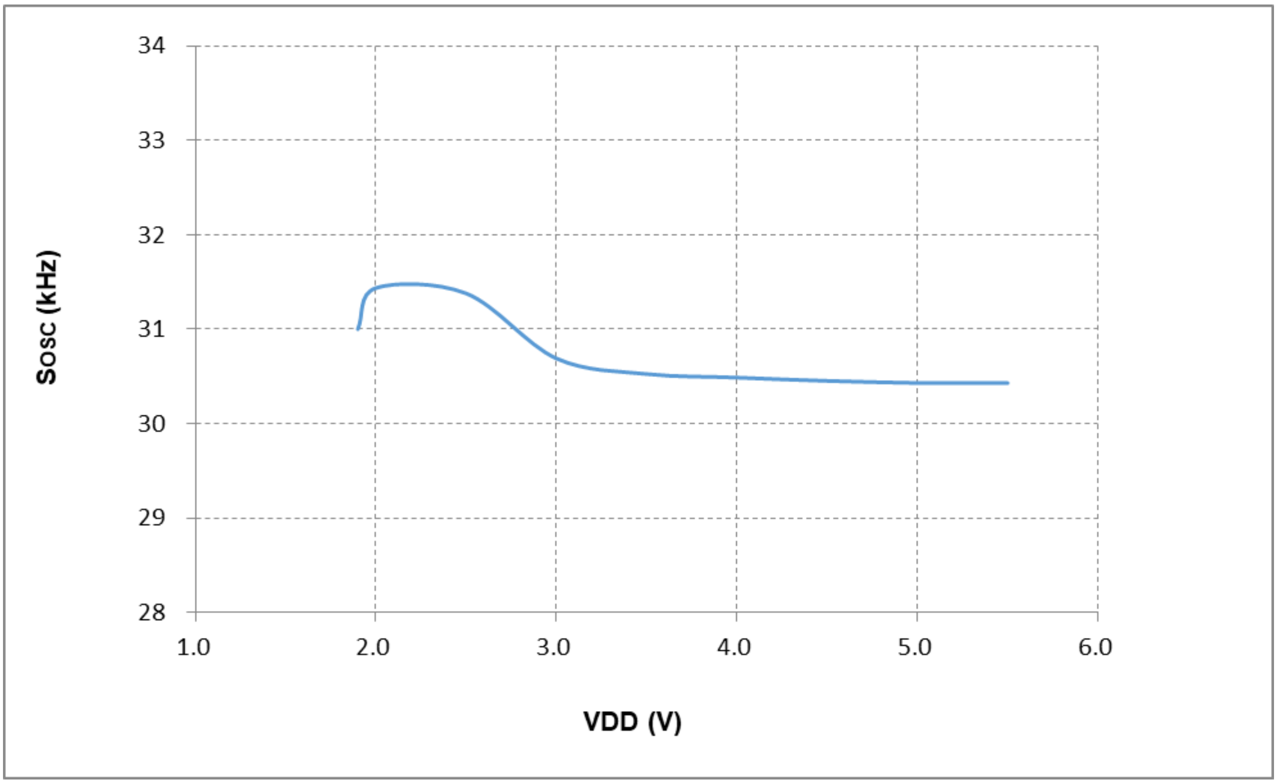


Figure 16-2 LIRC vs. V_{DD} (T_A = 25°C)

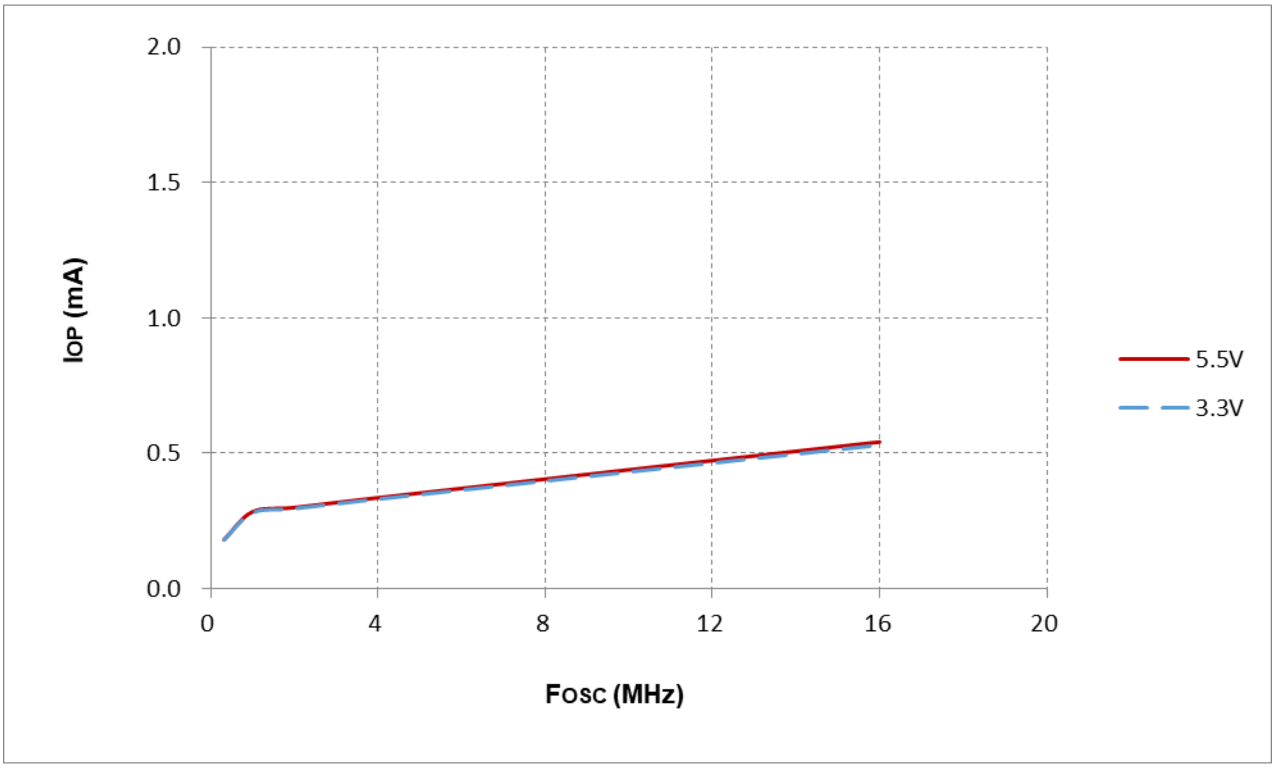


Figure 16-3 I_{DD} vs. Frequency (4T, T_A = 25°C)

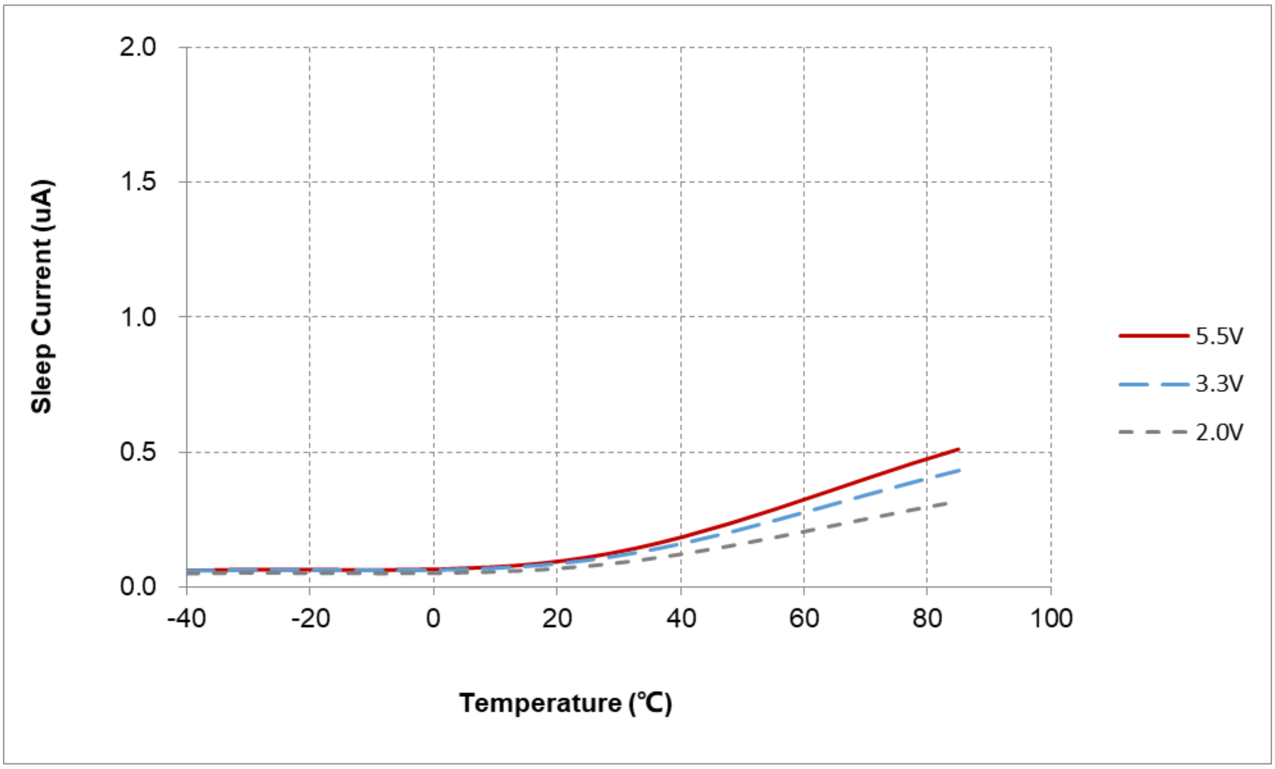


Figure 16-4 Sleep Current (I_{SB}) vs. Temperature

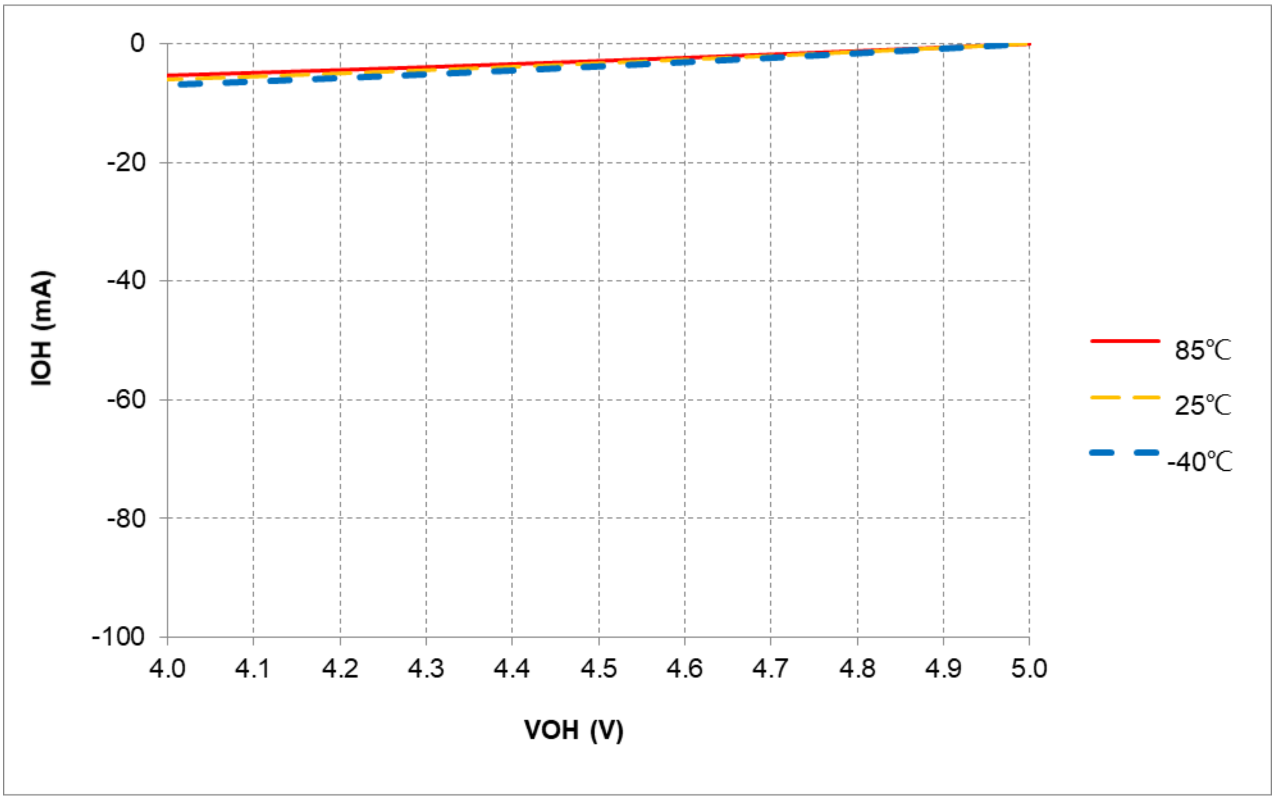


Figure 16-5 I_{OH} vs. V_{OH} @L0 = -3mA, V_{DD} = 5V

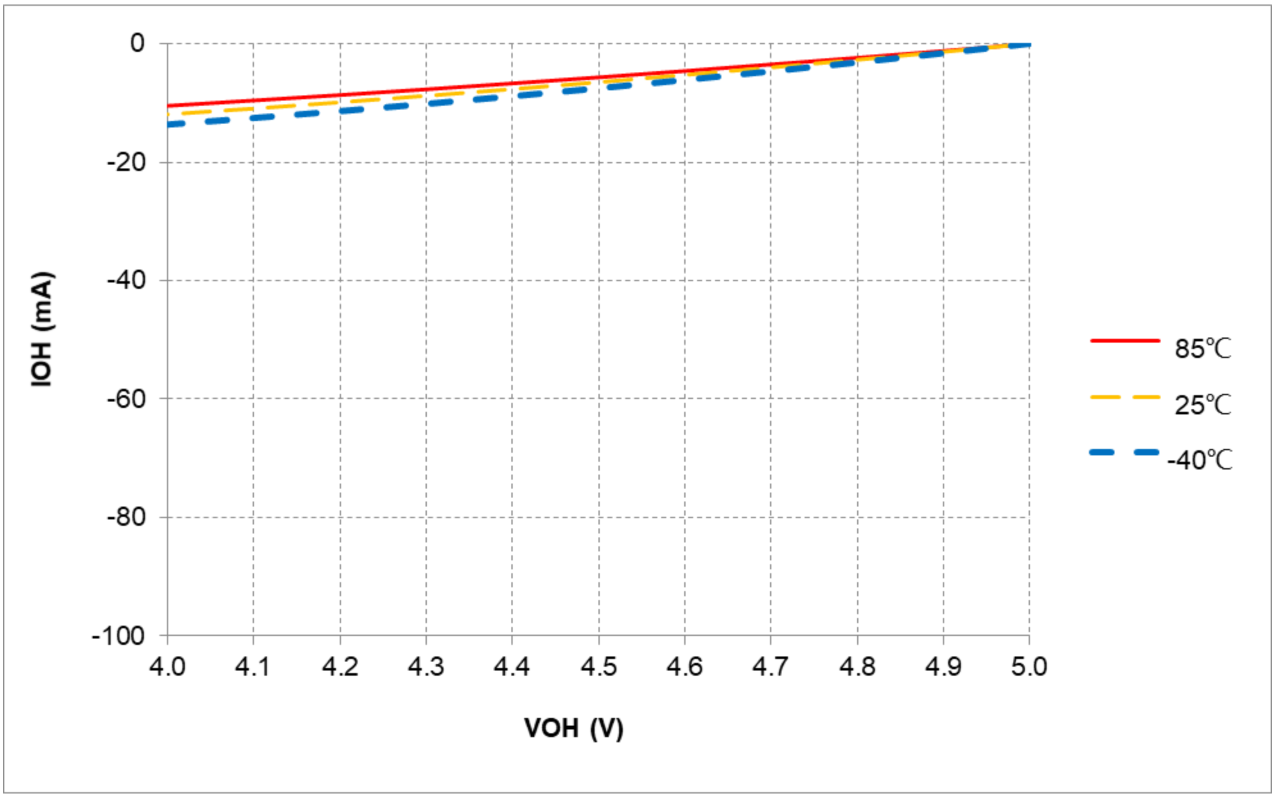


Figure 16-6 I_{OH} vs. V_{OH} @L1 = -6mA, V_{DD} = 5V

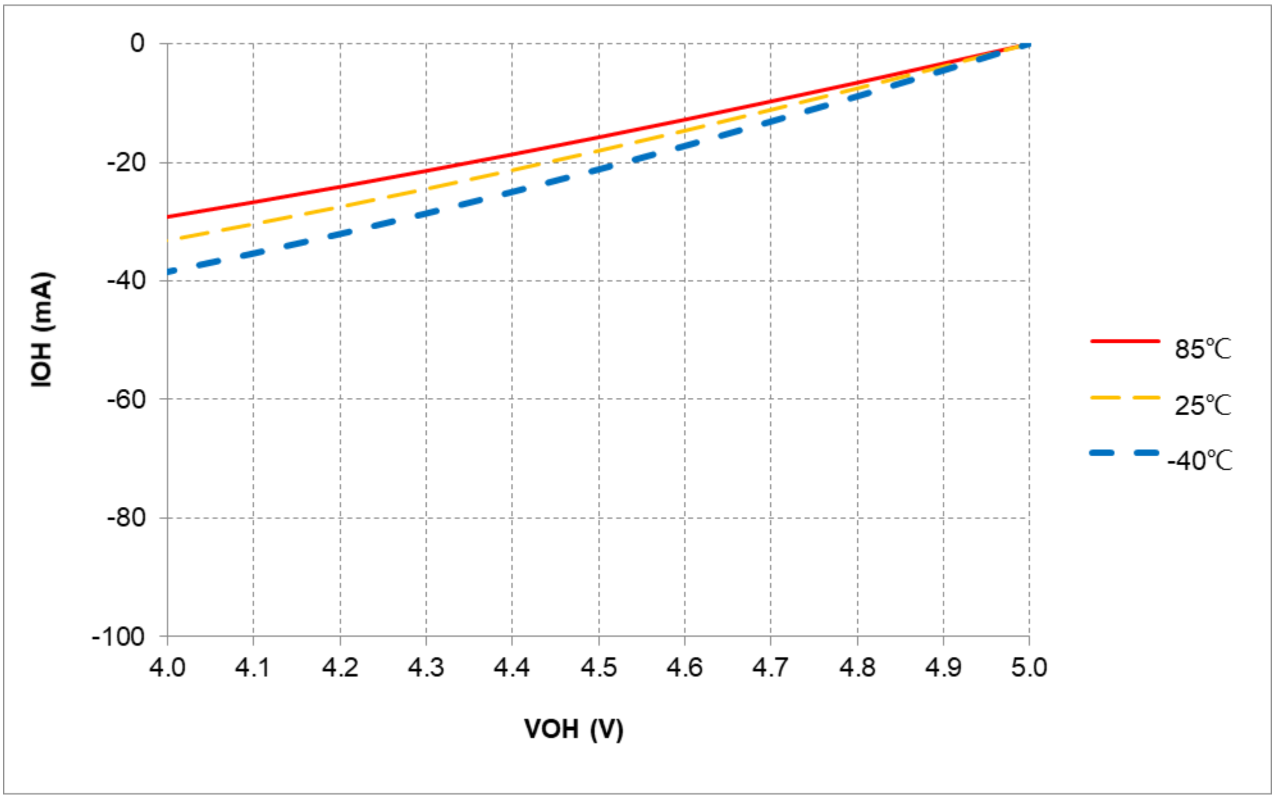


Figure 16-7 I_{OH} vs. V_{OH} @L2 = -18mA, V_{DD} = 5V

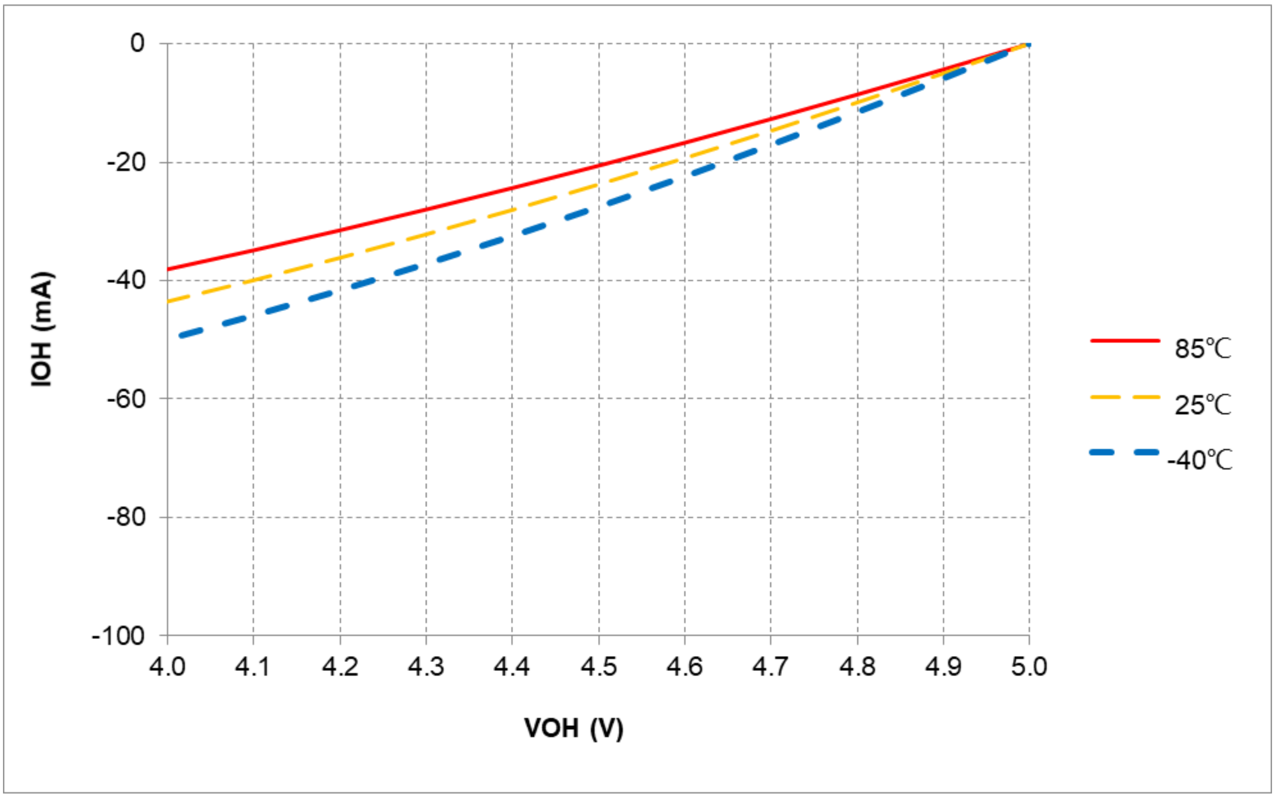


Figure 16-8 I_{OH} vs. V_{OH} @L3 = -24mA, V_{DD} = 5V

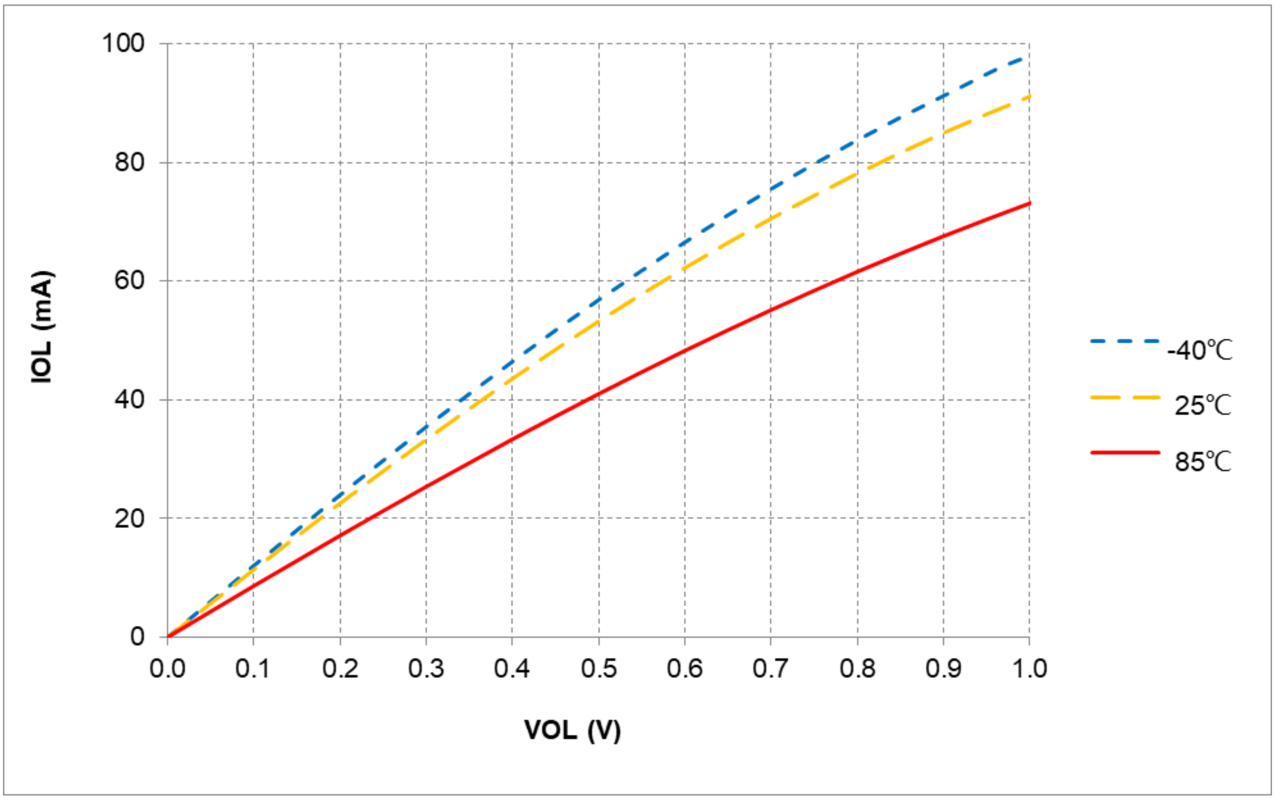


Figure 16-9 I_{OL} vs. V_{OL} @L0 = 53mA, V_{DD} = 5V

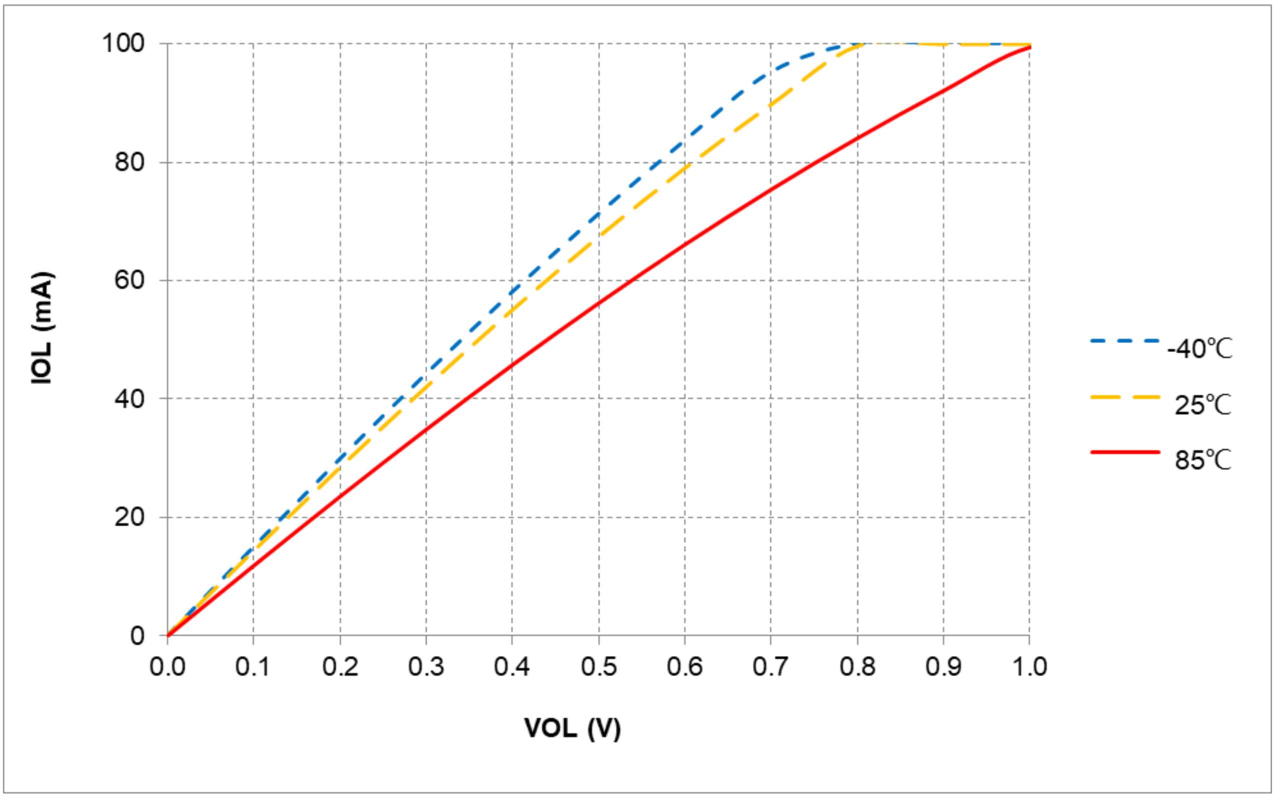
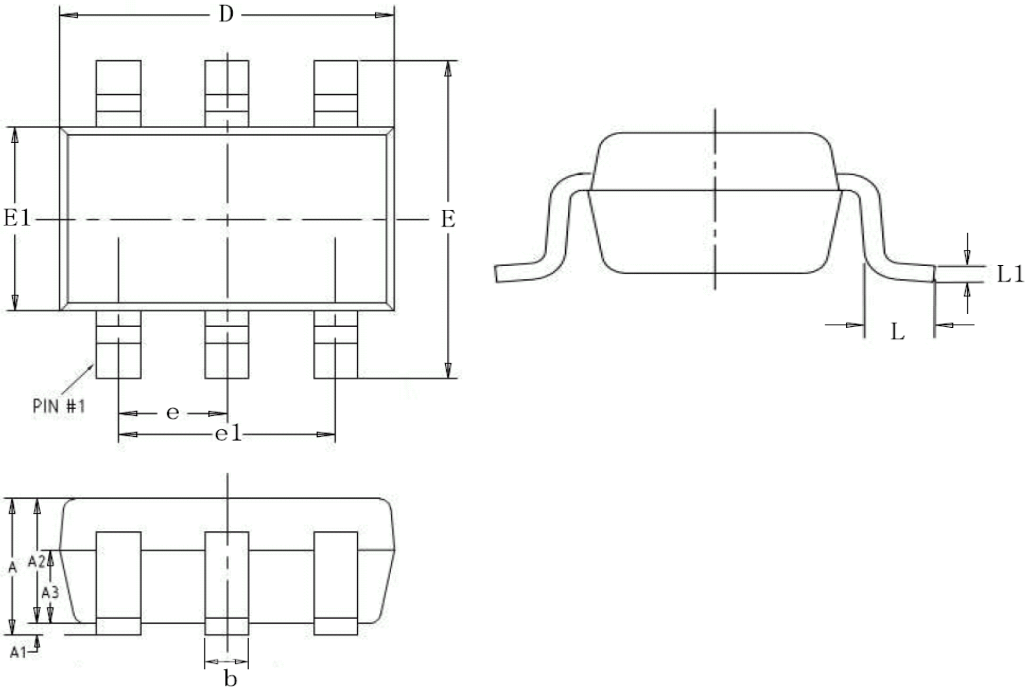


Figure 16-10 I_{OL} vs. V_{OL} @L1 = 67mA, V_{DD} = 5V

17. PACKAGING INFORMATION

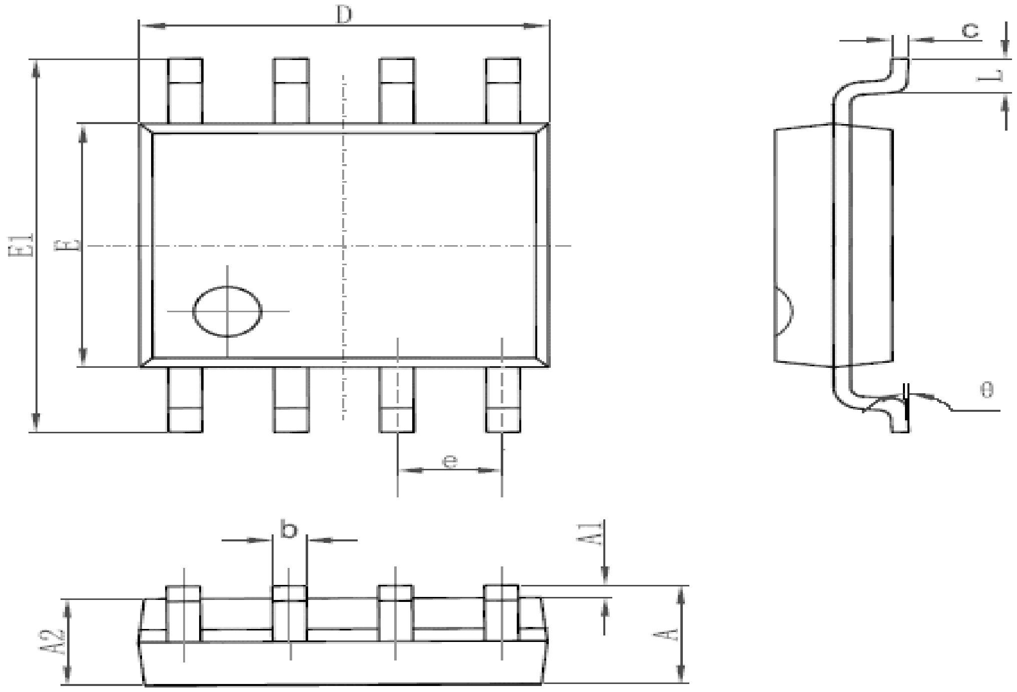
The device is available in SOT23-6 and SOP8 packages. The specific package size information is shown below:

SOT23-6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	—	1.300	—	0.051
A1	0.040	0.100	0.002	0.004
A2	1.050	1.150	0.041	0.045
A3	0.600	0.700	0.024	0.028
e	0.920	0.980	0.036	0.039
e1	1.850	1.950	0.073	0.077
b	0.350	0.450	0.014	0.018
D	2.820	2.920	0.111	0.115
E	2.650	2.950	0.104	0.116
E1	1.550	1.650	0.061	0.065
L	0.400	0.500	0.016	0.020
L1	0.25BSC		0.010BSC	

SOP8



Symbol	Dimensions (mm)		Dimensions (inches)	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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