HT32F54231/HT32F54241
HT32F54243/HT32F54253
Datasheet

32-Bit Arm® Cortex®-M0+ 5V Touch Microcontroller,
up to 128 KB Flash and 16 KB SRAM with 1 Msps ADC,
Touch Key, DIV, CMP, USART, UART, SPI, I²C, GPTM, SCTM,
BFTM, MCTM, PDMA, LED Controller, CRC, RTC and WDT

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1 General Description

The Holtek HT32F54231/HT32F54241/HT32F54243/HT32F54253 devices are high performance, low power consumption 32-bit microcontrollers based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer and including advanced debug support.

The devices operate at a frequency of up to 60 MHz with a Flash accelerator to obtain maximum efficiency. It provides up to 128 KB of embedded Flash memory for code / data storage and up to 16 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as Hardware Divider DIV, PDMA, ADC, I^2C, USART, UART, SPI, GPTM, SCTM, BFTM, MCTM, CRC-16/32, RTC, WDT, Touch key, LED controller and SW-DP (Serial Wire Debug Port), etc., are also implemented in the device series. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the devices are suitable for use in a wide range of applications, especially in areas such as washing machines, refrigerators, electric pressure cookers, high-speed blenders, rice cookers and so on.

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 60 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O ports, hardware multiplier and low latency interrupt respond time.

On-Chip Memory

- Up to 128 KB on-chip Flash memory for instruction/data and option byte storage
- Up to 16 KB on-chip SRAM
- Supports multiple booting modes

The Arm® Cortex®-M0+ processor access and debug access share the single external interface to external AHB peripherals. The processor access takes priority over debug accesses. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 3 ~ 4 in the Overview chapter shows the memory map of the HT32F54231/HT32F54241/HT32F54243/HT32F54253 series devices, including code, SRAM, peripheral and other pre-defined regions.

Flash Memory Controller – FMC

- Flash accelerator for maximum efficiency
- 32-bit word programming with In System Programming (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer is provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor
  - Power On Reset / Power Down Reset – POR / PDR
  - Brown Out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by external signals, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- External 32,768 Hz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to ±2 % accuracy at 5 V operating voltage and 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Integrated system clock PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control Unit, CKCU, provides a range of oscillators and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), an HSE clock monitor, clock pre-scalers, clock multiplexers, APB clock divider and gating circuitry. The clocks of the AHB, APB and Cortex®-M0+ are derived from the system clock (CK_SYS) which can source from the HSI, HSE, LSI, LSE or system PLL. The Watchdog Timer and Real-Time Clock (RTC) use either the LSI or LSE as their clock source.

Power Management Control Unit – PWRCU

- Single V_{DD} power supply: 2.5 V to 5.5 V
- Integrated 1.5 V LDO regulator for MCU core, peripherals and memories power supply
- V_{DD} power supply for RTC
- Two power domains: V_{DD} and V_{CORE}
- Three power saving modes: Sleep, Deep-Sleep1 and Deep-Sleep2

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in the devices provide many types of power saving modes such as Sleep, Deep-Sleep1 and Deep-Sleep2 modes. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger sources and types
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edges
- Individual interrupt enable, wake-up enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt / Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 10 external analog input channels

A 12-bit multi-channel Analog to Digital Converter is integrated in the devices. There are multiplexed channels, which include up to 10 external analog signal channels and 3 internal channels. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset threshold levels. There are three conversion modes to convert an analog signal to digital data. The A/D Conversion can be operated in one shot, continuous and discontinuous conversion modes.

Comparator – CMP (HT32F54243/HT32F54253 only)

- Rail-to-rail comparator
- Each comparator has configurable negative input used for flexible voltage selection
  - External CNn pin
  - Internal 8-bit CVR output
- Programmable hysteresis
- Programmable respond speed and consumption
- Comparator output can be routed to I/O or to multiple timers or ADC trigger inputs
- 8-bit scaler can be configured to dedicated I/O for voltage reference
- Comparator has interrupt generation capability with wakeup from Sleep, Deep Sleep1 or Deep Sleep2 mode through the EXTI controller

The two general purpose comparators, CMP, are implemented within the devices. They can be configured either as standalone comparators or combined with the different kinds of peripheral IP. Each comparator is capable of asserting interrupts to the NVIC or waking up the MCU from the Sleep or Deep Sleep1 mode through the EXTI wakeup event management unit.

I/O Ports – GPIO

- Up to 54 GPIOs
- Port A, B, C, D are mapped as 16 external interrupts – EXTI
- Almost all I/O pins have a configurable output driving current

There are up to 54 General Purpose I/O pins, GPIO, for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

Motor Control Timer – MCTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Supports 3-phase motor control and hall sensor interface
- Break input to force the timer's output signals into a reset or fixed condition

The Motor Control Timer Module, MCTM, consists of one 16-bit up/down counter; four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR), one 8-bit repetition counter and several control/status registers. It can be used for a variety of purposes including measuring the pulse widths of input signals or generating output waveforms such as compare match outputs, PWM outputs or complementary PWM outputs with dead-time insertion. The MCTM is capable of offering full functional support for motor control, hall sensor interfacing and brake input.

General-Purpose Timer – GPTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General-Purpose Timer Module, GPTM, consists of one 16-bit up/down-counter, four 16-bit Capture / Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control / status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

Single-Channel Timer – SCTM

- 16-bit up auto-reload counter
- One channel for each timer
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned

The Single Channel Timer Module, SCTM, consists of one 16-bit up-counter, one 16-bit Capture / Compare Register (CCR), one 16-bit Counter Reload Register (CRR) and several control / status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as PWM output.

Basic Function Timer – BFTM

- 32-bit compare match count-up counter – no I/O control
- One shot mode – counter stops counting when compare match occurs
- Repetitive mode – counter restarts when compare match occurs

The Basic Function Timer Module, BFTM, is a simple count-up 32-bit counter designed to measure time intervals and generate a one shot or repetitive interrupts. The BFTM operates in two functional modes, repetitive or one shot mode. In the repetitive mode the BFTM restarts the counter when a compare match event occurs. The BFTM also supports a one shot mode which forces the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-bit count-down counter with 3-bit prescaler
- Provides reset to the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect system failures due to software malfunctions. It includes a 12-bit count-down counter, a prescaler, a WDT delta value register, a WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter when the counter value is greater than the WDT delta value. This means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. There is a register write protect function which can be enabled to prevent it from changing the Watchdog Timer configuration unexpectedly.

Real-Time Clock – RTC

- 24-bit count-up counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real-Time Clock, RTC, includes an APB interface, a 24-bit count-up counter, a control register, a prescaler, a compare register and a status register. The RTC counter is used as a wake-up timer to generate a system resume signal from the power saving modes.

Inter-Integrated Circuit – I²C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode using address mask function

The I²C is an internal circuit allowing communication with an external I²C interface which is an industry standard two-line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I²C bus is a bi-directional data line between the master and slave devices and is used for data transmission and reception. The I²C also has an arbitration detection and clock synchronization function to prevent situations where more than one master attempts to transmit data to the I²C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave modes
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, which are the serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Programmable baud rate clock frequency up to (f_{PCLK}/16) MHz for asynchronous mode and (f_{PCLK}/8) MHz for synchronous mode
- Capability of full duplex communication
- Fully programmable serial communication characteristics including
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8-level for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous data transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes a transmitter FIFO, TX FIFO, and receiver FIFO, RX FIFO. The software can detect a USART error status by reading the USART Status

& Interrupt Flag Register, USRSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud rate clock frequency of up to f_{PCLK}/16 MHz
- Capability of full duplex communication
- Fully programmable serial communication characteristics including
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Cyclic Redundancy Check – CRC

- Supports CRC16 polynomial: 0x8005,
  $X^{16} + X^{15} + X^{2} + 1$
- Supports CCITT CRC16 polynomial: 0x1021,
  $X^{16} + X^{12} + X^{5} + 1$
- Supports IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
  $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^{8} + X^{7} + X^{5} + X^{4} + X^{2} + X + 1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- The HT32F54243/HT32F54253 device support PDMA to complete a CRC computation of a block of memory

The CRC calculation unit is an error detection technique test algorithm and is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means the data stream contains a data error.

Peripheral Direct Memory Access – PDMA (HT32F54243/HT32F54253 only)

- 6 channels with trigger source grouping
- 8-bit, 16-bit and 32-bit width data transfer
- Supports Address increment, decrement and fixed modes
- 4-level programmable channel priority
- Auto reload mode
- Supports trigger source
  ADC, SPI, USART, UART, I^{2}C, MCTM, GPTM and software request

The Peripheral Direct Memory Access controller, PDMA, moves data between the peripherals and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt service routine execution. It improves system performance as the software does not need to connect each data movement operation.

Hardware Divider – DIV

- Signed/unsigned 32-bit divider
- Calculate in 8 clock cycles, load in 1 clock cycle
- Division by zero error flag

The divider is the truncated division and needs a software triggered start signal by using the control register “START” bit. After 8 clock cycles, the divider calculate complete flag will be set to 1, and if the divisor register data is zero, the division by zero error flag will be set to 1.

LED Controller – LEDC

- Supports 8-segment digital displays up to a maximum of N
  - For the HT32F54231/HT32F54241, N = 8
  - For the HT32F54243/HT32F54253, N = 12
- Supports 8-segment digital displays with common anode or common cathode
- Supports frame interrupt
- Three frequency sources: LSI, LSE and PCLK
- The LED light on/off times can be controlled using the dead time setting

The LED controller is used to drive 8-segment digital displays. For the HT32F54231/HT32F54241 devices, the LED controller can drive up to eight 8-segment digital displays. For the HT32F54243/HT32F54253 devices, the LED controller can drive up to twelve 8-segment digital displays. Users have the flexibility to configure the pin position and number of the COMs according to the digital displays in their application. In a complete frame period, the enabled COMs will be scanned from the lower to the higher. Taking an example of where four 8-segment LEDs are used and where COM0, COM5, COM6 and COM7 are enabled. Here COM0, COM5, COM6 and the COM7 will be scanned successively in this sequence within a complete frame period. The scanning time of each COM port is equal to 1/4 frame, which is subdivided into the dead time duty and the COM duty. Users can adjust the dead time duty to change the LED brightness.

Touch Key – TKEY

- Four key oscillator frequencies: 1 MHz / 3 MHz / 7 MHz / 11 MHz
- 1024 level reference oscillator internal capacitor for frequency matching
- Single 16-bit C/F Counter
- Three scan modes: Manual mode, Auto scan mode and Periodic auto scan mode
- Support detection in the Sleep, Deep-Sleep1 and Deep-Sleep2 modes
- Hardware Upper or lower threshold comparators
- Keys are organised into several groups, with each group known as a module
  - For the HT32F54231/HT32F54241, having a module number, M0 to M5
  - For the HT32F54243/HT32F54253, having a module number, M0 to M6
- Each module is a fully independent set of four Touch Keys and each Touch Key has its own oscillator

All touch keys share a set of register array, which is used to store the reference oscillator capacitor setting and the touch key detection results. In addition, each touch key corresponds to a pair of upper / lower limit comparison registers, which are used to store the upper / lower limit threshold values. The hardware judges that an touch key is pressed or released according to the value stored in these registers.

Support detection in the Sleep, Deep-Sleep1 and Deep-Sleep2 modes. If the detected results conform to the condition that an touch key is pressed or released, the system will be wake-up and returned to normal mode.

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoints or code / literal patches
- 2 comparators for hardware watch points

Package and Operation Temperature

- 28-pin SSOP, 32 / 46-pin QFN and 48 / 64-pin LQFP packages
- Operation temperature range: -40 °C to 85 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

<table>
<tr><th colspan="2">Peripherals</th><th>HT32F54231</th><th>HT32F54241</th><th>HT32F54243</th><th>HT32F54253</th></tr>
<tr><td colspan="2">Main Flash (KB)</td><td>32</td><td>63</td><td>64</td><td>127</td></tr>
<tr><td colspan="2">Option Bytes Flash (KB)</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td colspan="2">SRAM (KB)</td><td>4</td><td>8</td><td>8</td><td>16</td></tr>
<tr><td rowspan="6">Timers</td><td>MCTM</td><td colspan="2">1</td><td colspan="2">1</td></tr>
<tr><td>GPTM</td><td colspan="2">1</td><td colspan="2">1</td></tr>
<tr><td>SCTM</td><td colspan="2">2</td><td colspan="2">4</td></tr>
<tr><td>BFTM</td><td colspan="2">2</td><td colspan="2">2</td></tr>
<tr><td>WDT</td><td colspan="2">1</td><td colspan="2">1</td></tr>
<tr><td>RTC</td><td colspan="2">1</td><td colspan="2">1</td></tr>
<tr><td rowspan="4">Communication</td><td>SPI</td><td colspan="2">2</td><td colspan="2">2</td></tr>
<tr><td>USART</td><td colspan="2">1</td><td colspan="2">2</td></tr>
<tr><td>UART</td><td colspan="2">2</td><td colspan="2">4</td></tr>
<tr><td>I^2C</td><td colspan="2">2</td><td colspan="2">3</td></tr>
<tr><td colspan="2">Hardware Divider</td><td colspan="4">1</td></tr>
<tr><td colspan="2">CRC-16/32</td><td colspan="4">1</td></tr>
<tr><td colspan="2">PDMA</td><td colspan="2">—</td><td colspan="2">6 channels</td></tr>
<tr><td colspan="2">EXTI</td><td colspan="4">16</td></tr>
<tr><td colspan="2" rowspan="2">12-bit ADC
Number of channels</td><td colspan="4">1</td></tr>
<tr><td colspan="4">Max. 10 external channels</td></tr>
<tr><td colspan="2">Comparator</td><td colspan="2">—</td><td colspan="2">2</td></tr>
<tr><td colspan="2">GPIO</td><td colspan="2">Up to 40</td><td colspan="2">Up to 54</td></tr>
<tr><td colspan="2">LED controller</td><td colspan="2">Up to 8 × 8-segment</td><td colspan="2">Up to 12 × 8-segment</td></tr>
<tr><td colspan="2">Touch key</td><td colspan="2">24</td><td colspan="2">28</td></tr>
<tr><td colspan="2">CPU frequency</td><td colspan="4">Up to 60 MHz</td></tr>
<tr><td colspan="2">Operating voltage</td><td colspan="4">2.5 V ~ 5.5 V</td></tr>
<tr><td colspan="2">Operating temperature</td><td colspan="4">-40 °C ~ 85 °C</td></tr>
<tr><td colspan="2">Package</td><td colspan="2">28-pin SSOP
32 / 46-pin QFN, 48-pin LQFP</td><td colspan="2">32 / 46-pin QFN,
48 / 64-pin LQFP</td></tr>
</table>

Block Diagram

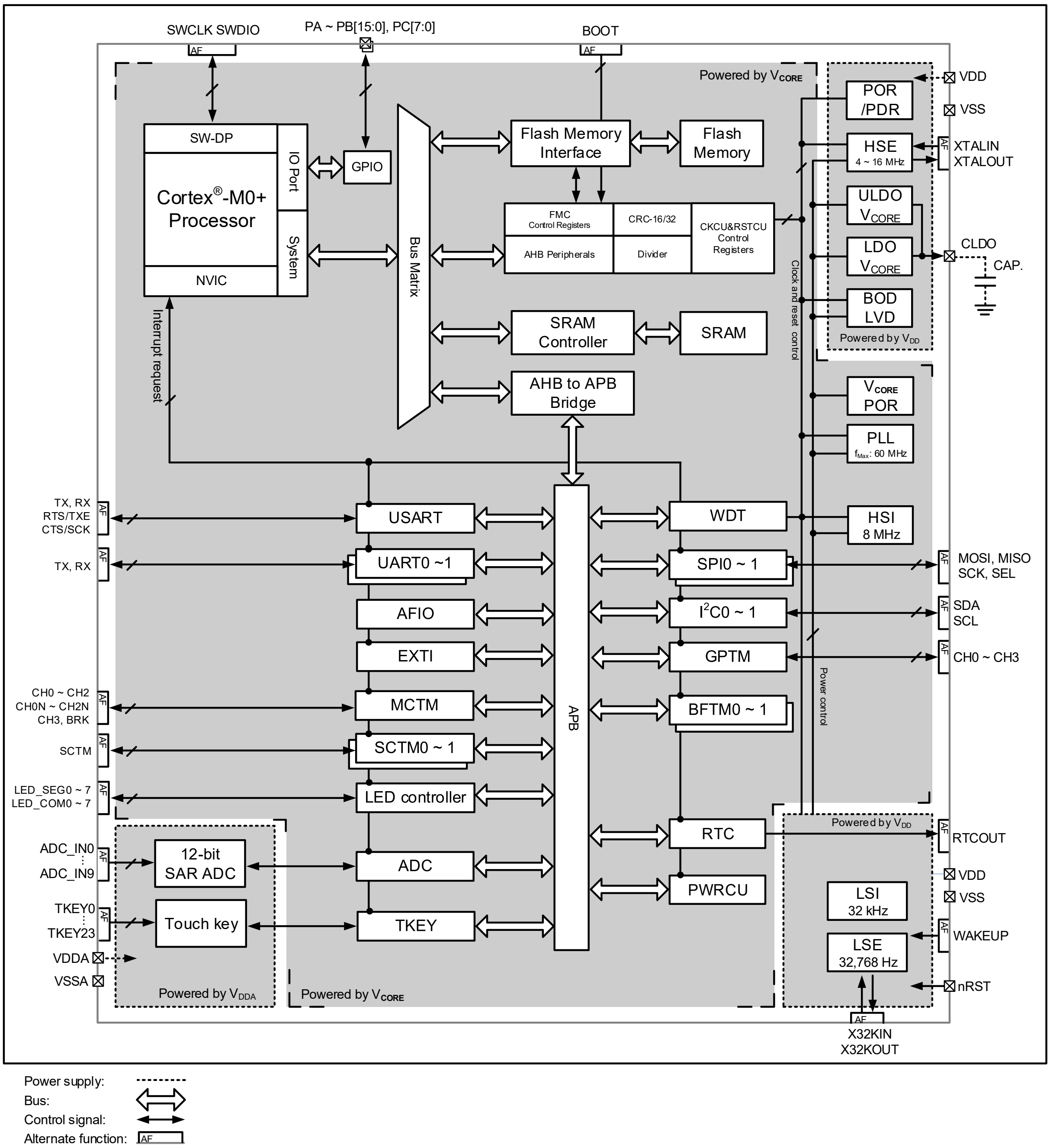


Figure 1. HT32F54231/HT32F54241 Block Diagram

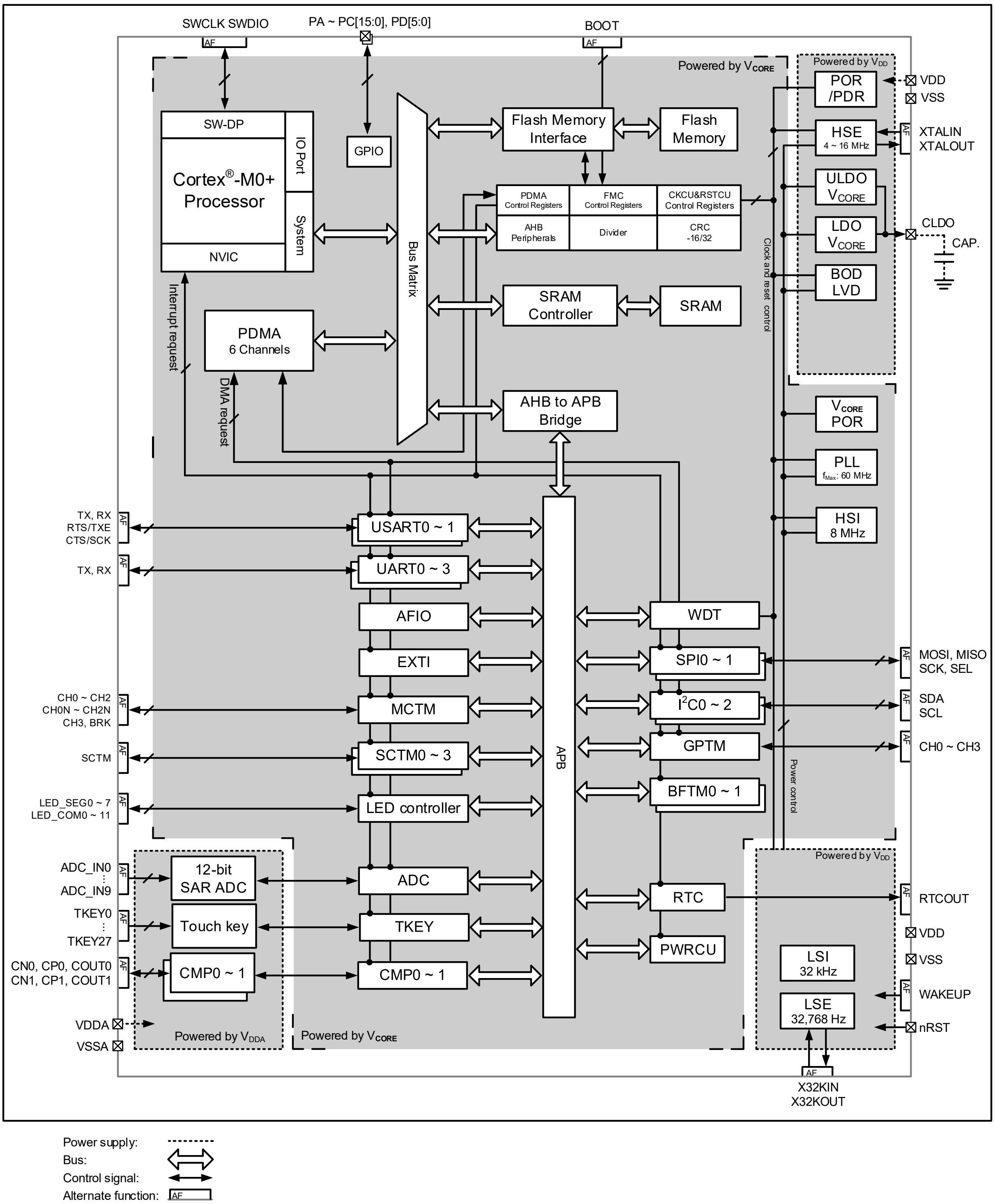


Figure 2. HT32F54243/HT32F54253 Block Diagram

Memory Map

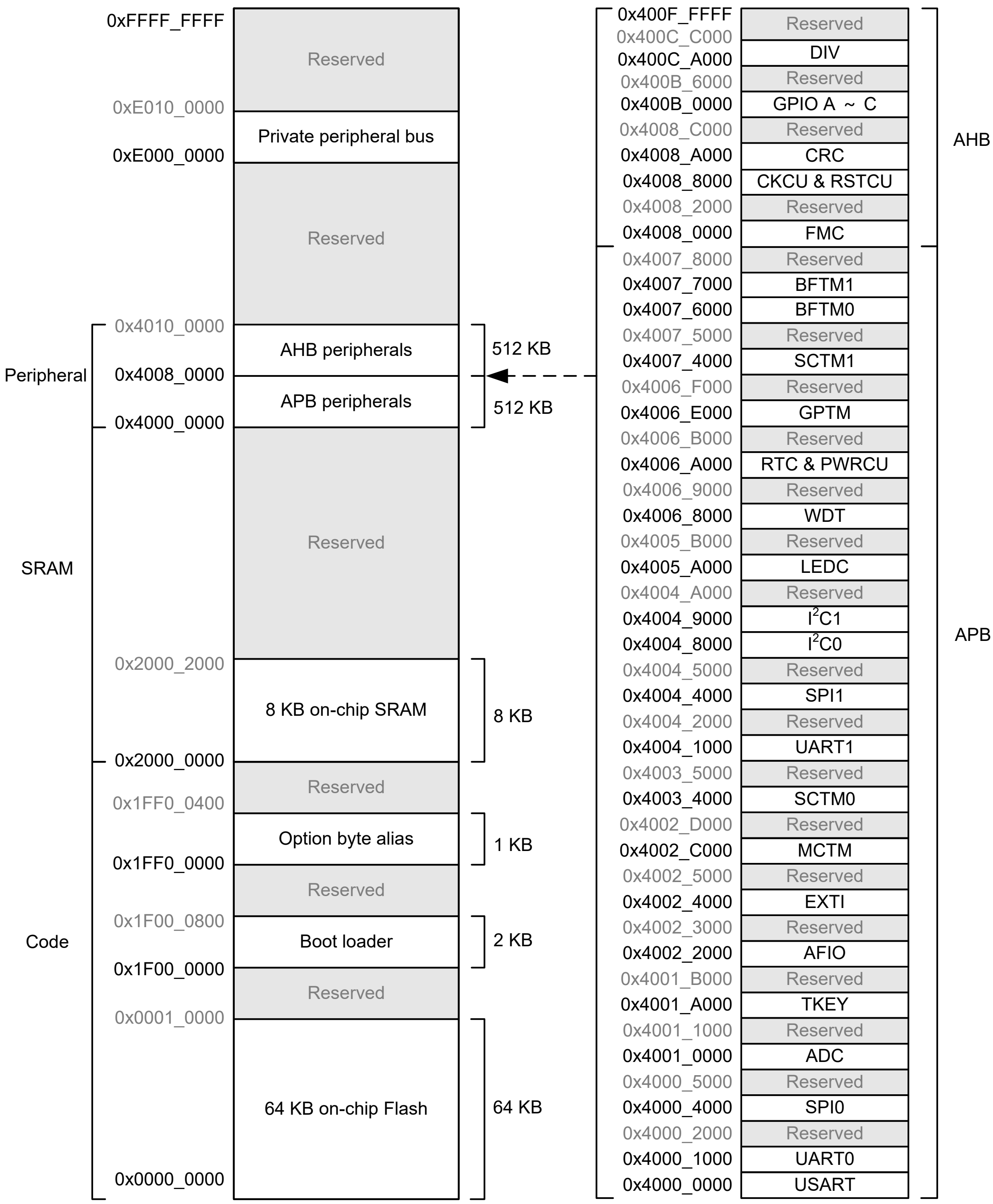


Figure 3. HT32F54231/HT32F54241 Memory Map

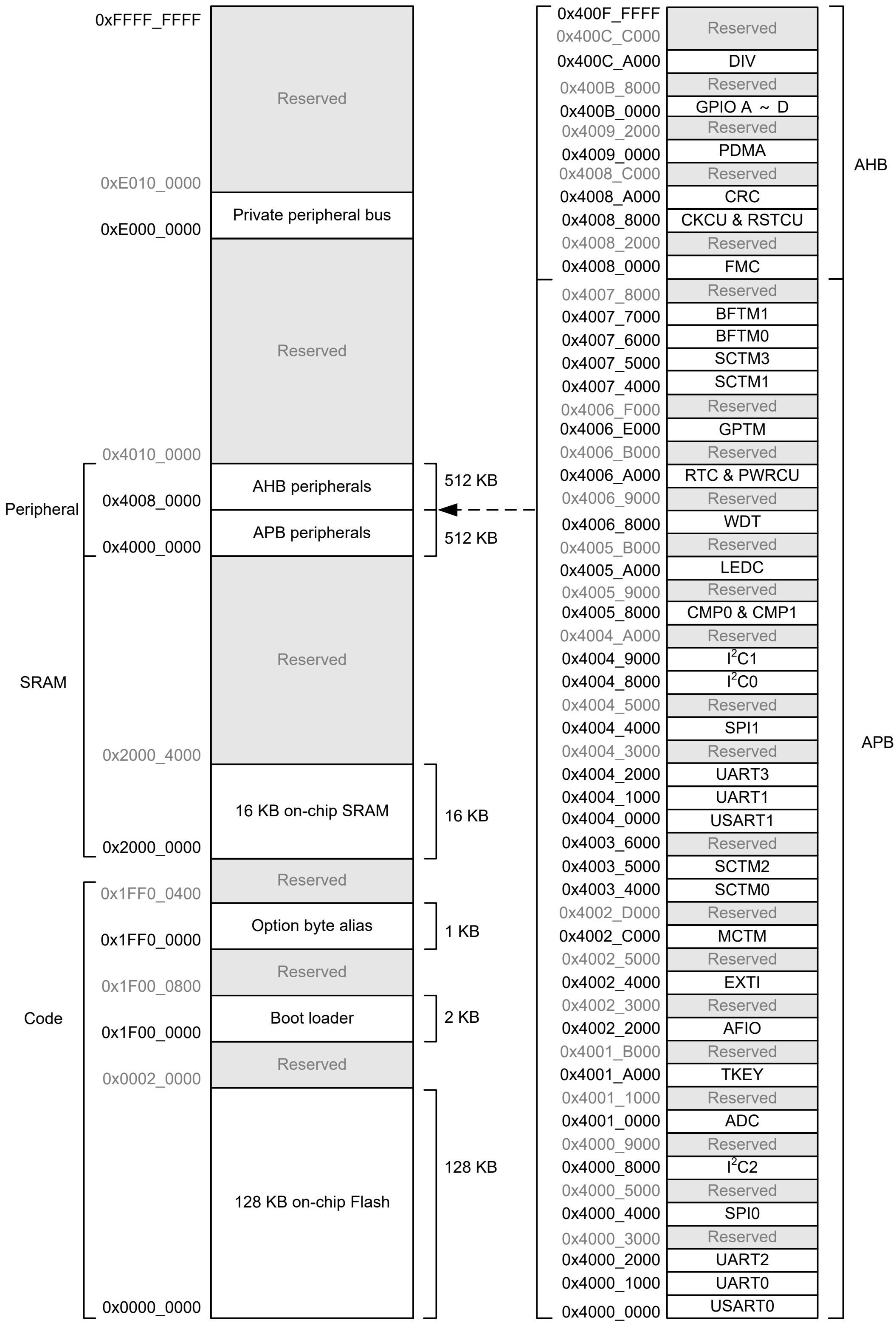


Figure 4. HT32F54243/HT32F54253 Memory Map

Table 2. HT32F54231/HT32F54241 Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART	APB
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI0	
0x4000_5000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4001_9FFF	Reserved	
0x4001_A000	0x4001_AFFF	TKEY	
0x4001_B000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4002_BFFF	Reserved	
0x4002_C000	0x4002_CFFF	MCTM	
0x4002_D000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4004_0FFF	Reserved	
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_3FFF	Reserved	
0x4004_4000	0x4004_4FFF	SPI1	
0x4004_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^2C0	
0x4004_9000	0x4004_9FFF	I^2C1	
0x4004_A000	0x4005_9FFF	Reserved	
0x4005_A000	0x4005_AFFF	LEDC	
0x4005_B000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC & PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	

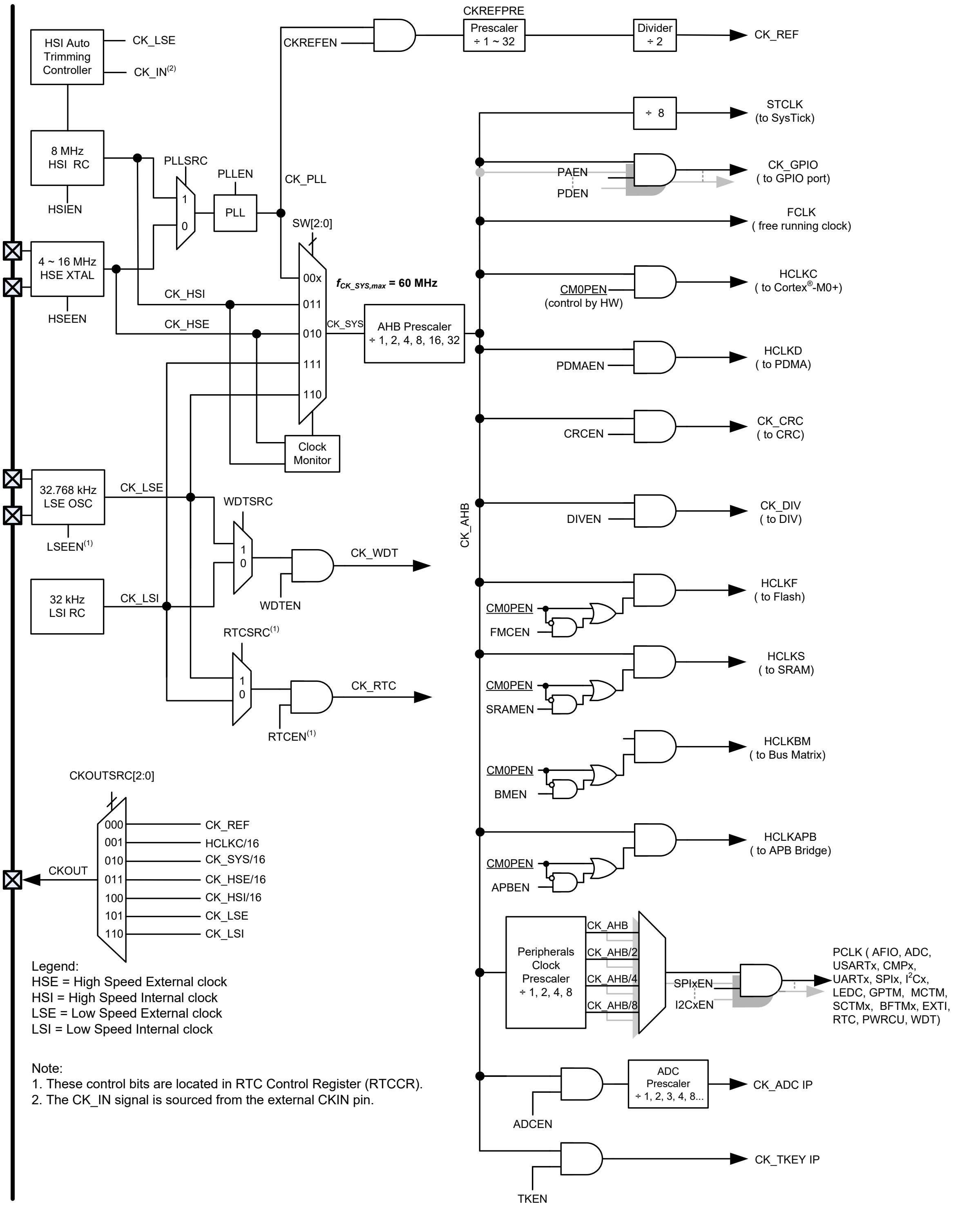
Start Address	End Address	Peripheral	Bus
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU & RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIO A	
0x400B_2000	0x400B_3FFF	GPIO B	
0x400B_4000	0x400B_5FFF	GPIO C	
0x400B_6000	0x400C_9FFF	Reserved	
0x400C_A000	0x400C_BFFF	DIV	
0x400C_C000	0x400F_FFFF	Reserved	

Table 3. HT32F54243/HT32F54253 Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART0	APB
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_2FFF	UART2	
0x4000_3000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI0	
0x4000_5000	0x4000_7FFF	Reserved	
0x4000_8000	0x4000_8FFF	I²C2	
0x4000_9000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4001_9FFF	Reserved	
0x4001_A000	0x4001_AFFF	TKEY	
0x4001_B000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4002_BFFF	Reserved	
0x4002_C000	0x4002_CFFF	MCTM	
0x4002_D000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4003_5FFF	SCTM2	
0x4003_6000	0x4003_FFFF	Reserved	
0x4004_0000	0x4004_0FFF	USART1	
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_2FFF	UART3	
0x4004_3000	0x4004_3FFF	Reserved	
0x4004_4000	0x4004_4FFF	SPI1	
0x4004_5000	0x4004_7FFF	Reserved	

Start Address	End Address	Peripheral	Bus
0x4004_8000	0x4004_8FFF	I2C0	APB
0x4004_9000	0x4004_9FFF	I2C1	
0x4004_A000	0x4005_7FFF	Reserved	
0x4005_8000	0x4005_8FFF	CMP0 & CMP1	
0x4005_9000	0x4005_9FFF	Reserved	
0x4005_A000	0x4005_AFFF	LEDC	
0x4005_B000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC & PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	SCTM3	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU & RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x4008_FFFF	Reserved	
0x4009_0000	0x4009_1FFF	PDMA	
0x4009_2000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIO A	
0x400B_2000	0x400B_3FFF	GPIO B	
0x400B_4000	0x400B_5FFF	GPIO C	
0x400B_6000	0x400B_7FFF	GPIO D	
0x400B_8000	0x400C_9FFF	Reserved	
0x400C_A000	0x400C_BFFF	DIV	
0x400C_C000	0x400F_FFFF	Reserved	

Clock Structure



Legend:
HSE = High Speed External clock
HSI = High Speed Internal clock
LSE = Low Speed External clock
LSI = Low Speed Internal clock

Note:
1. These control bits are located in RTC Control Register (RTCCR).
2. The CK_IN signal is sourced from the external CKIN pin.

Figure 5. Clock Structure

4 Pin Assignment

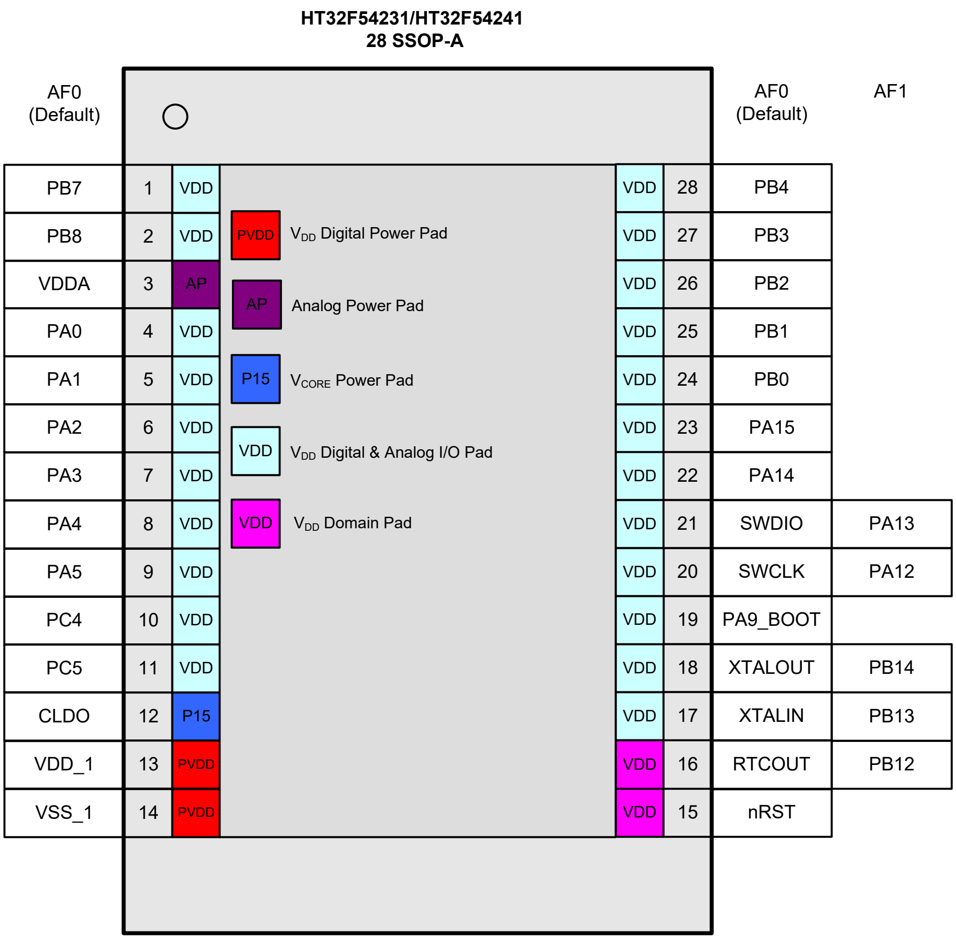
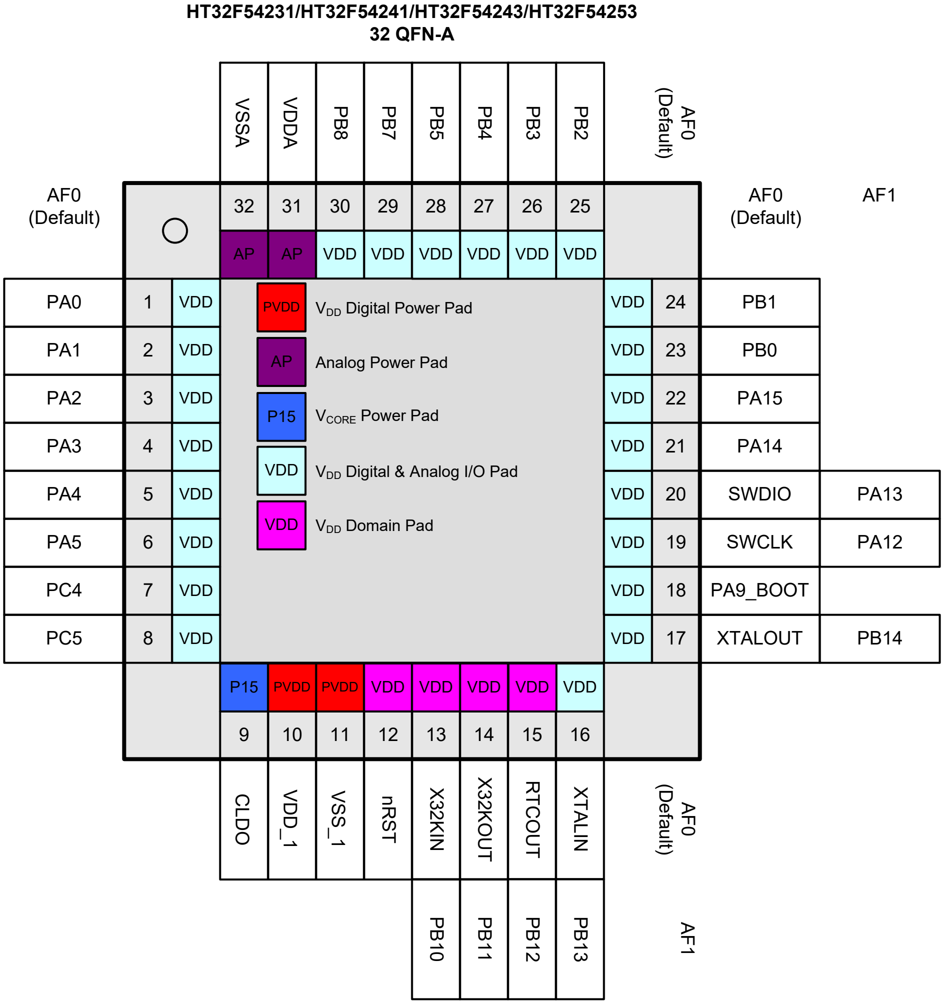


Figure 6. HT32F54231/HT32F54241 28-pin SSOP Pin Assignment



Note: The substrate is internally connected to VSS.

Figure 7. HT32F54231/HT32F54241/HT32F54243/HT32F54253 32-pin QFN Pin Assignment

HT32F54231/HT32F54241/HT32F54243/HT32F54253
46 QFN-A

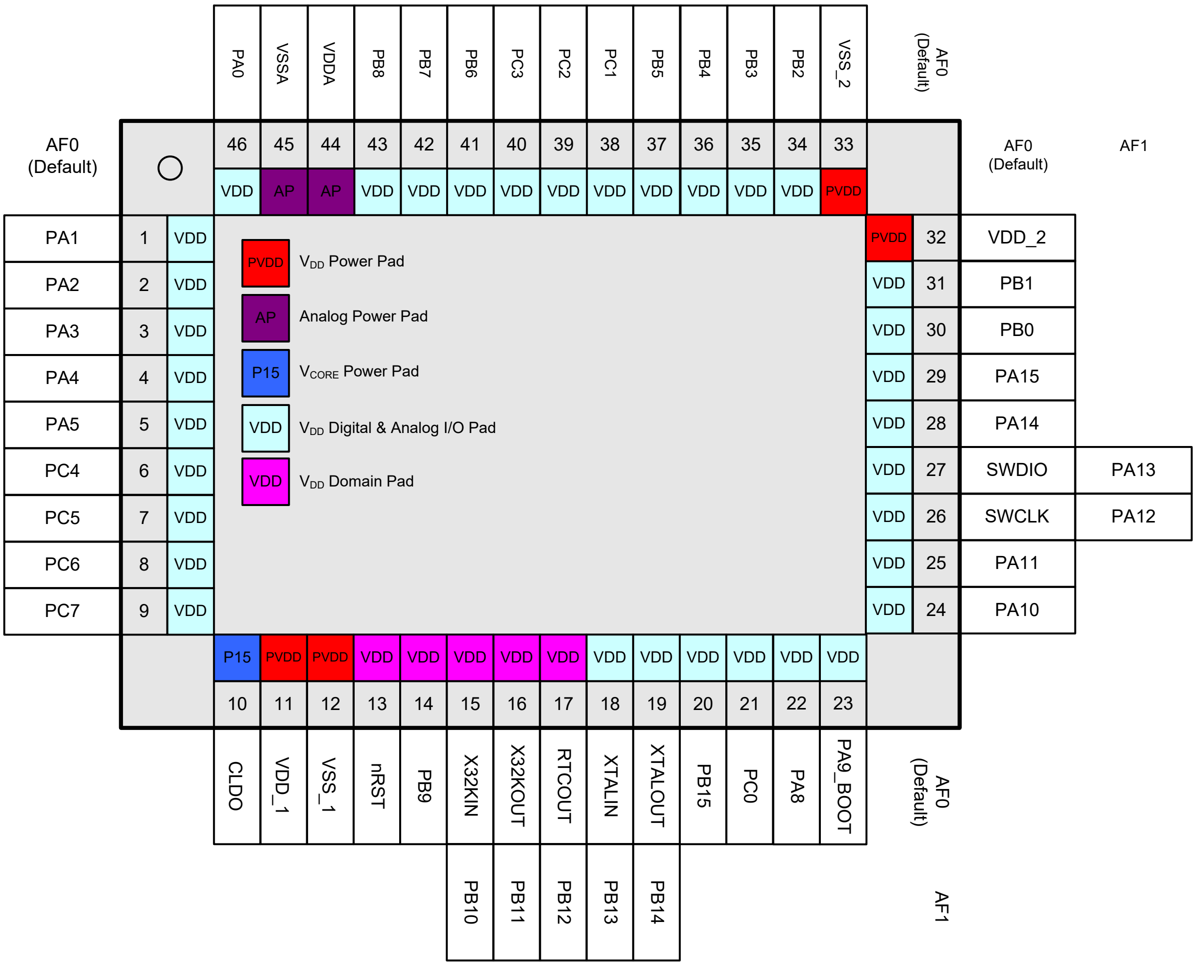


Figure 8. HT32F54231/HT32F54241/HT32F54243/HT32F54253 46-pin QFN Pin Assignment

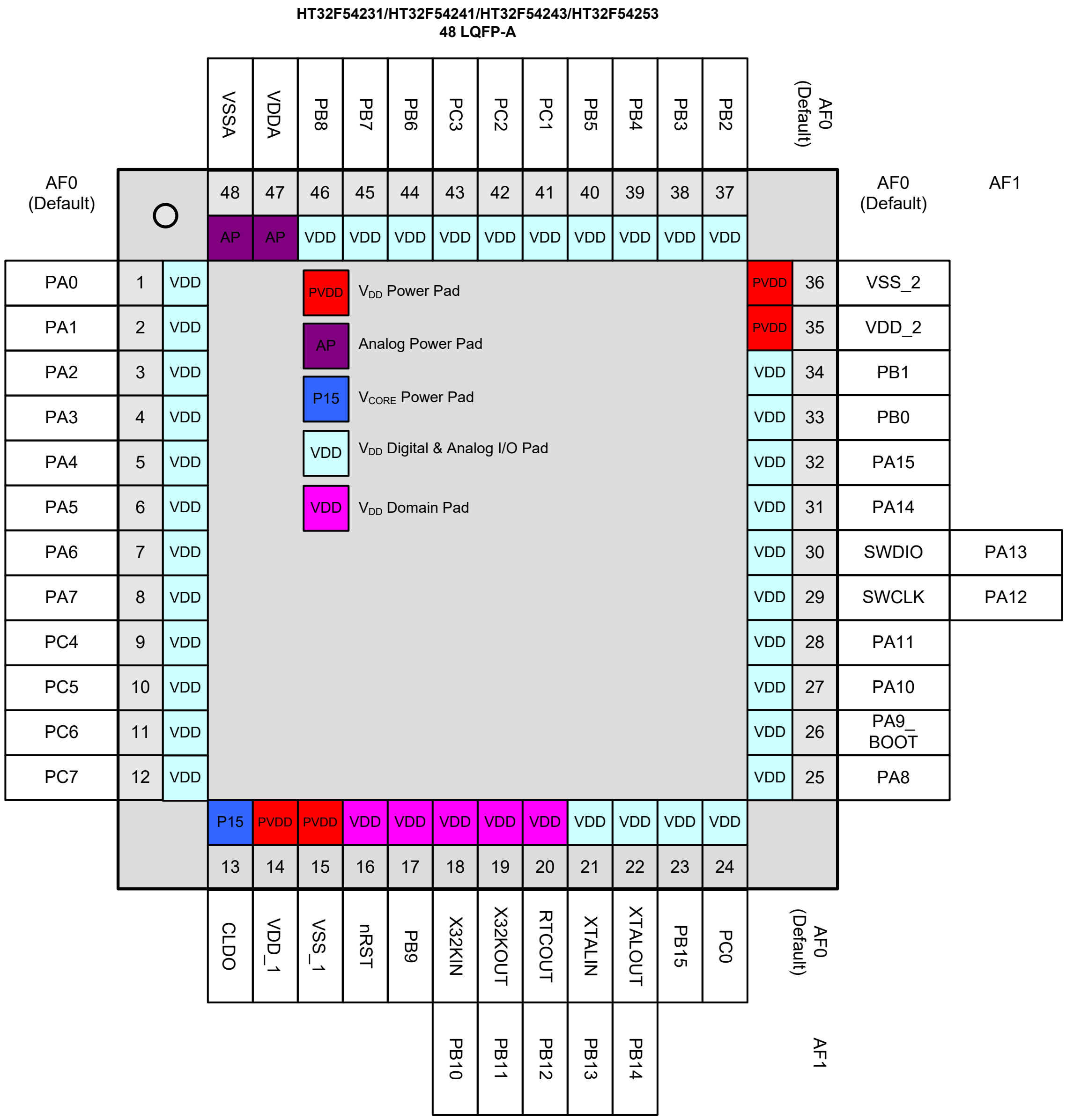


Figure 9. HT32F54231/HT32F54241/HT32F54243/HT32F54253 48-pin LQFP Pin Assignment

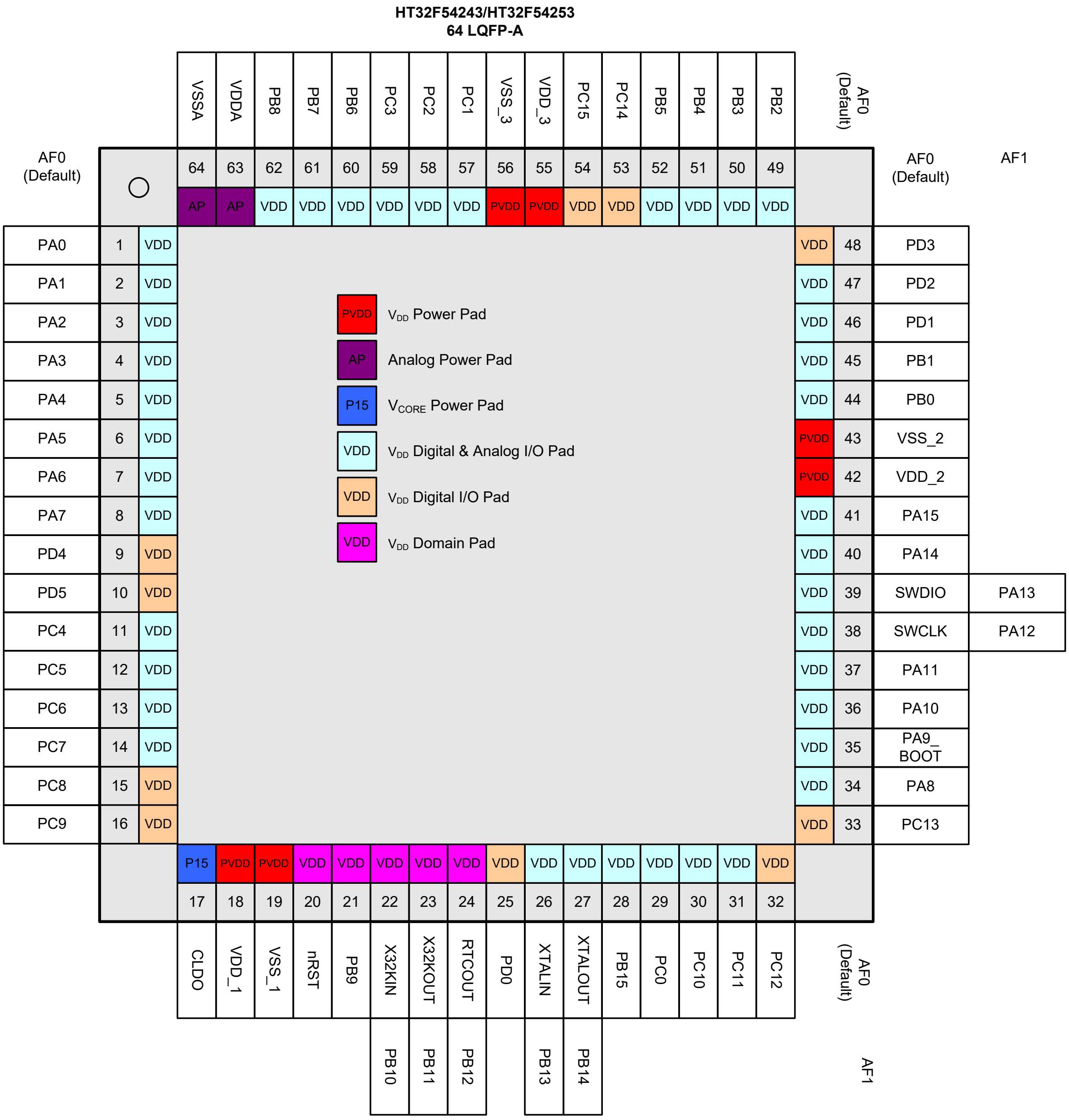


Figure 10. HT32F54243/HT32F54253 64-pin LQFP Pin Assignment

Table 4. HT32F54231/HT32F54241 Series Pin Assignment

Packages				Alternate Function Mapping															
				AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
48 LQFP	46 QFN	32 QFN	28 SSOP	System Default	GPIO	ADC	N/A	MCTM /GPTM	SPI	USART /UART	I²C	N/A	N/A	N/A	N/A	TKEY	SCTM	LEDC	System Other
1	46	1	4	PA0		ADC_IN2		GT_CH0	SPI1_SCK	USR_RTS	I2C1_SCL							LED_SEG0	VREF
2	1	2	5	PA1		ADC_IN3		GT_CH1	SPI1_MOSI	USR_CTS	I2C1_SDA							LED_SEG1	
3	2	3	6	PA2		ADC_IN4		GT_CH2	SPI1_MISO	USR_TX								LED_SEG2	
4	3	4	7	PA3		ADC_IN5		GT_CH3	SPI1_SEL	USR_RX								LED_SEG3	
5	4	5	8	PA4		ADC_IN6		GT_CH0	SPI0_SCK	UR1_TX	I2C0_SCL							LED_SEG4	
6	5	6	9	PA5		ADC_IN7		GT_CH1	SPI0_MOSI	UR1_RX	I2C0_SDA							LED_SEG5	
7				PA6		ADC_IN8		GT_CH2	SPI0_MISO									LED_SEG6	
8				PA7		ADC_IN9		GT_CH3	SPI0_SEL									LED_SEG7	
9	6	7	10	PC4						USR_TX						TKEY0	SCTM0	LED_COM4	
10	7	8	11	PC5						USR_RX						TKEY1	SCTM1	LED_COM5	
11	8			PC6				MT_CH2		UR0_TX	I2C0_SCL					TKEY2		LED_COM6	
12	9			PC7				MT_CH2N		UR0_RX	I2C0_SDA					TKEY3		LED_COM7	
13	10	9	12	CLDO															
14	11	10	13	VDD_1															
15	12	11	14	VSS_1															
16	13	12	15	nRST															
17	14			PB9				MT_CH3											WAKEUP1
18	15	13		X32KIN	PB10			GT_CH0	SPI1_SEL	USR_TX							SCTM0	LED_SEG4	
19	16	14		X32KOUT	PB11			GT_CH1	SPI1_SCK	USR_RX							SCTM1	LED_SEG5	
20	17	15	16	RTCOUT	PB12				SPI0_MISO	UR0_RX							SCTM0		WAKEUP0
21	18	16	17	XTALIN	PB13					UR0_TX	I2C0_SCL							LED_SEG6	
22	19	17	18	XTALOUT	PB14					UR0_RX	I2C0_SDA							LED_SEG7	
23	20			PB15				MT_CH0	SPI0_SEL		I2C1_SCL					TKEY4			
24	21			PC0				MT_CH0N	SPI0_SCK		I2C1_SDA					TKEY5	SCTM1	LED_COM0	
25	22			PA8						USR_TX						TKEY6	SCTM0	LED_COM1	
26	23	18	19	PA9_BOOT					SPI0_MOSI							TKEY7	SCTM1		CKOUT
27	24			PA10				MT_CH1	SPI0_MOSI	USR_RX						TKEY8		LED_COM2	
28	25			PA11				MT_CH1N	SPI0_MISO							TKEY9	SCTM0	LED_COM3	
29	26	19	20	SWCLK	PA12											TKEY10			
30	27	20	21	SWDIO	PA13											TKEY11			
31	28	21	22	PA14				MT_CH0	SPI1_SEL	UR1_TX	I2C1_SCL					TKEY12		LED_COM0	
32	29	22	23	PA15				MT_CH0N	SPI1_SCK	UR1_RX	I2C1_SDA					TKEY13	SCTM1	LED_COM1	
33	30	23	24	PB0				MT_CH1	SPI1_MOSI	USR_TX	I2C0_SCL					TKEY14		LED_SEG0	
34	31	24	25	PB1				MT_CH1N	SPI1_MISO	USR_RX	I2C0_SDA					TKEY15	SCTM0	LED_SEG1	
35	32			VDD_2															
36	33	SUB(Note)		VSS_2															

Packages				Alternate Function Mapping															
				AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
48 LQFP	46 QFN	32 QFN	28 SSOP	System Default	GPIO	ADC	N/A	MCTM /GPTM	SPI	USART /UART	I²C	N/A	N/A	N/A	N/A	TKEY	SCTM	LEDC	System Other
37	34	25	26	PB2				MT_CH2	SPI0_SEL	UR1_TX						TKEY16		LED_SEG2	CKIN
38	35	26	27	PB3				MT_CH2N	SPI0_SCK	UR1_RX						TKEY17	SCTM1	LED_SEG3	
39	36	27	28	PB4				MT_BRK	SPI0_MOSI	UR1_TX						TKEY18	SCTM0	LED_COM2	
40	37	28		PB5				GT_CH2	SPI0_MISO	UR1_RX						TKEY19		LED_COM3	
41	38			PC1				MT_CH0	SPI1_SEL	UR1_TX						TKEY20		LED_COM4	
42	39			PC2				MT_CH0N	SPI1_SCK							TKEY21		LED_COM5	
43	40			PC3				MT_BRK	SPI1_MOSI	UR1_RX						TKEY22		LED_COM6	
44	41			PB6				GT_CH3	SPI1_MISO	UR0_TX						TKEY23		LED_COM7	
45	42	29	1	PB7		ADC_IN0		MT_CH1	SPI0_MISO	UR0_TX	I2C1_SCL							LED_SEG4	
46	43	30	2	PB8		ADC_IN1		MT_CH1N	SPI0_SEL	UR0_RX	I2C1_SDA							LED_SEG5	
47	44	31	3	VDDA															
48	45	32		VSSA															

Note: The SUB is the substrate and connected to VSS.

Table 5. HT32F54243/HT32F54253 Series Pin Assignment

Packages				Alternate Function Mapping															
				AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64 LQFP	48 LQFP	46 QFN	32 QFN	System Default	GPIO	ADC	CMP	MCTM /GPTM	SPI	USART /UART	I²C	N/A	N/A	N/A	N/A	TKEY	SCTM	LEDC	System Other
1	1	46	1	PA0		ADC_IN2		GT_CH0	SPI1_SCK	USR0_RTS	I2C1_SCL							LED_SEG0	VREF
2	2	1	2	PA1		ADC_IN3		GT_CH1	SPI1_MOSI	USR0_CTS	I2C1_SDA							LED_SEG1	
3	3	2	3	PA2		ADC_IN4		GT_CH2	SPI1_MISO	USR0_TX								LED_SEG2	
4	4	3	4	PA3		ADC_IN5		GT_CH3	SPI1_SEL	USR0_RX							SCTM2	LED_SEG3	
5	5	4	5	PA4		ADC_IN6		GT_CH0	SPI0_SCK	USR1_TX	I2C0_SCL							LED_SEG4	
6	6	5	6	PA5		ADC_IN7		GT_CH1	SPI0_MOSI	USR1_RX	I2C0_SDA							LED_SEG5	
7	7			PA6		ADC_IN8		GT_CH2	SPI0_MISO	USR1_RTS								LED_SEG6	
8	8			PA7		ADC_IN9		GT_CH3	SPI0_SEL	USR1_CTS							SCTM3	LED_SEG7	
9				PD4						USR1_TX							SCTM0	LED_SEG4	
10				PD5						USR1_RX							SCTM1	LED_SEG5	
11	9	6	7	PC4				GT_CH0	SPI1_SEL	USR0_TX	I2C1_SCL					TKEY0	SCTM0	LED_COM4	
12	10	7	8	PC5				GT_CH1	SPI1_SCK	USR0_RX	I2C1_SDA					TKEY1	SCTM1	LED_COM5	
13	11	8		PC6				MT_CH2	SPI1_MOSI	UR0_TX	I2C0_SCL					TKEY2	SCTM2	LED_COM6	
14	12	9		PC7				MT_CH2N	SPI1_MISO	UR0_RX	I2C0_SDA					TKEY3	SCTM3	LED_COM7	
15				PC8				GT_CH2	SPI1_MOSI	UR1_TX	I2C0_SCL							LED_COM10	
16				PC9				GT_CH3	SPI1_MISO	UR1_RX	I2C0_SDA							LED_COM11	
17	13	10	9	CLDO															
18	14	11	10	VDD_1															
19	15	12	11	VSS_1															

Packages				Alternate Function Mapping															
				AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64 LQFP	48 LQFP	46 QFN	32 QFN	System Default	GPIO	ADC	CMP	MCTM /GPTM	SPI	USART /UART	I^{2}C	N/A	N/A	N/A	N/A	TKEY	SCTM	LEDC	System Other
20	16	13	12	nRST															
21	17	14		PB9				MT_CH3		UR0_TX							SCTM1		WAKEUP1
22	18	15	13	X32KIN	PB10			GT_CH0	SPI1_SEL	USR1_TX	I2C2_SCL						SCTM2	LED_SEG4	
23	19	16	14	X32KOUT	PB11			GT_CH1	SPI1_SCK	USR1_RX	I2C2_SDA						SCTM3	LED_SEG5	
24	20	17	15	RTCOUT	PB12				SPI0_MISO	UR0_RX							SCTM0		WAKEUP0
25				PD0							I2C2_SDA						SCTM2		
26	21	18	16	XTALIN	PB13					UR3_TX	I2C0_SCL							LED_SEG6	
27	22	19	17	XTALOUT	PB14					UR3_RX	I2C0_SDA							LED_SEG7	
28	23	20		PB15				MT_CH0	SPI0_SEL	USR1_TX	I2C1_SCL					TKEY4			
29	24	21		PC0				MT_CH0N	SPI0_SCK	USR1_RX	I2C1_SDA					TKEY5	SCTM3	LED_COM0	
30				PC10				GT_CH0	SPI1_SEL	UR2_TX						TKEY6		LED_SEG0	
31				PC11				GT_CH1	SPI1_SCK	UR2_RX						TKEY7		LED_SEG1	
32				PC12				GT_CH2	SPI1_MOSI	UR1_TX	I2C2_SCL							LED_SEG2	
33				PC13				GT_CH3	SPI1_MISO	UR1_RX	I2C2_SDA							LED_SEG3	
34	25	22		PA8						USR0_TX						TKEY8	SCTM2	LED_COM1	
35	26	23	18	PA9_BOOT					SPI0_MOSI	UR3_TX						TKEY9	SCTM3		CKOUT
36	27	24		PA10				MT_CH1	SPI0_MOSI	USR0_RX	I2C2_SCL					TKEY10		LED_COM2	
37	28	25		PA11				MT_CH1N	SPI0_MISO	UR3_RX	I2C2_SDA					TKEY11	SCTM0	LED_COM3	
38	29	26	19	SWCLK	PA12											TKEY12			
39	30	27	20	SWDIO	PA13											TKEY13			
40	31	28	21	PA14				MT_CH0	SPI1_SEL	USR0_RTS	I2C1_SCL					TKEY14		LED_COM0	
41	32	29	22	PA15				MT_CH0N	SPI1_SCK	USR0_CTS	I2C1_SDA					TKEY15	SCTM1	LED_COM1	
42	35	32		VDD_2															
43	36	33	SUB[Note]	VSS_2															
44	33	30	23	PB0				MT_CH1	SPI1_MOSI	USR0_TX	I2C0_SCL					TKEY16		LED_SEG0	
45	34	31	24	PB1				MT_CH1N	SPI1_MISO	USR0_RX	I2C0_SDA					TKEY17	SCTM2	LED_SEG1	
46				PD1				MT_CH2		USR1_RTS						TKEY18			
47				PD2				MT_CH2N		USR1_CTS						TKEY19		LED_SEG6	
48				PD3				MT_CH3										LED_SEG7	
49	37	34	25	PB2			COUT0	MT_CH2	SPI0_SEL	UR2_TX						TKEY20		LED_SEG2	CKIN
50	38	35	26	PB3			COUT1	MT_CH2N	SPI0_SCK	UR2_RX						TKEY21	SCTM1	LED_SEG3	
51	39	36	27	PB4				MT_BRK	SPI0_MOSI	UR1_TX						TKEY22	SCTM0	LED_COM2	
52	40	37	28	PB5				GT_CH2	SPI0_MISO	UR1_RX						TKEY23		LED_COM3	
53				PC14			COUT0	MT_CH3		UR3_TX	I2C2_SCL						SCTM2	LED_COM8	
54				PC15			COUT1			UR3_RX	I2C2_SDA						SCTM3	LED_COM9	
55				VDD_3															
56				VSS_3															

Packages				Alternate Function Mapping															
				AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64 LQFP	48 LQFP	46 QFN	32 QFN	System Default	GPIO	ADC	CMP	MCTM /GPTM	SPI	USART /UART	I²C	N/A	N/A	N/A	N/A	TKEY	SCTM	LEDC	System Other
57	41	38		PC1			CN0	MT_ CH0	SPI1_ SEL	UR1_TX						TKEY24		LED_ COM4	
58	42	39		PC2			CP0	MT_ CH0N	SPI1_ SCK	UR2_RX						TKEY25		LED_ COM5	
59	43	40		PC3			COUT0	MT_ BRK	SPI1_ MOSI	UR1_RX	I2C2_ SCL					TKEY26		LED_ COM6	
60	44	41		PB6			CN1	GT_ CH3	SPI1_ MISO	UR2_TX	I2C2_ SDA					TKEY27		LED_ COM7	
61	45	42	29	PB7		ADC_ IN0	CP1	MT_ CH1	SPI0_ MISO	UR0_TX	I2C1_ SCL							LED_ SEG4	
62	46	43	30	PB8		ADC_ IN1	COUT1	MT_ CH1N	SPI0_ SEL	UR0_RX	I2C1_ SDA							LED_ SEG5	
63	47	44	31	VDDA															
64	48	45	32	VSSA															

Note: The SUB is the substrate and connected to VSS.

Table 6. HT32F54231/HT32F54241 Pin Description

Pin Number				Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
48 LQFP	46 QFN	32 QFN	28 SSOP					Default Function (AF0)
1	46	1	4	PA0	AI/O	5V	4/8/12/16 mA	PA0
2	1	2	5	PA1	AI/O	5V	4/8/12/16 mA	PA1
3	2	3	6	PA2	AI/O	5V	4/8/12/16 mA	PA2
4	3	4	7	PA3	AI/O	5V	4/8/12/16 mA	PA3
5	4	5	8	PA4	AI/O	5V	4/8/12/16 mA	PA4, this pin provides a UART_TX function in the Boot loader mode.
6	5	6	9	PA5	AI/O	5V	4/8/12/16 mA	PA5, this pin provides a UART_RX function in the Boot loader mode.
7				PA6	AI/O	5V	4/8/12/16 mA	PA6
8				PA7	AI/O	5V	4/8/12/16 mA	PA7
9	6	7	10	PC4	AI/O	5V	4/8/12/16 mA	PC4
10	7	8	11	PC5	AI/O	5V	4/8/12/16 mA	PC5
11	8			PC6	AI/O	5V	4/8/12/16 mA	PC6
12	9			PC7	AI/O	5V	4/8/12/16 mA	PC7
13	10	9	12	CLDO	P	—	—	Core power LDO V_{CORE} output It is must be connected a 2.2 μF capacitor as close as possible between this pin and VSS_1.
14	11	10	13	VDD_1	P	—	—	Voltage for V_{DD} domain digital I/O
15	12	11	14	VSS_1	P	—	—	Ground reference for digital I/O
16	13	12	15	nRST(3)	I	5V_PU	—	External reset pin
17	14			PB9(3)	I/O (V_{DD})	5V	4/8/12/16 mA	PB9
18	15	13		PB10(3)	AI/O (V_{DD})	5V	4/8/12/16 mA	X32KIN
19	16	14		PB11(3)	AI/O (V_{DD})	5V	4/8/12/16 mA	X32KOUT
20	17	15	16	PB12(3)	I/O (V_{DD})	5V	4/8/12/16 mA	RTCOUT
21	18	16	17	PB13	AI/O	5V	4/8/12/16 mA	XTALIN
22	19	17	18	PB14	AI/O	5V	4/8/12/16 mA	XTALOUT
23	20			PB15	AI/O	5V	4/8/12/16 mA	PB15
24	21			PC0	AI/O	5V	4/8/12/16 mA	PC0

Pin Number				Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
48 LQFP	46 QFN	32 QFN	28 SSOP					Default Function (AF0)
25	22			PA8	AI/O	5V	4/8/12/16 mA	PA8
26	23	18	19	PA9	AI/O	5V_PU	4/8/12/16 mA	PA9_BOOT
27	24			PA10	AI/O	5V	4/8/12/16 mA	PA10
28	25			PA11	AI/O	5V	4/8/12/16 mA	PA11
29	26	19	20	PA12	AI/O	5V_PU	4/8/12/16 mA	SWCLK
30	27	20	21	PA13	AI/O	5V_PU	4/8/12/16 mA	SWDIO
31	28	21	22	PA14	AI/O	5V	4/8/12/16 mA	PA14
32	29	22	23	PA15	AI/O	5V	4/8/12/16 mA	PA15
33	30	23	24	PB0	AI/O	5V	4/8/12/16 mA	PB0
34	31	24	25	PB1	AI/O	5V	4/8/12/16 mA	PB1
35	32			VDD_2	P	—	—	Voltage for V_{DD} domain digital I/O
36	33			VSS_2	P	—	—	Ground reference for digital I/O
37	34	25	26	PB2	AI/O	5V	4/8/12/16 mA	PB2
38	35	26	27	PB3	AI/O	5V	4/8/12/16 mA	PB3
39	36	27	28	PB4	AI/O	5V	4/8/12/16 mA	PB4
40	37	28		PB5	AI/O	5V	4/8/12/16 mA	PB5
41	38			PC1	AI/O	5V	4/8/12/16 mA	PC1
42	39			PC2	AI/O	5V	4/8/12/16 mA	PC2
43	40			PC3	AI/O	5V	4/8/12/16 mA	PC3
44	41			PB6	AI/O	5V	4/8/12/16 mA	PB6
45	42	29	1	PB7	AI/O	5V	4/8/12/16 mA	PB7
46	43	30	2	PB8	AI/O	5V	4/8/12/16 mA	PB8
47	44	31	3	VDDA	P	—	—	Analog voltage for ADC
48	45	32		VSSA	P	—	—	Ground reference for the ADC

Note: 1. I = input, O = output, A = Analog port, P = Power Supply, V_{DD} = V_{DD} Power.
2. 5V = 5 V operation I/O type, PU = Pull-up.
3. These pins are located at the V_{DD} power domain.
4. In the Boot loader mode, the UART interface is available for communication.

Table 7. HT32F54243/HT32F54253 Pin Description

Pin Number				Pin Name	Type[(1)]	I/O Structure[(2)]	Output Driving	Description
64 LQFP	48 LQFP	46 QFN	32 QFN					Default Function (AF0)
1	1	46	1	PA0	AI/O	5V	4/8/12/16 mA	PA0
2	2	1	2	PA1	AI/O	5V	4/8/12/16 mA	PA1
3	3	2	3	PA2	AI/O	5V	4/8/12/16 mA	PA2
4	4	3	4	PA3	AI/O	5V	4/8/12/16 mA	PA3
5	5	4	5	PA4	AI/O	5V	4/8/12/16 mA	PA4, this pin provides a USART_TX function in the Boot loader mode.
6	6	5	6	PA5	AI/O	5V	4/8/12/16 mA	PA5, this pin provides a USART_RX function in the Boot loader mode.
7	7			PA6	AI/O	5V	4/8/12/16 mA	PA6
8	8			PA7	AI/O	5V	4/8/12/16 mA	PA7
9				PD4	I/O	5V	4/8/12/16 mA	PD4
10				PD5	I/O	5V	4/8/12/16 mA	PD5
11	9	6	7	PC4	AI/O	5V	4/8/12/16 mA	PC4
12	10	7	8	PC5	AI/O	5V	4/8/12/16 mA	PC5
13	11	8		PC6	AI/O	5V	4/8/12/16 mA	PC6
14	12	9		PC7	AI/O	5V	4/8/12/16 mA	PC7
15				PC8	I/O	5V	4/8/12/16 mA	PC8
16				PC9	I/O	5V	4/8/12/16 mA	PC9
17	13	10	9	CLDO	P	—	—	Core power LDO V_{CORE} output It is must be connected a 2.2 μF capacitor as close as possible between this pin and VSS_1.
18	14	11	10	VDD_1	P	—	—	Voltage for V_{DD} domain digital I/O
19	15	12	11	VSS_1	P	—	—	Ground reference for digital I/O
20	16	13	12	nRST[(3)]	I	5V_PU	—	External reset pin
21	17	14		PB9[(3)]	I/O (V_{DD})	5V	4/8/12/16 mA	PB9
22	18	15	13	PB10[(3)]	AI/O (V_{DD})	5V	4/8/12/16 mA	X32KIN
23	19	16	14	PB11[(3)]	AI/O (V_{DD})	5V	4/8/12/16 mA	X32KOUT
24	20	17	15	PB12[(3)]	I/O (V_{DD})	5V	4/8/12/16 mA	RTCOUT
25				PD0	I/O	5V	4/8/12/16 mA	PD0
26	21	18	16	PB13	AI/O	5V	4/8/12/16 mA	XTALIN
27	22	19	17	PB14	AI/O	5V	4/8/12/16 mA	XTALOUT
28	23	20		PB15	AI/O	5V	4/8/12/16 mA	PB15
29	24	21		PC0	AI/O	5V	4/8/12/16 mA	PC0
30				PC10	AI/O	5V	4/8/12/16 mA	PC10
31				PC11	AI/O	5V	4/8/12/16 mA	PC11
32				PC12	I/O	5V	4/8/12/16 mA	PC12
33				PC13	I/O	5V	4/8/12/16 mA	PC13
34	25	22		PA8	AI/O	5V	4/8/12/16 mA	PA8
35	26	23	18	PA9	AI/O	5V_PU	4/8/12/16 mA	PA9_BOOT
36	27	24		PA10	AI/O	5V	4/8/12/16 mA	PA10
37	28	25		PA11	AI/O	5V	4/8/12/16 mA	PA11
38	29	26	19	PA12	AI/O	5V_PU	4/8/12/16 mA	SWCLK
39	30	27	20	PA13	AI/O	5V_PU	4/8/12/16 mA	SWDIO
40	31	28	21	PA14	AI/O	5V	4/8/12/16 mA	PA14

Pin Number				Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
64 LQFP	48 LQFP	46 QFN	32 QFN					Default Function (AF0)
41	32	29	22	PA15	AI/O	5V	4/8/12/16 mA	PA15
42	35	32		VDD_2	P	—	—	Voltage for digital V_{DD} domain I/O
43	36	33	33	VSS_2	P	—	—	Ground reference for digital I/O
44	33	30	23	PB0	AI/O	5V	4/8/12/16 mA	PB0
45	34	31	24	PB1	AI/O	5V	4/8/12/16 mA	PB1
46				PD1	AI/O	5V	4/8/12/16 mA	PD1
47				PD2	AI/O	5V	4/8/12/16 mA	PD2
48				PD3	I/O	5V	4/8/12/16 mA	PD3
49	37	34	25	PB2	AI/O	5V	4/8/12/16 mA	PB2
50	38	35	26	PB3	AI/O	5V	4/8/12/16 mA	PB3
51	39	36	27	PB4	AI/O	5V	4/8/12/16 mA	PB4
52	40	37	28	PB5	AI/O	5V	4/8/12/16 mA	PB5
53				PC14	I/O	5V	4/8/12/16 mA	PC14
54				PC15	I/O	5V	4/8/12/16 mA	PC15
55				VDD_3	P	—	—	Voltage for V_{DD} domain digital I/O
56				VSS_3	P	—	—	Ground reference for digital I/O
57	41	38		PC1	AI/O	5V	4/8/12/16 mA	PC1
58	42	39		PC2	AI/O	5V	4/8/12/16 mA	PC2
59	43	40		PC3	AI/O	5V	4/8/12/16 mA	PC3
60	44	41		PB6	AI/O	5V	4/8/12/16 mA	PB6
61	45	42	29	PB7	AI/O	5V	4/8/12/16 mA	PB7
62	46	43	30	PB8	AI/O	5V	4/8/12/16 mA	PB8
63	47	44	31	VDDA	P	—	—	Analog voltage for ADC
64	48	45	32	VSSA	P	—	—	Ground reference for the ADC

Note: 1. I = input, O = output, A = Analog port, P = Power Supply, V_{DD} = V_{DD} Power.
2. 5V = 5 V operation I/O type, PU = Pull-up.
3. These pins are located at the V_{DD} power domain.
4. In the Boot loader mode, the USART interface is available for communication.

5 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	External Main Supply Voltage	V_{SS} - 0.3	V_{SS} + 5.5	V
V_{DDA}	External Analog Supply Voltage	V_{SSA} - 0.3	V_{SSA} + 5.5	V
V_{IN}	Input Voltage on I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
T_A	Ambient Operating Temperature Range	-40	85	°C
T_{STG}	Storage Temperature Range	-60	150	°C
T_J	Maximum Junction Temperature	—	125	°C
P_D	Total Power Dissipation	—	500	mW
V_{ESD}	Electrostatic Discharge Voltage – Human Body Mode	-4000	4000	V

Recommended DC Operating Conditions

Table 9. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	—	2.5	5.0	5.5	V
V_{DDA}	Analog Operating Voltage	—	2.5	5.0	5.5	V

On-Chip LDO Voltage Regulator Characteristics

Table 10. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	V_{DD} ≥ 2.5 V Regulator input @ I_{LDO} = 35 mA and voltage variant = ±5 %, After trimming	1.425	1.500	1.570	V
I_{LDO}	Output Current	V_{DD} = 2.5 V Regulator input @ V_{LDO} = 1.5 V	—	30	35	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1.0	2.2	—	μF

On-Chip Ultra-low Power LDO Voltage Regulator Characteristics

Table 11. ULDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operation Voltage	—	2.5	—	5.5	V
V_{ULDO}	Internal Regulator Output Voltage	V_{DD} ≥ 2.5 V Regulator input @ I_{ULDO} = 5 mA and voltage variant = ±10 %, after trimming	1.35	1.50	1.65	V
I_{ULDO}	Output Current	V_{DD} = 2.5 V Regulator input @ V_{ULDO} = 1.5 V	—	2	5	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	V_{IN} = 2.5 V Regulator input @ V_{ULDO} = 1.5 V, I_{ULDO} = 5 mA	1.0	2.2	—	μF

Power Consumption

Table 12. HT32F54231/HT32F54241 Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	f_{HCLK}	Conditions	Typ.	Max. @ T_A		Unit
					25 °C	85 °C	
I_{DD}	Supply Current (Run Mode)	60 MHz	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, All peripherals enabled	14.8	16.2	—	mA
			V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, All peripherals disabled	6.7	7.3	—	
		40 MHz	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, All peripherals enabled	11.8	12.9	—	
			V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, All peripherals disabled	6.4	7	—	
		20 MHz	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 20 MHz, All peripherals enabled	5.9	6.4	—	
			V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 20 MHz, All peripherals disabled	3.1	3.4	—	
		8 MHz	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = off, All peripherals enabled	2.5	2.7	—	
			V_{DD} = 5.0 V, HSI = 8 MHz, PLL = off, All peripherals disabled	1.3	1.5	—	
		32 kHz	V_{DD} = 5.0 V, LSI = 32 kHz, LDO off, ULDO on, All peripherals enabled	16.3	19.6	—	μA
			V_{DD} = 5.0 V, LSI = 32 kHz, LDO off, ULDO on, All peripherals disabled	11.8	14.9	—	

Symbol	Parameter	f_{HCLK}	Conditions	Typ.	Max. @ T_A 25 °C	Max. @ T_A 85 °C	Unit
I_{DD}	Supply Current (Sleep Mode)	60 MHz	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, All peripherals enabled	9.9	10.8	—	mA
			V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, All peripherals disabled	1.1	1.2	—	
		40 MHz	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, All peripherals enabled	6.8	7.4	—	
			V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, All peripherals disabled	0.81	0.91	—	
		20 MHz	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 20 MHz, All peripherals enabled	3.8	4.1	—	
			V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 20 MHz, All peripherals disabled	0.67	0.77	—	
		8 MHz	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = off, All peripherals enabled	1.6	1.7	—	
			V_{DD} = 5.0 V, HSI = 8 MHz, PLL = off, All peripherals disabled	0.32	0.39	—	
	Supply Current (Deep-Sleep1 Mode)	—	V_{DD} = 5.0 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC on	7.66	10.3	—	μA
	Supply Current (Deep-Sleep2 Mode)	—	V_{DD} = 5.0 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC on	7.63	10.27	—	μA

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
3. RTC means real-time clock.
4. Code = while (1) {208 NOP} executed in Flash.

Table 13. HT32F54243/HT32F54253 Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	f_{HCLK}	Conditions	Typ.	Max. @ T_A 25 °C	Max. @ T_A 85 °C	Unit
I_{DD}	Supply Current (Run Mode)	60 MHz	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, All peripherals enabled	18.4	21	—	mA
			V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, All peripherals disabled	7.4	8.1	—	
		40 MHz	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, All peripherals enabled	14.7	16.5	—	
			V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, All peripherals disabled	7.2	7.8	—	
		20 MHz	V_{DD} = 5.0 V, HSI = 8 MHz,PLL = 20 MHz, All peripherals enabled	7.4	8.1	—	
			V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 20 MHz, All peripherals disabled	3.5	3.8	—	
		8 MHz	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = off, All peripherals enabled	3.1	3.3	—	
			V_{DD} = 5.0 V, HSI = 8 MHz, PLL = off, All peripherals disabled	1.5	1.6	—	
		32 kHz	V_{DD} = 5.0 V, LSI = 32 kHz, LDO off, ULDO on, All peripherals enabled	19.2	23.8	—	μA
			V_{DD} = 5.0 V, LSI = 32 kHz, LDO off, ULDO on, All peripherals disabled	12.9	17.2	—	

Symbol	Parameter	f_{HCLK}	Conditions	Typ.	Max. @ T_A		Unit
					25 °C	85 °C	
I_{DD}	Supply Current (Sleep Mode)	60 MHz	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, All peripherals enabled	13.2	14.7	—	mA
			V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, All peripherals disabled	1.1	1.2	—	
		40 MHz	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, All peripherals enabled	9.1	10	—	
			V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, All peripherals disabled	0.86	0.94	—	
		20 MHz	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 20 MHz, All peripherals enabled	5	5.4	—	
			V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 20 MHz, All peripherals disabled	0.72	0.79	—	
		8 MHz	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = off, All peripherals enabled	2.1	2.2	—	
			V_{DD} = 5.0 V, HSI = 8 MHz, PLL = off, All peripherals disabled	0.33	0.36	—	
	Supply Current (Deep-Sleep1 Mode)	—	V_{DD} = 5.0 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC on	8.15	12.28	—	μA
	Supply Current (Deep-Sleep2 Mode)	—	V_{DD} = 5.0 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC on	8.13	12.26	—	μA

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
3. RTC means real-time clock.
4. Code = while (1) {208 NOP} executed in Flash.

Reset and Supply Monitor Characteristics

Table 14. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{POR}	Power On Reset Threshold (Rising Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	2.22	2.35	2.48	V
V_{PDR}	Power Down Reset Threshold (Falling Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	2.12	2.20	2.33	V
$V_{PORHYST}$	POR Hysteresis	—	—	150	—	mV
t_{POR}	Reset Delay Time	V_{DD} = 5.0 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.
2. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO will be turned off.

Table 15. LVD/BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown Out Detection	After factory-trimmed, V_{DD} Falling edge		2.37	2.45	2.53	V
V_{LVD}	Voltage of Low Voltage Detection	V_{DD} Falling edge	LVDS = 000	2.57	2.65	2.73	V
			LVDS = 001	2.77	2.85	2.93	V
			LVDS = 010	2.97	3.05	3.13	V
			LVDS = 011	3.17	3.25	3.33	V
			LVDS = 100	3.37	3.45	3,53	V
			LVDS = 101	4.15	4.25	4.35	V
			LVDS = 110	4.35	4.45	4.55	V
			LVDS = 111	4.55	4.65	4.75	V
$V_{LVDHTST}$	LVD Hysteresis	V_{DD} = 5.0 V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 5.0 V	—	—	—	5	μs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 5.0 V	—	—	—	—	ms
I_{DDLVD}	Operation Current(2)	V_{DD} = 5.0 V	—	—	10	20	μA

Note: 1. Data based on characterization results only, not tested in production.
2. Bandgap current is not included.
3. The LVDS field is in the PWRCU LVDCSR register.

External Clock Characteristics

Table 16. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{CK_HSE}	HSE Frequency	V_{DD} = 2.5 V ~ 5.0 V	4	—	16	MHz
C_L	Load Capacitance	V_{DD} = 5.0 V, R_{ESR} = 100 Ω, @ 16 MHz	—	—	12	pF
R_{FHSE}	Internal Feedback Resistor between XTALIN and XTALOUT pins	V_{DD} = 5.0 V	—	0.5	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 5.0 V, C_L = 12 pF @ 16 MHz, HSEGAIN = 0	—	—	110	Ω
		V_{DD} = 2.5 V, C_L = 12 pF @ 16 MHz, HSEGAIN = 1				
D_{HSE}	HSE Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	V_{DD} = 5.0 V, R_{ESR} = 100 Ω, C_L = 12 pF @ 8 MHz, HSEGAIN = 0	—	0.85	—	mA
		V_{DD} = 5.0 V, R_{ESR} = 25 Ω, C_L = 12 pF @ 16 MHz, HSEGAIN = 1	—	3.0	—	
I_{PWDHSE}	HSE Oscillator Power Down Current	V_{DD} = 5.0 V	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	V_{DD} = 5.0 V	—	—	4	ms

Table 17. Low Speed External Clock (LSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{CK_LSE}	LSE Frequency	V_{DD} = 2.5 V ~ 5.5 V	—	32.768	—	kHz
R_F	Internal feedback resistor	—	—	10	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 5.0 V	30	—	TBD	kΩ
C_L	Recommended load capacitances	V_{DD} = 5.0 V	6	—	TBD	pF
I_{DDLSE}	Oscillator Supply Current (High Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, C_L ≥ 7 pF, V_{DD} = 2.5 V ~ 5.5 V T_A = -40 °C ~ 85 °C	—	3.3	6.3	μA
	Oscillator Supply Current (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, C_L < 7 pF, V_{DD} = 2.5 V ~ 5.5 V T_A = -40 °C ~ 85 °C	—	1.8	3.3	μA
	Power Down Current	—	—	—	0.01	μA
t_{SULSE}	LSE Oscillator Startup Time (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, V_{DD} = 2.5 V ~ 5.5 V	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE / LSE clock in the PCB layout.

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace length as short as possible to reduce the parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep the high frequency signal lines away from the crystal area to prevent the crosstalk adverse effects.

Internal Clock Characteristics

Table 18. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{HSI}	HSI Frequency	V_{DD} = 5 V @ 25 °C	—	8	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V_{DD} = 5.0 V, T_A = 25 °C	-2	—	2	%
		V_{DD} = 2.5 V ~ 5.5 V T_A = -40 °C ~ 85 °C	-3	—	3	%
Duty	Duty Cycle	f_{HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	Oscillator Supply Current	f_{HSI} = 8 MHz @ V_{DD} = 2.5 V ~ 5.5 V	—	—	140	μA
	Power Down Current		—	—	0.01	μA
T_{SUHSI}	HSI Oscillator Startup time	f_{HSI} = 8 MHz	—	—	20	μs

Table 19. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{LSI}	LSI Frequency	V_{DD} = 5.0 V, T_A = -40 °C ~ 85 °C	21	32	43	kHz
ACC_{LSI}	LSI Frequency Accuracy	V_{DD} = 5.0 V, with factory-trimmed	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 5.0 V	—	0.5	0.8	μA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 5.0 V	—	—	100	μs

System PLL Characteristics

Table 20. System PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	System PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	System PLL Output Clock	—	16	—	60	MHz
t_{LOCK}	System PLL Lock Time	—	—	200	—	μs

Memory Characteristics

Table 21. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program / Erase Cycles before Failure (Endurance)	T_A = -40 °C ~ 85 °C	20	—	—	K Cycles
t_{RET}	Data Retention Time	T_A = -40 °C ~ 85 °C	10	—	—	Years
t_{PROG}	Word Programming Time	T_A = -40 °C ~ 85 °C	20	—	—	μs
t_{ERASE}	Page Erase Time	T_A = -40 °C ~ 85 °C	2	—	—	ms
t_{MERASE}	Mass Erase Time	T_A = -40 °C ~ 85 °C	10	—	—	ms

I/O Port Characteristics

Table 22. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	5.0 V I/O	$V_I = V_{SS}$, On-chip pull-up resister disabled	—	—	3	μA
		Reset pin		—	—	3	μA
I_{IH}	High Level Input Current	5.0 V I/O	$V_I = V_{DD}$, On-chip pull-down resister disabled	—	—	3	μA
		Reset pin		—	—	3	μA
V_{IL}	Low Level Input Voltage	5.0 V I/O		- 0.5	—	V_{DD} × 0.35	V
		Reset pin		- 0.5	—	V_{DD} × 0.35	V
V_{IH}	High Level Input Voltage	5.0 V I/O		V_{DD} × 0.65	—	V_{DD} + 0.5	V
		Reset pin		V_{DD} × 0.65	—	V_{DD} + 0.5	V
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	5.0 V I/O		—	0.12 × V_{DD}	—	mV
		Reset pin		—	0.12 × V_{DD}	—	mV
I_{OL}	Low Level Output Current (GPIO Sink Current)	5.0 V I/O 4 mA drive, V_{OL} = 0.6 V		4	—	—	mA
		5.0 V I/O 8 mA drive, V_{OL} = 0.6 V		8	—	—	mA
		5.0 V I/O 12 mA drive, V_{OL} = 0.6 V		12	—	—	mA
		5.0 V I/O 16 mA drive, V_{OL} = 0.6 V		16	—	—	mA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{OH}	High Level Output Current (GPIO Source Current)	5.0 V I/O 4 mA drive, V_{OH} = V_{DD} - 0.6 V	—	4	—	mA
		5.0 V I/O 8 mA drive, V_{OH} = V_{DD} - 0.6 V	—	8	—	mA
		5.0 V I/O 12 mA drive, V_{OH} = V_{DD} - 0.6 V	—	12	—	mA
		5.0 V I/O 16 mA drive, V_{OH} = V_{DD} - 0.6 V	—	16	—	mA
V_{OL}	Low Level Output Voltage	5.0 V 4 mA drive I/O, I_{OL} = 4 mA	—	—	0.6	V
		5.0 V 8 mA drive I/O, I_{OL} = 8 mA	—	—	0.6	V
		5.0 V 12 mA drive I/O, I_{OL} = 12 mA	—	—	0.6	V
		5.0 V 16 mA drive I/O, I_{OL} = 16 mA	—	—	0.6	V
V_{OH}	High Level Output Voltage	5.0 V 4 mA drive I/O, I_{OH} = 4 mA	V_{DD} - 0.6	—	—	V
		5.0 V 8 mA drive I/O, I_{OH} = 8 mA	V_{DD} - 0.6	—	—	V
		5.0 V 12 mA drive I/O, I_{OH} = 12 mA	V_{DD} - 0.6	—	—	V
		5.0 V 16 mA drive I/O, I_{OH} = 16 mA	V_{DD} - 0.6	—	—	V
R_{PU}	Internal Pull-up Resistor	V_{DD} = 5.0 V	—	50	—	kΩ
		V_{DD} = 3.3 V	—	76	—	
R_{PD}	Internal Pull-down Resistor	V_{DD} = 5.0 V	—	50	—	kΩ
		V_{DD} = 3.3 V	—	76	—	

ADC Characteristics

Table 23. ADC Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—	2.5	5.0	5.5	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference Voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	A/D Converter Current Consumption	V_{DDA} = 5.0 V, 1 Msps	—	1.4	1.5	mA
I_{ADC_DN}	A/D Converter Power Down Current Consumption	V_{DDA} = 5.0 V	—	—	0.1	μA
f_{ADC}	A/D Converter Clock Frequency	—	0.7	—	16.0	MHz
f_S	Sampling Rate	—	0.05	—	1.00	Msps
t_{DL}	Data Latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & Hold Time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter Conversion Time	ADST[7:0] = 2	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C_I	Input Sampling Capacitance	No pin/pad capacitance included	—	4	—	pF
t_{SU}	Start Up Time	—	—	—	1	μs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N	Resolution	—	—	12	—	bits
INL	Integral Non-linearity Error	f_S = 750 ksps, V_{DDA} = 5.0 V	—	±2	±5	LSB
DNL	Differential Non-linearity Error	f_S = 750 ksps, V_{DDA} = 5.0 V	—	±1	—	LSB
E_O	Offset Error	—	—	—	±10	LSB
E_G	Gain Error	—	—	—	±10	LSB

Note: 1. Data based on characterization results only, not tested in production.

2. Due to the A/D Converter input channel and GPIO pin-shared function design limitation, the V_{DDA} supply power of the A/D Converter has to be equal to the V_{DD} supply power of the MCU in the application circuit.

3. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.

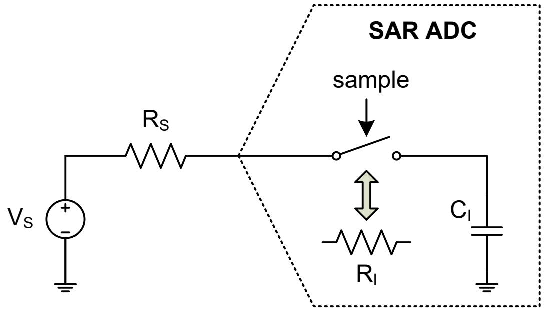


Figure 11. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0 V and V_{REF}) are sampled consecutively. In this situation a sampling error below 1/4 LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

Internal Reference Voltage Characteristics

Table 24. Internal Reference Voltage Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—		2.5	—	5.5	V
V_{REF}	Internal Reference Voltage after Factory Trimming @ T_A = 25 °C	V_{DDA} ≥ 2.8 V	VREFSEL[1:0] = 00	2.44	2.50	2.56	V
		V_{DDA} ≥ 3.3 V	VREFSEL[1:0] = 01	2.92	3.00	3.08	
		V_{DDA} ≥ 4.3 V	VREFSEL[1:0] = 10	3.90	4.00	4.10	
		V_{DDA} ≥ 4.8 V	VREFSEL[1:0] = 11	4.39	4.50	4.61	
ACC_{VREF}	Reference Voltage Accuracy after Trimming	V_{DDA} = 2.5 V ~ 5.5 V, V_{REF} = 0.809 V, T_A = -40 °C ~ 85 °C		-2	—	+2	%
t_{STABLE}	Reference Voltage Stable Time	—		—	—	100	ms
t_{SREFV}	ADC Sampling Time when Reading Reference Voltage	—		10	—	—	μs
I_{DD}	Operating Current	—		—	50	70	μA
I_{DDPWD}	Power Down Current	—		—	—	0.01	μA

Note: 1. Data based on characterization results only, not tested in production.
2. The trimming bits of the internal reference voltage are 6-bit resolution.

Comparator Characteristics

Table 25. Comparator Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	Comparator mode		2.5	—	5.5	V
V_{IN}	Input Common Mode Voltage Range	CPn or CNn		V_{SSA}	—	V_{DDA}	V
V_{IOS}	Input Offset Voltage(Note)	—		-5	—	5	mV
V_{HYS}	Input Hysteresis V_{DDA} = 5.0 V	No hysteresis, CMPHM [1:0] = 00		—	0	—	mV
		Low hysteresis, CMPHM [1:0] = 01		—	50	—	mV
		Middle hysteresis, CMPHM [1:0] = 10		—	100	—	mV
		High hysteresis, CMPHM [1:0] = 11		—	150	—	mV
t_{RT}	Response Time Input Overdrive = ±100 mV	High Speed Mode	V_{DDA} ≥ 3.6 V	—	50	100	ns
			V_{DDA} < 3.6 V	—	100	250	
		Low Speed Mode		—	2	5	μs
I_{CMP}	Current Consumption V_{DDA} = 5.0 V	High Speed Mode		—	150	—	μA
		Low Speed Mode		—	10	—	μA
t_{CMPST}	Comparator Startup Time	Comparator enabled to output valid		—	—	50	μs
I_{CMP_DN}	Comparator Power Down Supply Current	CMPEN = 0, CVREN = 0, CVROE = 0		—	—	0.1	μA
Comparator Voltage Reference (CVR)							
V_{CVR}	Output Range	—		V_{SSA}	—	V_{DDA}	V
N_{Bits}	CVR Scaler Resolution	—		—	8	—	bits

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{CVRST}	Setting Time	V_{DDA} = 3.3 V, CVREFOE = 1, C_{LOAD} ≤ 100 pF, R_{LOAD} ≥ 50 kΩ CVR Scaler Setting Time from CVRVAL = “00000000” to “11111111”	—	—	250	µs
I_{CVR}	Current Consumption V_{DDA} = 5.0 V	CVREN = 1, CVROE =0	—	100	—	µA
		CVREN = 1, CVROE = 1	—	125	150	µA

Note: Data based on characterization results only, not tested in production.

GPTM/MCTM/SCTM Characteristics

Table 26. GPTM/MCTM/SCTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for GPTM, MCTM and SCTM	—	—	—	f_{PCLK}	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	$1/f_{TM}$
f_{EXT}	External Signal Frequency on Channel 0 ~ 3	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	bits

I²C Characteristics

Table 27. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.500	—	1.125	—	0.450	—	µs
$t_{SCL(L)}$	SCL Clock Low Time	4.500	—	1.125	—	0.450	—	µs
t_{FALL}	SCL and SDA Fall Time	—	1.300	—	0.340	—	0.135	µs
t_{RISE}	SCL and SDA Rise Time	—	1.300	—	0.340	—	0.135	µs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time(5)	0	—	0	—	0	—	ns
	SDA Data Hold Time(6)	—	1.600	—	0.475	—	0.250	µs
$t_{VD(SDA)}$	SDA Data Valid Time	—	1.600	—	0.475	—	0.250	µs
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Data based on characterization results only, not tested in production.
2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast plus mode, the peripheral clock frequency must be higher than 20 MHz.
5. This characteristic parameter of the I²C bus timing is based on: COMBFILTEREN = 0 and SEQFILTER = 00.
6. This characteristic parameter of the I²C bus timing is based on: COMBFILTEREN = 1 and SEQFILTER = 00.

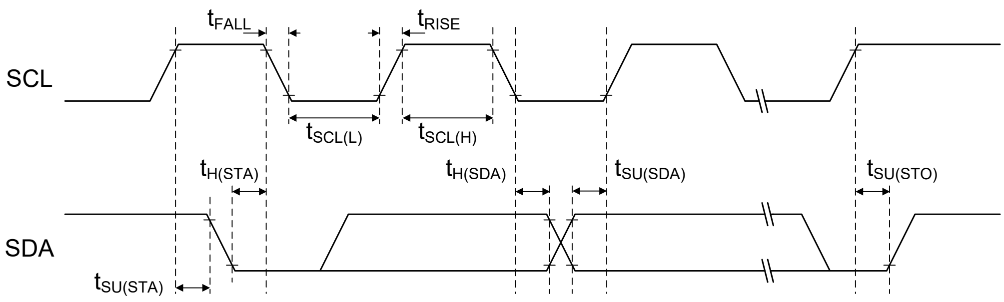


Figure 12. I²C Timing Diagram

SPI Characteristics

Table 28. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK}	SPI Master Output SCK Clock Frequency	Master mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High or Low Time	—	$t_{SCK}/2$ - 2	—	$t_{SCK}/2$ + 1	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
f_{SCK}	SPI Slave Input SCK Clock Frequency	Slave mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	3 t_{PCLK}	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	2 t_{PCLK}	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	3 t_{PCLK}	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

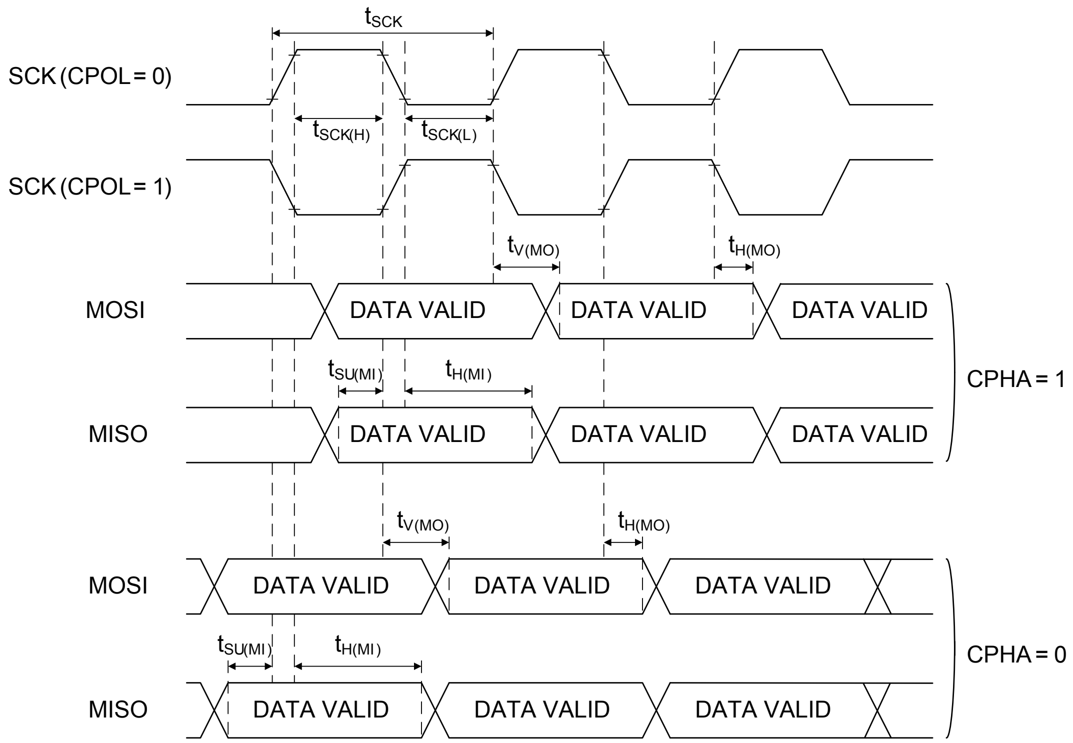


Figure 13. SPI Timing Diagrams – SPI Master Mode

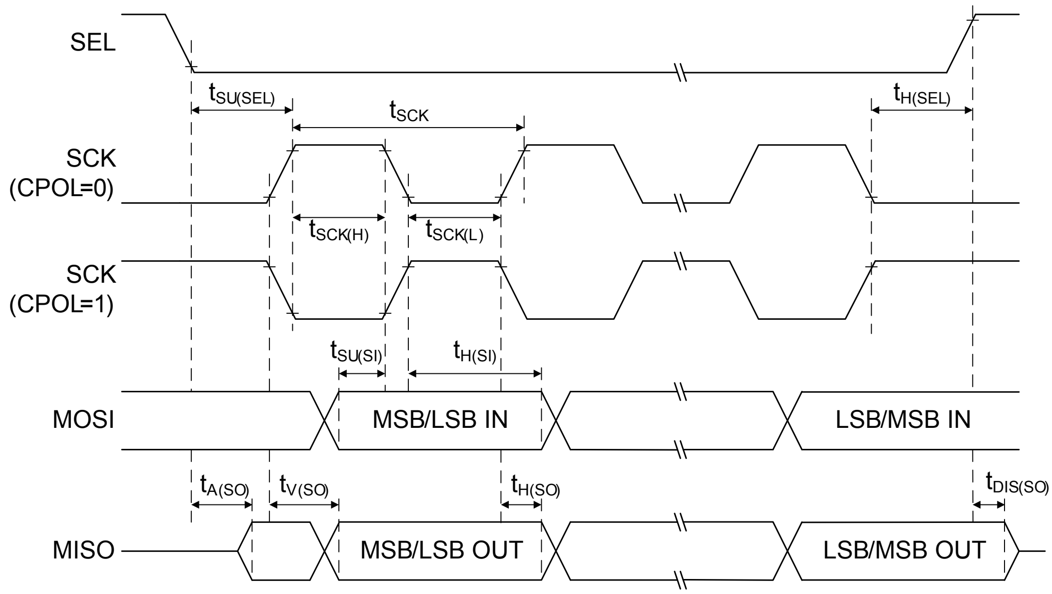


Figure 14. SPI Timing Diagrams – SPI Slave Mode with CPHA = 1

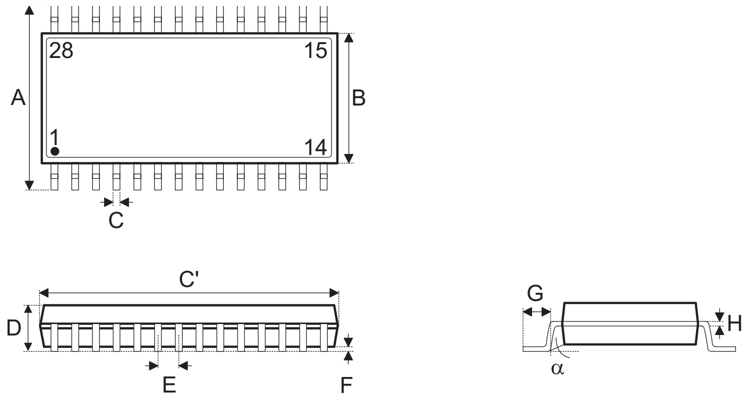
6 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

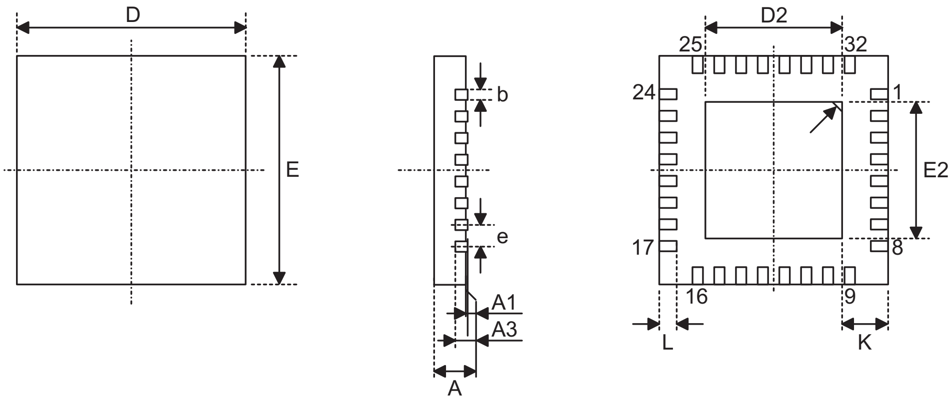
28-pin SSOP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.236 BSC	
B		0.154 BSC	
C	0.008	—	0.012
C’		0.390 BSC	
D	—	—	0.069
E		0.025 BSC	
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		6.00 BSC	
B		3.90 BSC	
C	0.20	—	0.30
C’		9.90 BSC	
D	—	—	1.75
E		0.635 BSC	
F	0.10	—	0.25
G	0.41	—	1.27
H	0.10	—	0.25
α	0°	—	8°

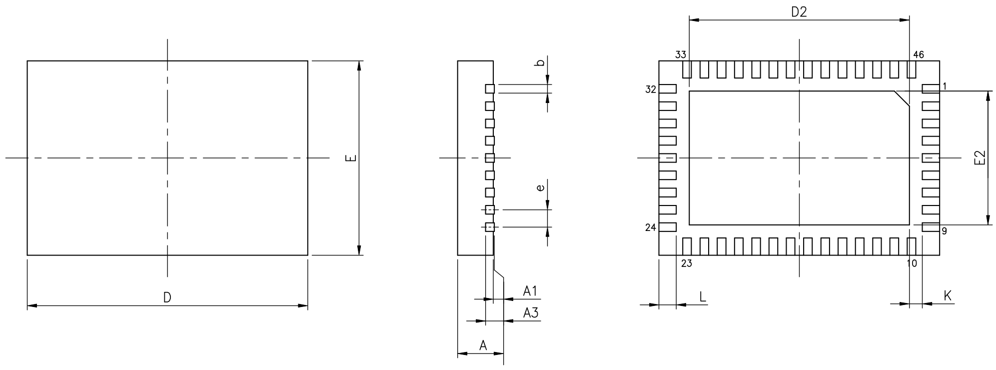
SAW Type 32-pin QFN (4mm × 4mm × 0.75mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3		0.008 REF	
b	0.006	0.008	0.010
D		0.157 BSC	
E		0.157 BSC	
e		0.016 BSC	
D2	0.100	—	0.108
E2	0.100	—	0.108
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
D2	2.55	—	2.75
E2	2.55	—	2.75
L	0.35	0.40	0.45
K	0.20	—	—

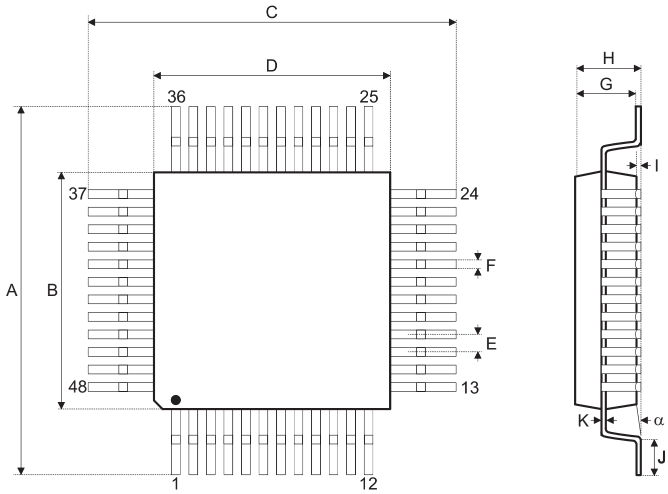
SAW Type 46-pin QFN (6.5mm × 4.5mm × 0.75mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3		0.008 REF	
b	0.006	0.008	0.010
D		0.256 BSC	
E		0.177 BSC	
e		0.016 BSC	
D2	0.197	—	0.205
E2	0.118	—	0.126
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.15	0.20	0.25
D		6.50 BSC	
E		4.50 BSC	
e		0.40 BSC	
D2	5.00	—	5.20
E2	3.00	—	3.20
L	0.35	0.40	0.45
K	0.20	—	—

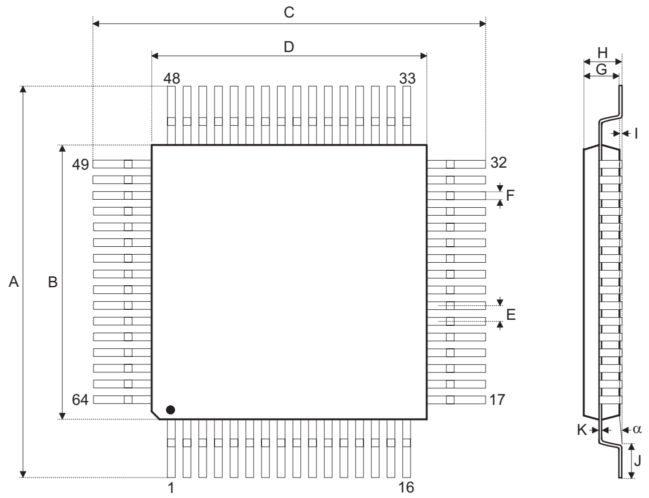
48-pin LQFP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.354 BSC	
B		0.276 BSC	
C		0.354 BSC	
D		0.276 BSC	
E		0.020 BSC	
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		9.00 BSC	
B		7.00 BSC	
C		9.00 BSC	
D		7.00 BSC	
E		0.50 BSC	
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

64-pin LQFP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.354 BSC	
B		0.276 BSC	
C		0.354 BSC	
D		0.276 BSC	
E		0.016 BSC	
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		9.00 BSC	
B		7.00 BSC	
C		9.00 BSC	
D		7.00 BSC	
E		0.40 BSC	
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°