



HT32F52342/HT32F52352 Datasheet

**32-Bit Arm® Cortex®-M0+ Microcontroller,
up to 128 KB Flash and 16 KB SRAM with 1 Msps ADC, USART,
UART, SPI, I²C, I²S, MCTM, GPTM, BFTM, SCI, CRC, RTC, WDT,
PDMA, EBI and USB2.0 FS**

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1 General Description

The Holtek HT32F52342/52352 devices are high performance, low power consumption 32-bit microcontrollers based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The devices operate at a frequency of up to 48 MHz with a Flash accelerator to obtain maximum efficiency. It provides up to 128 KB of embedded Flash memory for code/data storage and 16 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, I²C, USART, UART, SPI, I²S, GPTM, MCTM, SCI, CRC-16/32, RTC, WDT, PDMA, EBI, USB2.0 FS, SW-DP (Serial Wire Debug Port), etc., are also implemented in the device series. Several power saving modes provide the flexibility for maximum optimisation between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the devices are suitable for use in a wide range of applications, especially in areas such as white goods application control, power monitors, alarm systems, consumer products, handheld equipment, data logging applications, motor control and so on.

arm CORTEX

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 48 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O ports, hardware multiplier and low latency interrupt respond time.

On-Chip Memory

- Up to 128 KB on-chip Flash memory for instruction/data and option byte storage
- 16 KB on-chip SRAM
- Supports multiple boot modes

The Arm® Cortex®-M0+ processor accesses and debug accesses share the single external interface to external AHB peripherals. The processor access takes priority over debug access. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 shows the memory map of the HT32F52342/52352 series of devices, including code, SRAM, peripheral, and other pre-defined regions.

Flash Memory Controller – FMC

- Flash accelerator for maximum efficiency
- 32-Bit word programming with In System Programming (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer and cache are provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor:
 - Power On Reset / Power Down Reset – POR/PDR
 - Brown-out Detector – BOD
 - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by an external signal, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- External 32,768 Hz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to $\pm 2\%$ accuracy at 3.3V operating voltage and 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Integrated system clock PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), a HSE clock monitor, clock prescalers, clock multiplexers, APB clock divider and gating circuitry. The AHB, APB and Cortex®-M0+ clocks are derived from the system clock (CK_SYS) which can come from the LSI, LSE, HSI, HSE or PLL. The Watchdog Timer and Real-Time Clock (RTC) use either the LSI or LSE as their clock source.

Power Management – PWRCU

- Single V_{DD} power supply: 2.0 V to 3.6 V
- Integrated 1.5 V LDO regulator for MCU core, peripherals and memories power supply
- V_{BAT} battery power supply for RTC and backup registers
- Three power domains: V_{DD} , V_{CORE} and Backup
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Power-Down

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in these devices provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down modes. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge, or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 12 external analog input channels

A 12-bit multi-channel ADC is integrated in the device. There are multiplexed channels, which include 12 external analog signal channels and 2 internal channels which can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function

will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset thresholds. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

Analog Comparator – CMP

- Rail-to-rail comparator
- Each comparator has configurable negative inputs used for flexible voltage selection
- Dedicated I/O pins or internal voltage reference provided by 6-bit scaler
- Programmable hysteresis
- Programming response speed and power consumption
- Comparator output can be routed to I/O pin or to multiple timers or ADC trigger input
- 6-bit scaler can be configurable to dedicated I/O for voltage reference
- Interrupt generation capability with wakeup from Sleep or Deep Sleep modes through the EXTI controller

Two general purpose comparators (CMP) are implemented within the device. They can be configured either as standalone comparators or combined with the different kinds of peripheral IPs. Each comparator is capable of asserting interrupts to the NVIC or waking up the MCU from Sleep or Deep Sleep modes through the EXTI wakeup event management unit.

I/O Ports – GPIO

- Up to 51 GPIOs
- Port A, B, C, D are mapped as 16 external interrupts – EXTI
- Almost all I/O pins have a configurable output driving current.

There are up to 51 General Purpose I/O pins, GPIO, named from PA0~PA15, PB0 ~ PB8, PB10 ~ PB15. PC0 ~ PC15 and PD0~PD3 for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximise flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

Motor Control Timer – MCTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Supports 3-phase motor control and hall sensor interface
- Break input to force the timer's output signals into a reset or fixed condition

The Motor Control Timer Module, MCTM, consists of a single 16-bit up/down counter, four 16-bit CCRs (Capture/Compare Registers), single one 16-bit counter-reload register (CRR), single 8-bit repetition counter and several control/status registers. It can be used for a variety of purposes including measuring the pulse widths of input signals or generating output waveforms such as compare match outputs, PWM outputs or complementary PWM outputs with dead-time insertion. The MCTM is capable of offering full functional support for motor control, hall sensor interfacing and brake input.

General-Purpose Timer – GPTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels for each timer
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General Purpose Timer Module, GPTM, consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control / status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation, or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

Single Channel Timer – SCTM

- 16-bit auto-reload up-counter
- One channel for each timer
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned

The Single-Channel Timer Module, SCTM, consists of one 16-bit up-counter, one 16-bit Capture / Compare Register (CCR), one 16-bit Counter-Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as PWM output.

Basic Function Timer – BFTM

- One 32-Bit compare / match count-up counter – no I/O control
- One shot mode – counting stops after a match condition
- Repetitive mode – counter restarts when compare match occurs

The Basic Function Timer Module, BFTM, is a simple 32-bit up-counting counter designed to measure time intervals and generate a one shot or repetitive interrupts. The BFTM can operate in two modes, repetitive and one shot modes. In the repetitive mode, the counter will restart at each compare match event. The BFTM also supports a one shot mode which will force the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-Bit down counter with 3-bit prescaler
- Provides reset to the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect a system lock-up due to software trapped in a deadlock. It includes a 12-bit count-down counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter before it reaches a delta value. This means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. The register write protect function which can be enabled to prevent an unexpected change in the Watchdog timer configuration.

Real-Time Clock – RTC

- 32-Bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real-Time Clock, RTC, includes an APB interface, a 32-bit count-up counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the Backup Domain except for the APB interface. The APB interface is located in the V_{CORE} power domain. Therefore, it is necessary to be isolated from the ISO signal that comes from the power control unit when the V_{CORE} power domain is powered off, that is when the device enters the Power-Down mode. The RTC counter is used as a wakeup timer to generate a system resume signal from the Power-Down mode.

Inter-integrated Circuit – I²C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronisation
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode with maskable address

The I²C is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I²C bus is a bi-directional data line between the master and slave devices and is used for data transmission and reception. The I²C also has an arbitration detect function and clock synchronisation to prevent situations where more than one master attempts to transmit data to the I²C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave modes
- Frequency of up to ($f_{PCLK}/2$) MHz for the master mode and ($f_{PCLK}/3$) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave mode. The SPI interface uses 4 pins, which are the serial data input and output lines, MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Programmable baud rate clock frequency up to ($f_{PCLK}/16$) MHz for Asynchronous mode and ($f_{PCLK}/8$) MHz for synchronous mode
- Full duplex communication
- Fully programmable serial communication characteristics including:
 - Word length: 7, 8, or 9-bit character
 - Parity: Even, odd, or no-parity bit generation and detection
 - Stop bit: 1 or 2 stop bit generation
 - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8-level for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous data transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes a transmitter FIFO, (TX_FIFO) and receiver FIFO (RX_FIFO). The software can detect a USART error status by reading the USART Status & Interrupt Flag Register, USRSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to ($f_{PCLK}/16$) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
 - Word length: 7, 8, or 9-bit character
 - Parity: Even, odd, or no-parity bit generation and detection
 - Stop bit: 1 or 2 stop bit generation
 - Bit order: LSB-first or MSB-first transfer

- Error detection: Parity, overrun, and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Smart Card Interface – SCI

- Supports ISO 7816-3 standard
- Character Transfer mode
- Single transmit buffer and single receive buffer
- 11-bit ETU (elementary time unit) counter
- 9-bit guard time counter
- 24-bit general purpose waiting time counter
- Parity generation and checking
- Automatic character retry on parity error detection in transmission and reception modes

The Smart Card Interface is compatible with the ISO 7816-3 standard. This interface includes Card Insertion/Removal detection, SCI data transfer control logic and data buffers, internal Timer Counters and corresponding control logic circuits to perform all the necessary Smart Card operations. The Smart Card interface acts as a Smart Card Reader to facilitate communication with the external Smart Card. The overall functions of the Smart Card interface are controlled by a series of registers including control and status registers together with several corresponding interrupts which are generated to get the attention of the microcontroller for SCI transfer status.

Inter-IC Sound – I²S

- Master or slave mode
- Mono and stereo
- I²S-justified, Left-justified and Right-justified mode
- 8/16/24/32-bit sample size with 32-bit channel extended
- 8 × 32-bit TX & RX FIFO with PDMA supported
- 8-bit Fractional Clock Divider with rate control

The I²S is a synchronous communication interface that can be used as a master or slave to exchange data with other audio peripherals, such as ADCs or DACs. The I²S supports a variety of data formats. In addition to the stereo I²S-justified, Left-justified and Right-justified modes, there are mono PCM modes with 8/16/24/32-bit sample size. When the I²S operates in the master mode, then when using the fractional divider, it can provide an accurate sampling frequency output and support the rate control function and fine-tuning of the output frequency to avoid system problems caused by the cumulative frequency error between different devices.

Cyclic Redundancy Check – CRC

- Supports CRC16 polynomial: 0x8005,
 $X^{16} + X^{15} + X^2 + 1$
- Supports CCITT CRC16 polynomial: 0x1021,
 $X^{16} + X^{12} + X^5 + 1$
- Supports IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
 $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Supports PDMA to complete a CRC computation of a block of memory

The CRC calculation unit is an error detection technique test algorithm which is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16- or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, then this means that the data stream contains a data error.

Peripheral Direct Memory Access – PDMA

- 6 channels with trigger source grouping
- 8-/16-/32-bit width data transfer
- Supports Linear address, circular address and fixed address modes
- 4-level programmable channel priority
- Auto reload mode
- Supports trigger source: ADC, SPI, USART, UART, I²C, I²S, GPTM, MCTM, SCI and software request

The Peripheral Direct Memory Access controller, PDMA, moves data between the peripherals and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt service routine execution. It improves system performance as the software does not need to connect each data movement operation.

External Bus Interface – EBI

- Programmable interface for various memory types
- Translate the AHB transactions into the appropriate external device protocol
- Individual chip select signal for per memory bank
- Programmable timing to support a wide range of devices
- Automatic translation when AHB transaction width and external memory interface width is different
- Write buffer to decrease the stalling of the AHB write burst transaction
- Multiplexed and non-multiplexed address and data line configurations
 - Up to 21 address lines
 - Up to 16-bit data bus width

The external bus interface is able to access external parallel interface devices such as SRAM, Flash and LCD modules. The interface is memory mapped into the CPU internal address map. The data and address lines are multiplexed in order to reduce the number of pins required to connect to the external devices. The read/write timing of the bus can be adjusted to meet the timing specification of the external devices. Note the interface only supports asynchronous 8 or 16-bit bus interface.

Universal Serial Bus Device Controller – USB

- Complies with USB 2.0 full-speed (12 Mbps) specification
- On-chip USB full-speed transceiver
- 1 control endpoint (EP0) for control transfer
- 3 single-buffered endpoints for bulk and interrupt transfer
- 4 double-buffered endpoints for bulk, interrupt and isochronous transfer
- 1,024 bytes EP_SRAM used as the endpoint data buffers

The USB device controller is compliant with the USB 2.0 full-speed specification. There is one control endpoint known as Endpoint 0 and seven configurable endpoints. A 1024-byte EP_SRAM is used as the endpoint buffer. Each endpoint buffer size is programmable using corresponding registers, which provides maximum flexibility for various applications. The integrated USB full-speed transceiver helps to minimise the overall system complexity and cost. The USB functional block also contains the resume and suspend feature to meet the requirements of low-power consumption.

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watchpoints

Package and Operation Temperature

- 33-pin QFN, 48/64-pin LQFP packages
- Operation temperature range: -40 °C to 85 °C

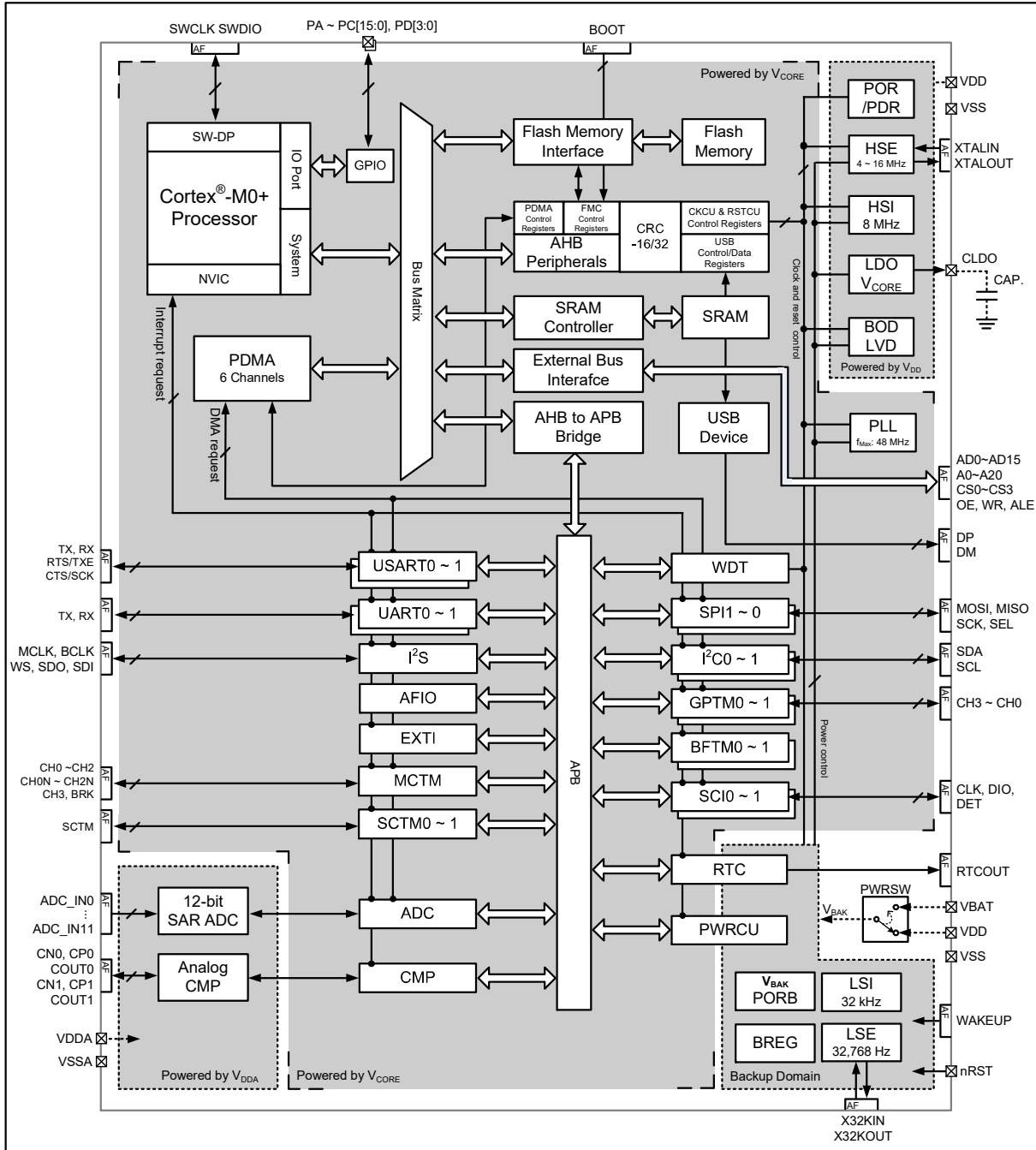
3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F52342	HT32F52352
Main Flash (KB)		64	127.5
Option Bytes Flash (KB)		0.5	0.5
SRAM (KB)		8	16
Timers	MCTM		1
	GPTM		2
	SCTM		2
	BFTM		2
	RTC		1
	WDT		1
Communication	USB		1
	SPI		2
	USART		2
	UART		2
	I ² C		2
	I ² S		1
	SCI (ISO7816-3)		2
EBI			1
CRC-16/32			1
GPIO			Up to 51
EXTI			16
12-bit ADC			1
Number of channels			12 External Channels
Comparator			2
CPU frequency			Up to 48 MHz
Operating voltage			2.0 V ~ 3.6 V
Operating temperature			-40 °C ~ 85 °C
Package			33-pin QFN, 48/64-pin LQFP

Block Diagram



Power supply:
 Bus:
 Control signal:
 Alternate function:

Figure 1. Block Diagram

Memory Map

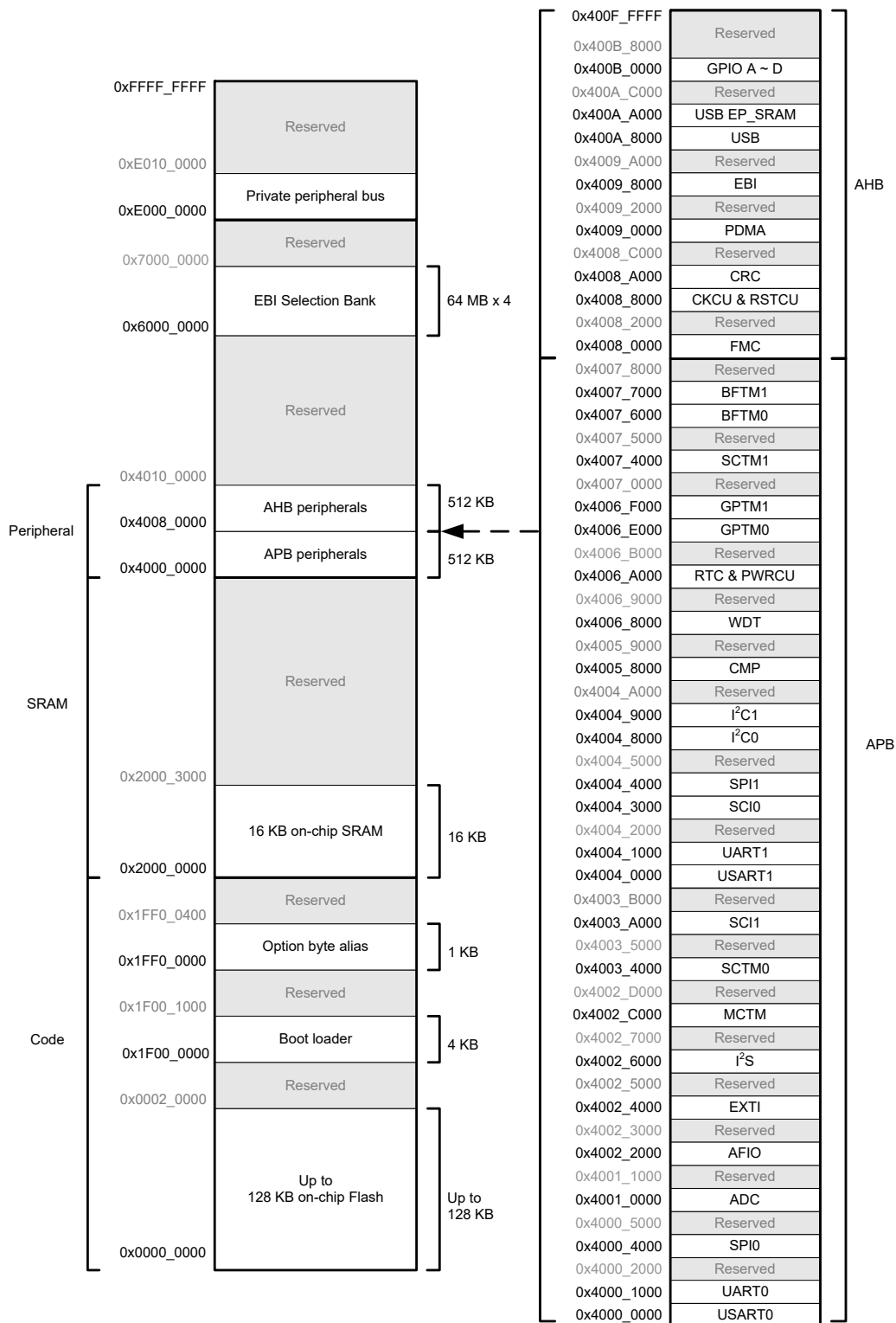


Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART0	APB
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI0	
0x4000_5000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4002_5FFF	Reserved	
0x4002_6000	0x4002_6FFF	I ² S	
0x4002_7000	0x4002_BFFF	Reserved	
0x4002_C000	0x4002_CFFF	MCTM	
0x4002_D000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4003_9FFF	Reserved	
0x4003_A000	0x4003_AFFF	SCI1	
0x4003_B000	0x4004_0FFF	Reserved	
0x4004_0000	0x4004_0FFF	USART1	
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_2FFF	Reserved	
0x4004_3000	0x4004_3FFF	SCI0	
0x4004_4000	0x4004_4FFF	SPI1	
0x4004_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I ² C0	
0x4004_9000	0x4004_9FFF	I ² C1	
0x4004_A000	0x4005_7FFF	Reserved	
0x4005_8000	0x4005_8FFF	Comparator	
0x4005_9000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC & PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM0	
0x4006_F000	0x4006_FFFF	GPTM1	
0x4007_0000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	

Start Address	End Address	Peripheral	Bus
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU & RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x4008_FFFF	Reserved	
0x4009_0000	0x4009_1FFF	PDMA	
0x4009_2000	0x4009_7FFF	Reserved	
0x4009_8000	0x4009_9FFF	EBI	
0x4009_A000	0x400A_7FFF	Reserved	
0x400A_8000	0x400A_9FFF	USB	
0x400A_A000	0x400A_BFFF	USB EP_SRAM	
0x400A_C000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIOA	
0x400B_2000	0x400B_3FFF	GPIOB	
0x400B_4000	0x400B_5FFF	GPIOC	
0x400B_6000	0x400B_7FFF	GPIOD	
0x400B_8000	0x400F_FFFF	Reserved	

Clock Structure

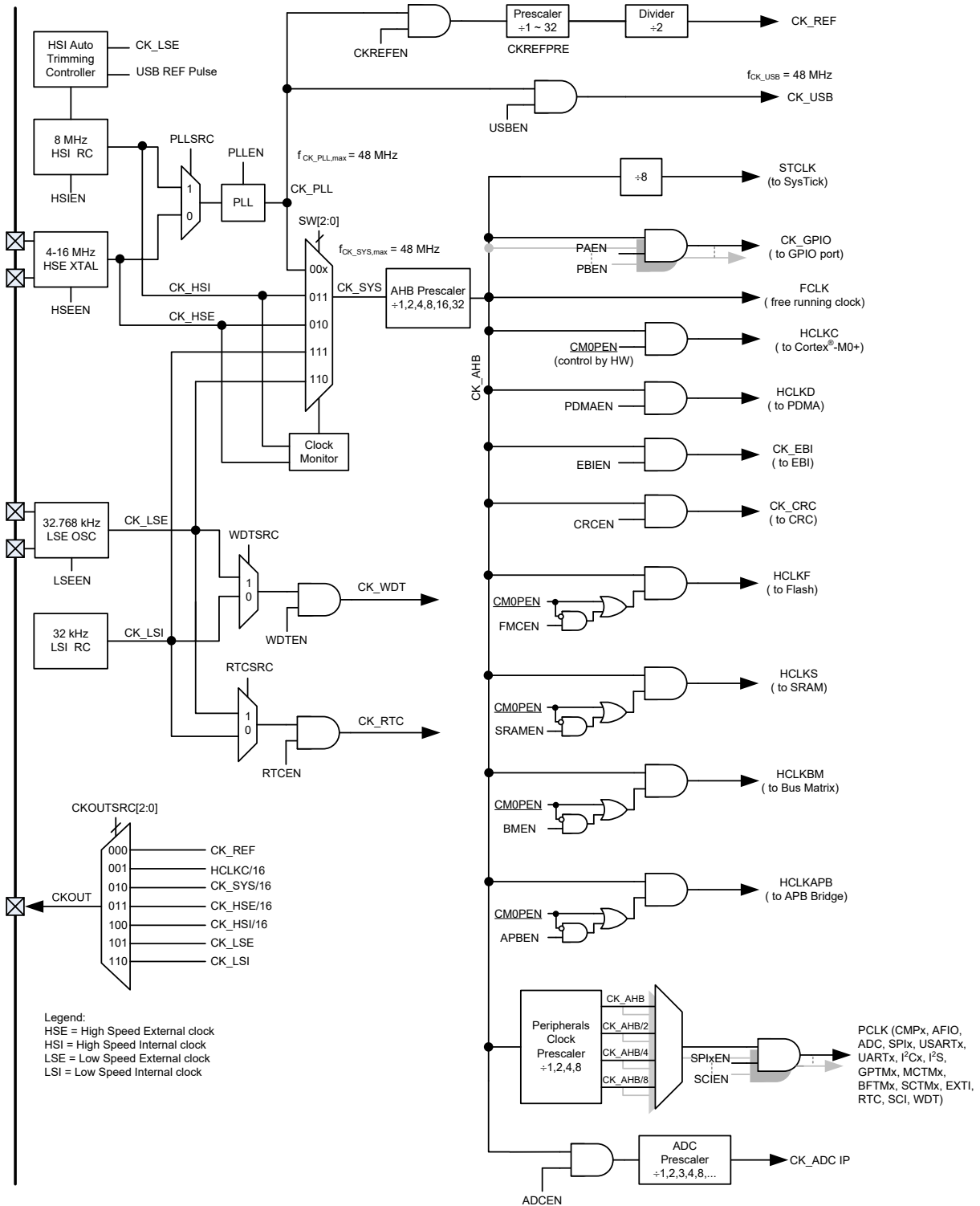


Figure 3. Clock Structure

4 Pin Assignment

4 Pin Assignment

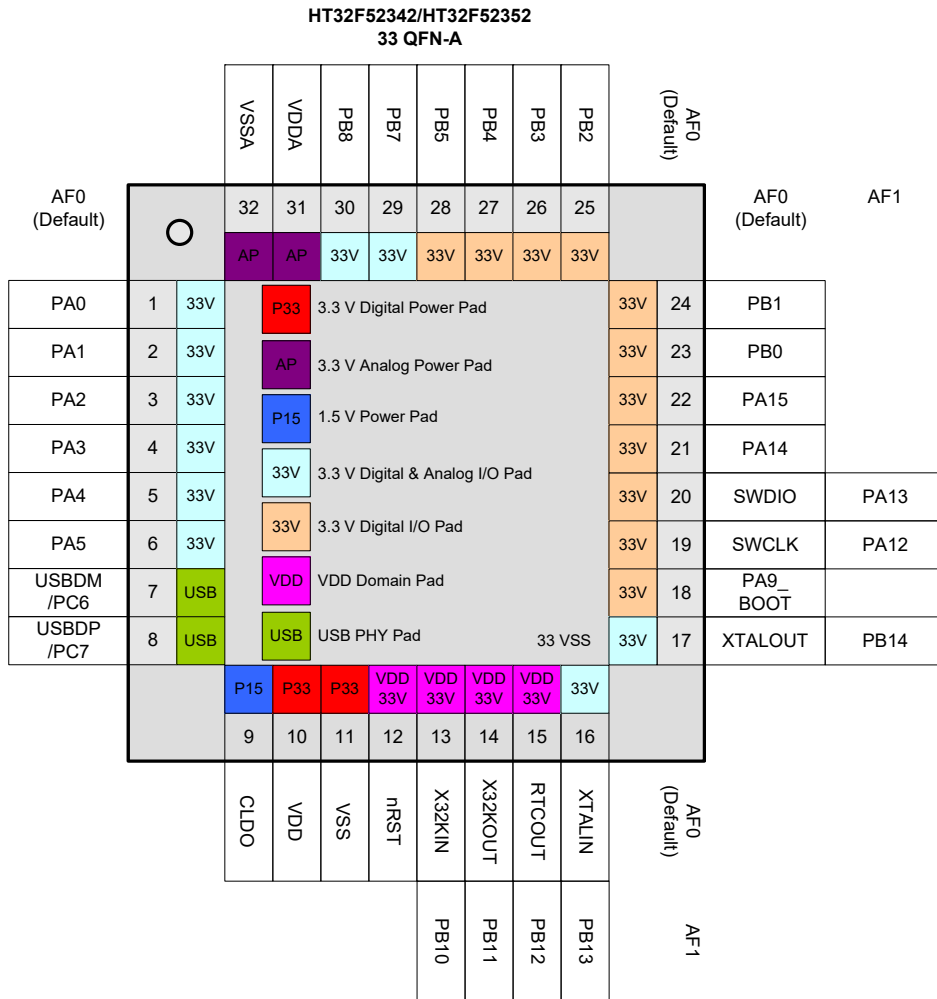
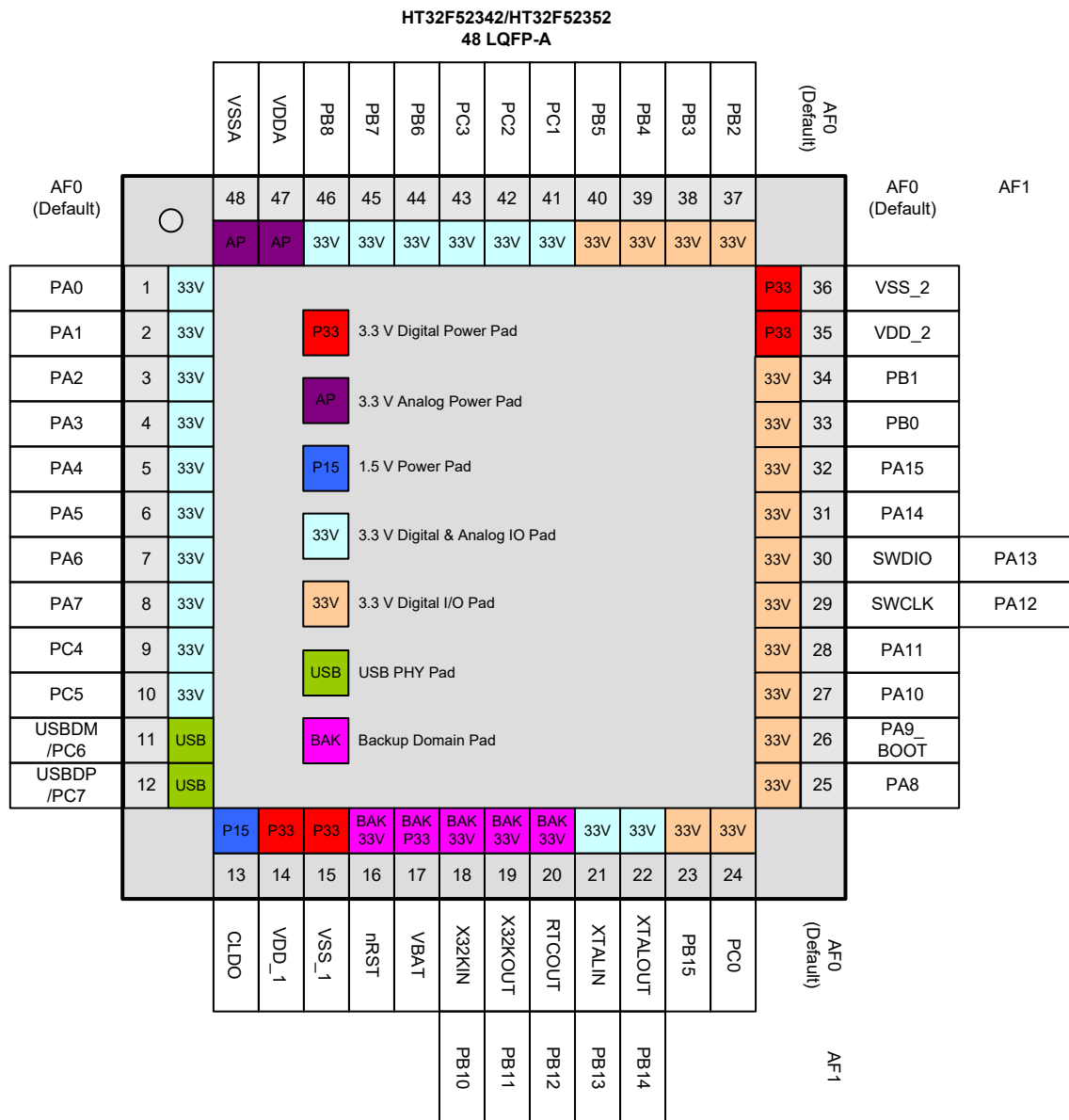


Figure 4. 33-pin QFN Pin Assignment



4 Pin Assignment

Figure 5. 48-pin LQFP Pin Assignment

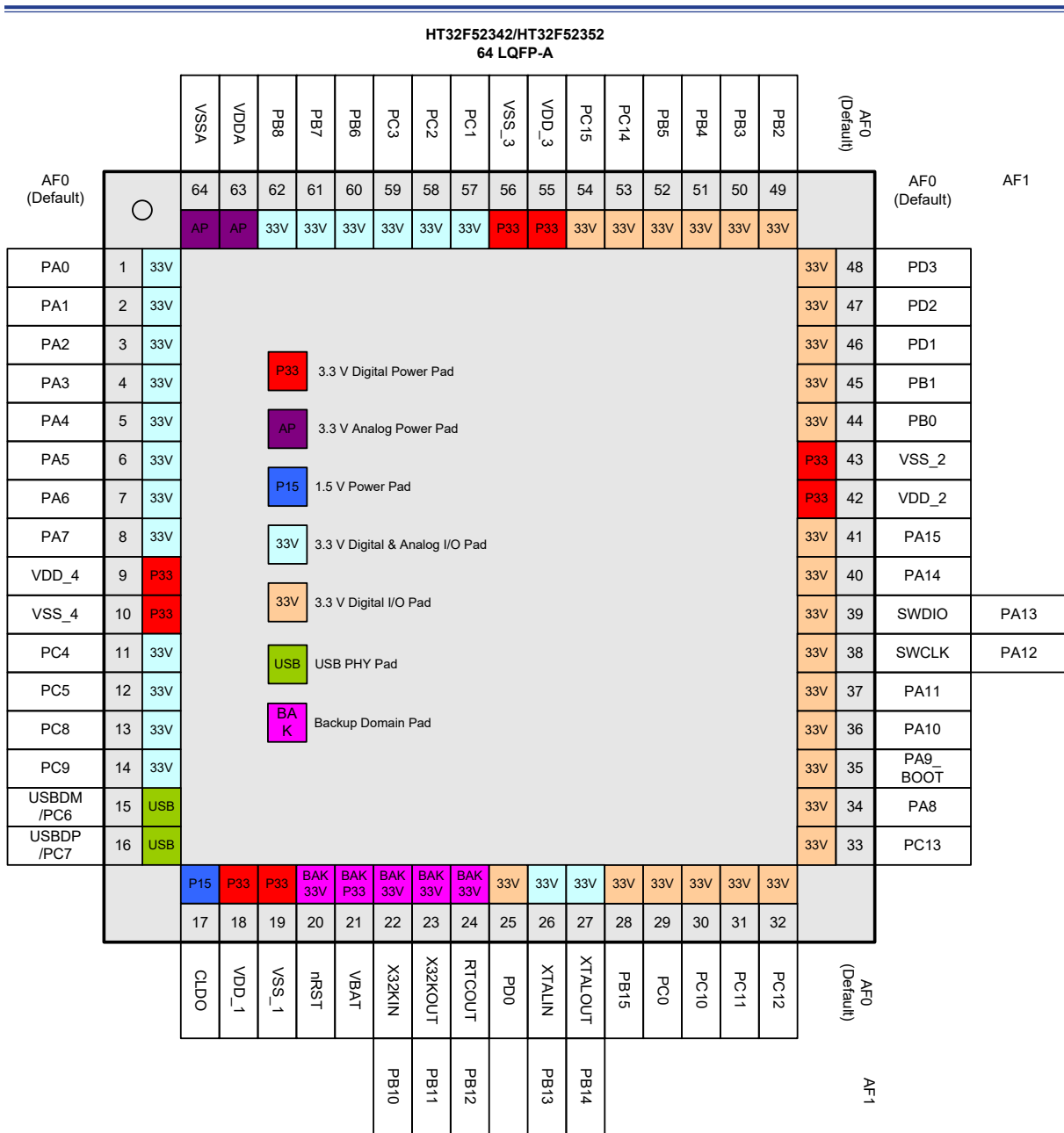


Figure 6. 64-pin LQFP Pin Assignment

Table 3. Pin Assignment

Package			Alternate Function Mapping																
64 LQFP	48 LQFP	33 QFN	AF0 System Default	AF1 GPIO	AF2 ADC	AF3 CMP	AF4 MCTM/GPTM	AF5 SPI	AF6 USART/UART	AF7 I2C1_SDA	AF8 SCI	AF9 EBI	AF10 I2S_WS	AF11 N/A	AF12 N/A	AF13 SCTM	AF14 N/A	AF15 System Other	
1	1	1	PA0		ADC_IN0		GT1_CH0	SPI1_SCK	USR0_RTS	I2C1_SCL	SCI0_CLK		I2S_WS						
2	2	2	PA1		ADC_IN1		GT1_CH1	SPI1_MOSI	USR0_CTS	I2C1_SDA	SCI0_DIO		I2S_BCLK						
3	3	3	PA2		ADC_IN2		GT1_CH2	SPI1_MISO	USR0_TX				I2S_SDO						
4	4	4	PA3		ADC_IN3		GT1_CH3	SPI1_SEL	USR0_RX				I2S_SDI						
5	5	5	PA4		ADC_IN4		GT0_CH0	SPI0_SCK	USR1_TX	I2C0_SCL	SCI1_CLK								
6	6	6	PA5		ADC_IN5		GT0_CH1	SPI0_MOSI	USR1_RX	I2C0_SDA	SCI1_DIO								
7	7		PA6		ADC_IN6		GT0_CH2	SPI0_MISO	USR1_RTS		SCI1_DET								
8	8		PA7		ADC_IN7		GT0_CH3	SPI0_SEL	USR1_CTS				I2S_MCLK						
9			VDD_4																
10			VSS_4																
11	9		PC4		ADC_IN8		GT0_CH0	SPI1_SEL	UR0_TX	I2C1_SCL		EBI_A19				SCTM0			
12	10		PC5		ADC_IN9		GT0_CH1	SPI1_SCK	UR0_RX	I2C1_SDA		EBI_A20				SCTM1			
13			PC8		ADC_IN10		GT0_CH2	SPI1_MOSI				EBI_A0							
14			PC9		ADC_IN11		GT0_CH3	SPI1_MISO				EBI_A1							
15	11	7	PC6				MT_CH2		USR0_TX	I2C0_SCL									
15	11	7	USBDM																
16	12	8	USBDP																
16	12	8	PC7				MT_CH2N		USR0_RX	I2C0_SDA									
17	13	9	CLDO																
18	14	10	VDD_1																
19	15	11	VSS_1																
20	16	12	nRST																
21	17		VBAT																
22	18	13	X32KIN	PB10															
23	19	14	X32KOUT	PB11															
24	20	15	RTCOUT	PB12															WAKE-UP
25			PD0							I2C0_SDA		EBI_A18	I2S_SDI			SCTM0			
26	21	16	XTALIN	PB13															
27	22	17	XTALOUT	PB14															
28	23		PB15				MT_CH0	SPI0_SEL	USR1_TX	I2C1_SCL		EBI_A16	I2S_MCLK						
29	24		PC0				MT_CH0N	SPI0_SCK	USR1_RX	I2C1_SDA		EBI_A17							
30			PC10				GT1_CH0	SPI1_SEL				EBI_AD13	I2S_WS						
31			PC11				GT1_CH1	SPI1_SCK				EBI_AD14	I2S_BCLK						
32			PC12				GT1_CH2	SPI1_MOSI	UR1_TX	I2C0_SCL		EBI_AD15	I2S_SDO						
33			PC13				GT1_CH3	SPI1_MISO	UR1_RX	I2C0_SDA		EBI_CS3	I2S_SDI						

Package			Alternate Function Mapping																
64 LQFP	48 LQFP	33 QFN	AF0 System Default	AF1 GPIO	AF2 ADC	AF3 CMP	AF4 MCTM /GPTM	AF5 SPI	AF6 USART /UART	AF7 I²C	AF8 SCI	AF9 EBI	AF10 I²S	AF11 N/A	AF12 N/A	AF13 SCTM	AF14 N/A	AF15 System Other	
34	25		PA8						USR0_TX		SCI1_CLK		I2S_MCLK						
35	26	18	PA9_BOOT					SPI0_MOSI			SCI1_DIO	EBI_A1	I2S_WS						CKOUT
36	27		PA10				MT_CH1		USR0_RX		SCI0_DET								
37	28		PA11				MT_CH1N	SPI0_MISO			SCI1_DET	EBI_A0	I2S_MCLK				SCTM0		
38	29	19	SWCLK	PA12															
39	30	20	SWDIO	PA13															
40	31	21	PA14				MT_CH0	SPI1_SEL	USR1_TX	I2C1_SCL	SCI0_CLK	EBI_AD0							
41	32	22	PA15				MT_CH0N	SPI1_SCK	USR1_RX	I2C1_SDA	SCI0_DIO	EBI_AD1					SCTM1		
42			VDD_2																
43			VSS_2																
44	33	23	PB0				MT_CH1	SPI1_MOSI	USR0_TX	I2C0_SCL		EBI_AD2							
45	34	24	PB1				MT_CH1N	SPI1_MISO	USR0_RX	I2C0_SDA		EBI_AD3							
46			PD1				MT_CH2		USR1_RTS		SCI0_CLK	EBI_AD10							
47			PD2				MT_CH2N		USR1_CTS		SCI0_DIO	EBI_AD11							
48			PD3				MT_CH3				SCI0_DET	EBI_AD12							
	35		VDD_2																
	36	33	VSS_2																
49	37	25	PB2				MT_CH2	SPI0_SEL	UR0_TX			EBI_AD4							
50	38	26	PB3				MT_CH2N	SPI0_SCK	UR0_RX			EBI_AD5					SCTM1		
51	39	27	PB4				MT_BRK	SPI0_MOSI	UR1_TX			EBI_AD6					SCTM0		
52	40	28	PB5				MT_BRK	SPI0_MISO	UR1_RX			EBI_AD7							
53			PC14				MT_CH3			I2C0_SCL		EBI_AD8							
54			PC15							I2C0_SDA		EBI_AD9					SCTM1		
55			VDD_3																
56			VSS_3																
57	41		PC1			CN0	MT_CH0	SPI1_SEL	UR1_TX			EBI_OE	I2S_MCLK						
58	42		PC2			CP0	MT_CH0N	SPI1_SCK				EBI_CS0							
59	43		PC3			COUT0		SPI1_MOSI	UR1_RX			EBI_WE							
60	44		PB6			CN1	MT_CH2	SPI1_MISO	UR0_TX		SCI1_CLK	EBI_ALE	I2S_BCLK						
61	45	29	PB7			CP1	MT_CH2N			I2C1_SCL	SCI1_DET	EBI_CS1	I2S_SDO						
62	46	30	PB8			COUT1	MT_CH3		UR0_RX	I2C1_SDA	SCI1_DIO	EBI_CS2	I2S_SDI						
63	47	31	VDDA																
64	48	32	VSSA																

Table 4. Pin Description

Pin Number			Pin Name	Type ⁽¹⁾	I/O Structure ⁽²⁾	Output Driving	Description
64 LQFP	48 LQFP	33 QFN					Default Function (AF0)
1	1	1	PA0	AI/O	33V	4/8/12/16 mA	PA0
2	2	2	PA1	AI/O	33V	4/8/12/16 mA	PA1
3	3	3	PA2	AI/O	33V	4/8/12/16 mA	PA2
4	4	4	PA3	AI/O	33V	4/8/12/16 mA	PA3
5	5	5	PA4	AI/O	33V	4/8/12/16 mA	PA4, this pin provides a USART_TX function in the Boot loader mode
6	6	6	PA5	AI/O	33V	4/8/12/16 mA	PA5, this pin provides a USART_RX function in the Boot loader mode
7	7		PA6	AI/O	33V	4/8/12/16 mA	PA6
8	8		PA7	AI/O	33V	4/8/12/16 mA	PA7
9			VDD_4	P	—	—	Voltage for digital I/O
10			VSS_4	P	—	—	Ground reference for digital I/O
11	9		PC4	AI/O	33V	4/8/12/16 mA	PC4
12	10		PC5	AI/O	33V	4/8/12/16 mA	PC5
13			PC8	AI/O	33V	4/8/12/16 mA	PC8
14			PC9	AI/O	33V	4/8/12/16 mA	PC9
15	11	7	PC6	I/O	33V	4/8/12/16 mA	PC6
15	11	7	USBDM	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
16	12	8	USBDP	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
16	12	8	PC7	I/O	33V	4/8/12/16 mA	PC7
17	13	9	CLDO	P	—	—	Core power LDO V _{CORE} output It must be connected a 2.2 μF capacitor as close as possible between this pin and VSS_1
18	14	10	VDD_1	P	—	—	Voltage for digital I/O
19	15	11	VSS_1	P	—	—	Ground reference for digital I/O
20	16	12	nRST	I(BK)	33V_PU	—	External reset pin and external wakeup pin in the Power-Down mode
21	17		VBAT	P	—	—	Battery power input for the backup domain
22	18	13	PB10 ⁽⁴⁾	AI/O(BK)	33V	< 2 mA	X32KIN
23	19	14	PB11 ⁽⁴⁾	AI/O(BK)	33V	< 2 mA	X32KOUT
24	20	15	PB12 ⁽⁴⁾	I/O(BK)	33V	< 2 mA	RTCOUT
25			PD0	I/O	33V	4/8/12/16 mA	PD0
26	21	16	PB13	AI/O	33V	4/8/12/16 mA	XTALIN
27	22	17	PB14	AI/O	33V	4/8/12/16 mA	XTALOUT
28	23		PB15	I/O	33V	4/8/12/16 mA	PB15
29	24		PC0	I/O	33V	4/8/12/16 mA	PC0
30			PC10	I/O	33V	4/8/12/16 mA	PC10
31			PC11	I/O	33V	4/8/12/16 mA	PC11
32			PC12	I/O	33V	4/8/12/16 mA	PC12
33			PC13	I/O	33V	4/8/12/16 mA	PC13

Pin Number			Pin Name	Type ⁽¹⁾	I/O Structure ⁽²⁾	Output Driving	Description
64 LQFP	48 LQFP	33 QFN					Default Function (AF0)
34	25		PA8	I/O	33V_PU	4/8/12/16 mA	PA8
35	26	18	PA9	I/O	33V_PU	4/8/12/16 mA	PA9_BOOT
36	27		PA10	I/O	33V	4/8/12/16 mA	PA10
37	28		PA11	I/O	33V	4/8/12/16 mA	PA11
38	29	19	PA12	I/O	33V_PU	4/8/12/16 mA	SWCLK
39	30	20	PA13	I/O	33V_PU	4/8/12/16 mA	SWDIO
40	31	21	PA14	I/O	33V	4/8/12/16 mA	PA14
41	32	22	PA15	I/O	33V	4/8/12/16 mA	PA15
42			VDD_2	P	—	—	Voltage for digital I/O
43			VSS_2	P	—	—	Ground reference for digital I/O
44	33	23	PB0	I/O	33V	4/8/12/16 mA	PB0
45	34	24	PB1	I/O	33V	4/8/12/16 mA	PB1
46			PD1	I/O	33V	4/8/12/16 mA	PD1
47			PD2	I/O	33V	4/8/12/16 mA	PD2
48			PD3	I/O	33V	4/8/12/16 mA	PD3
	35		VDD_2	P	—	—	Voltage for digital I/O
	36	33	VSS_2	P	—	—	Ground reference for digital I/O
49	37	25	PB2	I/O	33V	4/8/12/16 mA	PB2
50	38	26	PB3	I/O	33V	4/8/12/16 mA	PB3
51	39	27	PB4	I/O	33V	4/8/12/16 mA	PB4
52	40	28	PB5	I/O	33V	4/8/12/16 mA	PB5
53			PC14	I/O	33V	4/8/12/16 mA	PC14
54			PC15	I/O	33V	4/8/12/16 mA	PC15
55			VDD_3	P	—	—	Voltage for digital I/O
56			VSS_3	P	—	—	Ground reference for digital I/O
57	41		PC1	AI/O	33V	4/8/12/16 mA	PC1
58	42		PC2	AI/O	33V	4/8/12/16 mA	PC2
59	43		PC3	AI/O	33V	4/8/12/16 mA	PC3
60	44		PB6	AI/O	33V	4/8/12/16 mA	PB6
61	45	29	PB7	AI/O	33V	4/8/12/16 mA	PB7
62	46	30	PB8	AI/O	33V	4/8/12/16 mA	PB8
63	47	31	VDDA	P	—	—	Analog voltage for ADC and Comparator
64	48	32	VSSA	P	—	—	Ground reference for the ADC and Comparator

- Note: 1. I = input, O = output, A = Analog port, P = power supply, PU = pull-up, BK = Back-up domain
 2. 33V = 3.3 V tolerant.
 3. The GPIOs are in an AF0 state after a V_{CORE} power on reset (V_{CORE_POR}) except for the RTCOUT pin in the Backup Domain I/O. The RTCOUT pin is reset by the Backup Domain power-on-reset (PORB) or by the Backup Domain software reset (BAK_RST bit in BAK_CR register).
 4. The backup domain of the I/O pins have a source current capability limitation of < 2 mA @ V_{DD} = 3.3 V. The typical sink current is 4/8 mA configurable @ V_{DD} = 3.3 V.
 5. In the Boot loader mode, the USART interface and USB function can be used for communication.

5 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V _{DD}	External Main Supply Voltage	V _{SS} - 0.3	V _{SS} + 3.6	V
V _{DDA}	External Analog Supply Voltage	V _{SSA} - 0.3	V _{SSA} + 3.6	V
V _{BAT}	External Battery Supply Voltage	V _{SS} - 0.3	V _{SS} + 3.6	V
V _{IN}	Input Voltage on I/O	V _{SS} - 0.3	V _{DD} + 0.3	V
T _A	Ambient Operating Temperature Range	-40	+85	°C
T _{STG}	Storage Temperature Range	-60	+150	°C
T _J	Maximum Junction Temperature	—	125	°C
P _D	Total Power Dissipation	—	500	mW
V _{ESD}	Electrostatic Dscharge Voltage – Human Body Mode	-4000	+4000	V

Recommended DC Operating Conditions

Table 6. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{DD}	I/O Operating Voltage		2.0	3.3	3.6	V
V _{DDA}	Analog Operating Voltage		2.5	3.3	3.6	V
V _{BAT}	Battery Supply Operating Voltage		2.0	3.3	3.6	V

On-Chip LDO Voltage Regulator Characteristics

Table 7. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{LDO}	Internal Regulator Output Voltage	V _{DD} ≥ 2.0 V Regulator input @ I _{LDO} = 35 mA and voltage, variant = ±5 %, after trimming.	1.425	1.5	1.57	V
I _{LDO}	Output Current	V _{DD} = 2.0 V Regulator input @ V _{LDO} = 1.5 V	—	35	—	mA
C _{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent upon the core power current consumption	—	2.2	—	μF

Power Consumption

Table 8. Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Typ.	Max. @ T _A		Unit
				25 °C	85 °C	
I _{DD}	Supply Current (Run Mode)	V _{DD} = V _{BAT} = 3.3 V, HSI = 8 MHz, PLL = 48 MHz, f _{CPU} = 48 MHz, f _{BUS} = 48 MHz, all peripherals enabled	20	22.1	—	mA
		V _{DD} = V _{BAT} = 3.3 V, HSI = 8 MHz, PLL = 48 MHz, f _{CPU} = 48 MHz, f _{BUS} = 48 MHz, all peripherals disabled	10.1	11.6	—	
		V _{DD} = V _{BAT} = 3.3 V, HSI off, PLL off, LSI on, f _{CPU} = 32 kHz, f _{BUS} = 32 kHz, all peripherals enabled	44	55	—	μA
		V _{DD} = V _{BAT} = 3.3 V, HSI off, PLL off, LSI on, f _{CPU} = 32 kHz, f _{BUS} = 32 kHz, all peripherals disabled	40	51	—	
	Supply Current (Sleep Mode)	V _{DD} = V _{BAT} = 3.3 V, HSI = 8 MHz, PLL = 48 MHz, f _{CPU} = 0 MHz, f _{BUS} = 48 MHz, all peripherals enabled	12	13.8	—	mA
		V _{DD} = V _{BAT} = 3.3 V, HSI = 8 MHz, PLL = 48 MHz, f _{CPU} = 0 MHz, f _{BUS} = 48 MHz, all peripherals disabled	2	2.3	—	
	Supply Current (Deep-Sleep1 Mode)	V _{DD} = V _{BAT} = 3.3 V, All clock off (HSE/HSI/PLL/LSE), LDO in low power mode, LSI on, RTC on	34	43.8	—	μA
	Supply Current (Deep-Sleep2 Mode)	V _{DD} = V _{BAT} = 3.3 V, All clock off (HSE/HSI/PLL/LSE), LDO off, DMOS on, LSI on, RTC on	5	12	—	
	Supply current (Power-Down Mode)	V _{DD} = V _{BAT} = 3.3 V, LDO off, DMOS off, LSE off, LSI on, RTC on	1.85	2.75	—	
		V _{DD} = V _{BAT} = 3.3 V, LDO off, DOMS off, LSE off, LSI on, RTC off	1.80	2.67	—	
I _{BAT}	Battery Supply Current (Power-Down Mode)	V _{DD} not present, V _{BAT} = 3.3 V, LDO off, DMOS off, LSE off, LSI on, RTC on	1.36	2	—	
		V _{DD} not present, V _{BAT} = 3.3 V, LDO off, DMOS off, LSE off, LSI on, RTC off	1.36	2	—	

- Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
 2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
 3. RTC means Real-Time clock.
 4. Code = while (1) { 208 NOP } executed in Flash.
 5. f_{BUS} means f_{HCLK} and f_{PCLK}.

Reset and Supply Monitor Characteristics

Table 9. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{POR}	Power on Reset Threshold (Rising Voltage on V _{DD})	T _A = -40 °C~ 85 °C	1.66	1.79	1.90	V
V _{PDR}	Power Down Reset Threshold (Falling Voltage on V _{DD})		1.49	1.64	1.78	V
V _{PORHYST}	POR Hysteresis	—	—	150	—	mV
t _{POR}	Reset Delay Time	V _{DD} = 3.3 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.

2. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO will be turned off.

Table 10. LVD/BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
V _{BOD}	Voltage of Brown Out Detection	After factory-trimmed (V _{DD} Falling edge)	2.02	2.1	2.18	V	
V _{LVD}	Voltage of Low Voltage Detection	(V _{DD} Falling edge)	LVDS = 000	2.17	2.25	2.33	V
			LVDS = 001	2.32	2.4	2.48	V
			LVDS = 010	2.47	2.55	2.63	V
			LVDS = 011	2.62	2.7	2.78	V
			LVDS = 100	2.77	2.85	2.93	V
			LVDS = 101	2.92	3.0	3.08	V
			LVDS = 110	3.07	3.15	3.23	V
LVDS = 111	3.22	3.3	3.38	V			
V _{LVDHTST}	LVD Hysteresis	V _{DD} = 3.3 V	—	—	100	mV	
t _{suLVD}	LVD Setup Time	V _{DD} = 3.3 V	—	—	5	μs	
t _{aLLVD}	LVD Active Delay Time	V _{DD} = 3.3 V	—	—	—	μs	
I _{DDLVD}	Operation Current ⁽²⁾	V _{DD} = 3.3 V	—	—	5	15	μA

Note: 1. Data based on characterization results only, not tested in production.

2. Bandgap current is not included.

3. LVDS field is in the PWRUCU LVDCSR register

External Clock Characteristics

Table 11. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{DD}	Operation Range	—	2.0	—	3.6	V
f _{HSE}	High Speed External Oscillator Frequency (HSE)	—	4	—	16	MHz
C _L	Load Capacitance	V _{DD} = 3.3 V, R _{ESR} = 100 Ω @ 16 MHz	—	—	22	pF
R _{FHSE}	Internal Feedback Resistor between XTALIN and XTALOUT Pins	—	—	1	—	MΩ
R _{ESR}	Equivalent Series Resistance	V _{DD} = 3.3 V, C _L = 12 pF @ 16 MHz, HSEDR = 0 V _{DD} = 2.4 V, C _L = 12 pF @ 16 MHz, HSEDR = 1	—	—	160	Ω
D _{HSE}	HSE Oscillator Duty cycle	—	40	—	60	%
I _{DDHSE}	HSE Oscillator Current Consumption	V _{DD} = 3.3 V @ 16 MHz	—	TBD	—	mA
I _{PWDHSE}	HSE Oscillator Power Down Current	V _{DD} = 3.3 V	—	—	0.01	μA
t _{SUHSE}	HSE Oscillator Startup Time	V _{DD} = 3.3 V	—	—	4	ms

Table 12. Low Speed External Clock (LSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{BAK}	Operation Range	—	2.0	—	3.6	V
f _{CK_LSE}	LSE Frequency	V _{BAK} = 2.0 V ~ 3.6 V	—	32.768	—	kHz
R _F	Internal Feedback Resistor	—	—	10	—	MΩ
R _{ESR}	Equivalent Series Resistance	V _{BAK} = 3.3 V	30	—	TBD	KΩ
C _L	Recommended Load Capacitances	V _{BAK} = 3.3 V	6	—	TBD	pF
I _{DDLSE}	Oscillator Supply Current (High Current Mode)	f _{CK_LSE} = 32.768 kHz, R _{ESR} = 50 kΩ, C _L ≥ 7 p, V _{BAK} = 2.0 V ~ 2.7 V, T _A = -40 °C ~ 85 °C	—	3.3	6.3	μA
	Oscillator Supply Current (Low Current Mode)	f _{CK_LSE} = 32.768 kHz, R _{ESR} = 50 kΩ, C _L < 7 pF, V _{BAK} = 2.0 V ~ 3.6 V, T _A = -40 °C ~ 85 °C	—	1.8	3.3	μA
	Power Down Current	—	—	—	0.01	μA
t _{SULSE}	Startup Time (Low Current Mode)	f _{CK_LSI} = 32.768 kHz, V _{BAK} = 2.0 V ~ 3.6 V	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE / LSE clock in the PCB layout:

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace lengths as short as possible to reduce any parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep any high frequency signal lines away from the crystal area to prevent any crosstalk adverse effects.

Internal Clock Characteristics

Table 13. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{DD}	Operation Range	—	2.0		3.6	V
f _{HSI}	HSI Frequency	V _{DD} = 3.3 V @ 25 °C	—	8	—	MHz
ACC _{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V _{DD} = 3.3 V, T _A = 25 °C	-2	—	2	%
		V _{DD} = 2.5 V ~ 3.6 V, T _A = -40 °C ~ 85 °C	-3	—	3	%
		V _{DD} = 2.0 V ~ 3.6 V, T _A = -40 °C ~ 85 °C	-4	—	4	%
Duty	Duty Cycle	f _{HSI} = 8 MHz	35	—	65	%
I _{DDHSI}	Oscillator Supply Current	f _{HSI} = 8 MHz	—	300	500	μA
	Power Down Current		—	—	0.05	μA
t _{suHSI}	Startup Time	f _{HSI} = 8 MHz	—	—	10	μs

Table 14. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f _{LSI}	Low Speed Internal Oscillator Frequency (LSI)	V _{DD} = 3.3 V, T _A = -40 °C ~ 85 °C	21	32	43	kHz
ACC _{LSI}	LSI Frequency Accuracy	After factory-trimmed, V _{DD} = 3.3 V	-10	—	+10	%
I _{DDL}	LSI Oscillator Operating Current	V _{DD} = 3.3 V	—	0.4	0.8	μA
t _{SULSI}	LSI Oscillator Startup Time	V _{DD} = 3.3 V	—	—	100	μs

PLL Characteristics

Table 15. PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f _{PLLIN}	PLL Input Clock	—	4	—	16	MHz
f _{CK_PLL}	PLL Output Clock	—	4	—	48	MHz
t _{LOCK}	PLL Lock Time	—	—	200	—	μs

Memory Characteristics

Table 16. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N _{ENDU}	Number of Guaranteed Program / Erase Cycles Before Failure. (Endurance)	T _A = -40 °C ~ 85 °C	20	—	—	K cycles
t _{RET}	Data Retention Time	T _A = -40 °C ~ 85 °C	10	—	—	Years
t _{PROG}	Word Programming Time	T _A = -40 °C ~ 85 °C	20	—	—	μs
t _{ERASE}	Page Erase Time	T _A = -40 °C ~ 85 °C	2	—	—	ms
t _{MERASE}	Mass Erase Time	T _A = -40 °C ~ 85 °C	10	—	—	ms

I/O Port Characteristics

Table 17. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
I _{IL}	Low Level Input Current	3.3 V I/O	V _I = V _{SS} , On-chip pull-up resistor disabled.	—	—	3	μA
		Reset pin		—	—	3	μA
I _{IH}	High Level Input Current	3.3 V I/O	V _I = V _{DD} , On-chip pull-down resistor disabled.	—	—	3	μA
		Reset pin		—	—	3	μA
V _{IL}	Low Level Input Voltage	3.3 V I/O	—	—	V _{DD} × 0.35	V	
		Reset pin	-0.5	—	V _{DD} × 0.35	V	
V _{IH}	High Level Input Voltage	3.3 V I/O	V _{DD} × 0.65	—	V _{DD} + 0.5	V	
		Reset pin	V _{DD} × 0.65	—	V _{DD} + 0.5	V	
V _{HYS}	Schmitt Trigger Input Voltage Hysteresis	3.3 V I/O	—	0.12 × V _{DD}	—	mV	
		Reset pin	—	0.12 × V _{DD}	—	mV	
I _{OL}	Low Level Output Current (GPIO Sink Current)	3.3 V I/O 4 mA drive, V _{OL} = 0.4 V	4	—	—	mA	
		3.3 V I/O 8 mA drive, V _{OL} = 0.4 V	8	—	—	mA	
		3.3 V I/O 12 mA drive, V _{OL} = 0.4 V	12	—	—	mA	
		3.3 V I/O 16 mA drive, V _{OL} = 0.4 V	16	—	—	mA	
		Backup Domain I/O drive @ V _{DD} = 3.3 V, V _{OL} = 0.4 V, PB10, PB11, PB12	4	—	—	mA	
I _{OH}	High Level Output current (GPIO Source Current)	3.3 V I/O 4 mA drive, V _{OH} = V _{DD} - 0.4 V	4	—	—	mA	
		3.3 V I/O 8 mA drive, V _{OH} = V _{DD} - 0.4 V	8	—	—	mA	
		3.3 V I/O 12 mA drive, V _{OH} = V _{DD} - 0.4 V	12	—	—	mA	
		3.3 V I/O 16 mA drive, V _{OH} = V _{DD} - 0.4 V	16	—	—	mA	
		Backup Domain I/O drive @ V _{DD} = 3.3 V, V _{OL} = V _{DD} - 0.4 V, PB10, PB11, PB12.	—	—	2	mA	
V _{OL}	Low Level Output Voltage	3.3 V 4 mA drive I/O, I _{OL} = 4 mA	—	—	0.4	V	
		3.3 V 8 mA drive I/O, I _{OL} = 8 mA	—	—	0.4	V	
		3.3 V 12 mA drive I/O, I _{OL} = 12 mA	—	—	0.4	V	
		3.3 V 16 mA drive I/O, I _{OL} = 16 mA	—	—	0.4	V	
		Backup Domain I/O Sink Current = 4 mA (Low driving strength)	V _{DD} = 2.7 V~3.6 V	—	—	0.4	V
			V _{DD} = 2.0 V~2.7 V	—	—	0.6	V
		Backup Domain I/O Sink Current = 8 mA (High driving strength)	V _{DD} = 2.7 V~3.6 V	—	—	0.4	V
V _{DD} = 2.0 V~2.7 V	—		—	0.6	V		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
V _{OH}	High Level Output Voltage	3.3 V 4 mA drive I/O, I _{OH} = 4 mA	V _{DD} - 0.4	—	—	V	
		3.3 V 8 mA drive I/O, I _{OH} = 8 mA	V _{DD} - 0.4	—	—	V	
		3.3 V 12 mA drive I/O, I _{OL} = 12 mA	V _{DD} - 0.4	—	—	V	
		3.3 V 16 mA drive I/O, I _{OL} = 16 mA	V _{DD} - 0.4	—	—	V	
		Backup Domain I/O Source Current = 2mA	V _{DD} = 2.7 V~3.6 V	2.4	—	—	V
		Backup Domain I/O Source Current = 1mA	V _{DD} = 2.0 V~2.7 V	V _{DD} - 0.4	—	—	V
R _{PU}	Internal Pull-up Resistor	3.3 V I/O	—	46	—	kΩ	
R _{PD}	Internal Pull-down Resistor	3.3 V I/O	—	46	—	kΩ	

ADC Characteristics

Table 18. ADC Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{DDA}	Operating Voltage	—	2.5	3.3	3.6	V
V _{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V _{REF+}	V
V _{REF+}	A/D Converter Reference Voltage	—	—	V _{DDA}	V _{DDA}	V
I _{ADC}	Current Consumption	V _{DDA} = 3.3 V	—	1	TBD	mA
I _{ADC_DN}	Power Down Current Consumption	V _{DDA} = 3.3 V	—	—	0.1	μA
f _{ADC}	A/D Converter Clock	—	0.7	—	16	MHz
f _S	Sampling Rate	—	0.05	—	1	Msp/s
t _{DL}	Data Latency	—	—	12.5	—	1/f _{ADC} Cycles
t _{S&H}	Sampling & Hold Time	—	—	3.5	—	1/f _{ADC} Cycles
t _{ADCCONV}	A/D Converter Conversion Time	ADST[7:0] = 2	—	16	—	1/f _{ADC} Cycles
R _I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C _I	Input Sampling Capacitance	No pin/pad capacitance included	—	16	—	pF
t _{SU}	Startup Time	—	—	—	1	μs
N	Resolution	—	—	12	—	bits
INL	Integral Non-linearity Error	f _S = 750 ksps, V _{DDA} = 3.3 V	—	±2	±5	LSB
DNL	Differential Non-linearity Error	f _S = 750 ksps, V _{DDA} = 3.3 V	—	±1	—	LSB
E _O	Offset Error	—	—	—	±10	LSB
E _G	Gain Error	—	—	—	±10	LSB

Note: 1. Data based on characterization results only, not tested in production.

2. Due to the A/D Converter input channel and GPIO pin-shared function design limitation, the V_{DDA} supply power of the A/D Converter has to be equal to the V_{DD} supply power of the MCU in the application circuit.

3. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_1 is the storage capacitor, R_1 is the resistance of the sampling switch and R_s is the output impedance of the signal source V_s . Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_1 , must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_s for accuracy. To guarantee this, R_s is not allowed to have an arbitrarily large value.

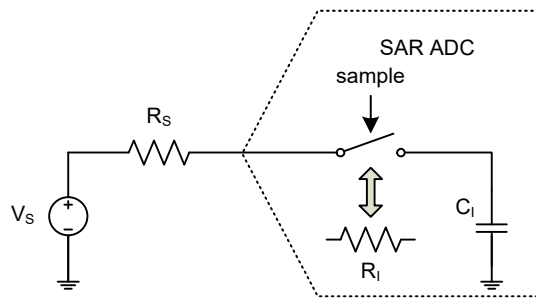


Figure 7. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0 V and V_{REF}) are sampled consecutively. In this situation a sampling error below $\frac{1}{4}$ LSB is ensured by using the following equation:

$$R_s < \frac{3.5}{f_{ADC} C_1 \ln(2^{N+2})} - R_1$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution ($N = 12$ in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_s may be larger than the value indicated by the equation above.

Comparator Characteristics

Table 19. Comparator Characteristics

$T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
V_{DDA}	Operating Voltage	Comparator mode	2.4	3.3	3.6	V	
V_{IN}	Input Common Mode Voltage Range	CP or CN	V_{SSA}	—	V_{DDA}	V	
V_{IOS}	Input Offset Voltage ⁽¹⁾	—	-15	—	15	mV	
V_{hys}	Input Hysteresis	No hysteresis (CMPnHM [1:0] = 00)	—	0	—	mV	
		Low hysteresis (CMPnHM [1:0] = 01)	—	30	—	mV	
		Middle hysteresis (CMPnHM [1:0] = 10)	—	70	—	mV	
		High hysteresis (CMPnHM [1:0] = 11)	—	100	—	mV	
t_{RT}	Response Time Input Overdrive = $\pm 100\text{mV}$	High Speed mode	$V_{DDA} \geq 2.7\text{ V}$	—	50	100	ns
			$V_{DDA} < 2.7\text{ V}$	—	100	250	
I_{CMP}	Current Consumption $V_{DDA} = 3.3\text{ V}$	High Speed mode	—	130	—	μA	
		Low Speed mode	—	30	—	μA	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t _{CMPST}	Comparator Startup Time	Comparator enabled to output valid.	—	—	50	μs
I _{CMP_DN}	Power Down Supply Current	COMPEN = 0, CVREFEN = 0 CVREFOE=0	—	—	0.1	μA
Comparator Voltage Reference (CVR)						
V _{CVR}	Output Range	—	V _{SSA}	—	V _{DDA}	V
N _{Bits}	CVR Scaler Resolution	—	—	6	—	bits
t _{CVRST}	Setting Time	V _{DDA} = 3.3 V, CVREFOE = 1, C _{LOAD} ≤ 100 pF, R _{LOAD} ≥ 50 kΩ, CVR scaler setting time from CVREF = "000000" to "111111"	—	—	100	μs
I _{CVR}	Current Consumption V _{DDA} = 3.3 V	CVREFEN=1, CMPREFOE=0	—	65	—	μA
		CVREFEN=1, CVREFOE=1	—	80	110	μA

Note: Data based on characterization results only, not tested in production.

SCTM/GPTM/MCTM Characteristics

Table 20. SCTM/GPTM/MCTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f _{TM}	Timer Clock Source for SCTM, GPTM and MCTM	—	—	—	48	MHz
t _{RES}	Timer Resolution Time	—	1	—	—	1/f _{TM}
f _{EXT}	External Single Frequency on Channel 1 ~ 4	—	—	—	1/2	f _{TM}
RES	Timer Resolution	—	—	—	16	bits

I²C Characteristics

Table 21. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{SCL}	SCL Clock Rrequency	—	100	—	400	—	1000	kHz
t _{SCL(H)}	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
t _{SCL(L)}	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t _{FALL}	SCL and SDA Rall Time	—	1.3	—	0.34	—	0.135	μs
t _{RISE}	SCL and SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
t _{SU(SDA)}	SDA Data Setup Time	500	—	125	—	50	—	ns
t _{H(SDA)}	SDA Data Hold Time ⁽⁵⁾	0	—	0	—	0	—	ns
	SDA Data Hold Time ⁽⁶⁾	100	—	100	—	100	—	ns
t _{VD(SDA)}	SDA Data Valid Time	—	1.6	—	0.475	—	0.25	μs
t _{SU(STA)}	START Condition Setup Time	500	—	125	—	50	—	ns
t _{H(STA)}	START Condition Hold Time	0	—	0	—	0	—	ns
t _{SU(STO)}	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Data based on characterization results only, not tested in production.

- To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
- To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
- To achieve 1 MHz fast mode plus, the peripheral clock frequency must be higher than 20 MHz.

5. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 0 and SEQFILTER = 00
6. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 1 and SEQFILTER = 00

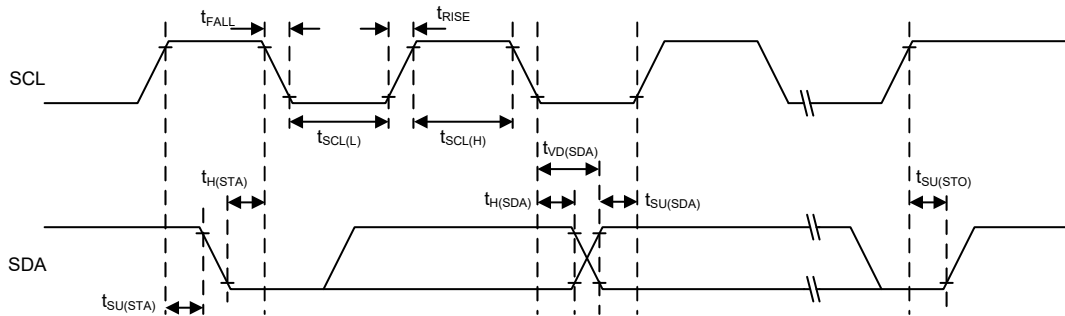


Figure 8. I²C Timing Diagrams

SPI Characteristics

Table 22. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f _{SCK}	SCK Clock Frequency	—	—	—	f _{PCLK} /2	MHZ
t _{SCK(H)}	SCK Clock High Time	—	f _{PCLK} /8	—	—	ns
t _{SCK(L)}	SCK Clock Low Time	—	f _{PCLK} /8	—	—	ns
SPI Master Mode						
t _{V(MO)}	Data Output Valid Time	—	—	—	5	ns
t _{H(MO)}	Data Output Hold Time	—	2	—	—	ns
t _{SU(MI)}	Data Input Setup Time	—	5	—	—	ns
t _{H(MI)}	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
t _{SU(SEL)}	SEL Enable Setup Time	—	4 t _{PCLK}	—	—	ns
t _{H(SEL)}	SEL Enable Hold Time	—	2 t _{PCLK}	—	—	ns
t _{A(SO)}	Data Output Access Time	—	—	—	3 t _{PCLK}	ns
t _{DIS(SO)}	Data Output Disable Time	—	—	—	10	ns
t _{V(SO)}	Data Output Valid Time	—	—	—	25	ns
t _{H(SO)}	Data Output Hold Time	—	15	—	—	ns
t _{SU(SI)}	Data Input Setup Time	—	5	—	—	ns
t _{H(SI)}	Data Input Hold Time	—	4	—	—	ns

Note: t_{SCK} = 1/f_{SCK}; t_{PCLK} = 1/f_{PCLK}. SPI output (input) clock frequency f_{SCK}; SPI peripheral clock frequency f_{PCLK}.

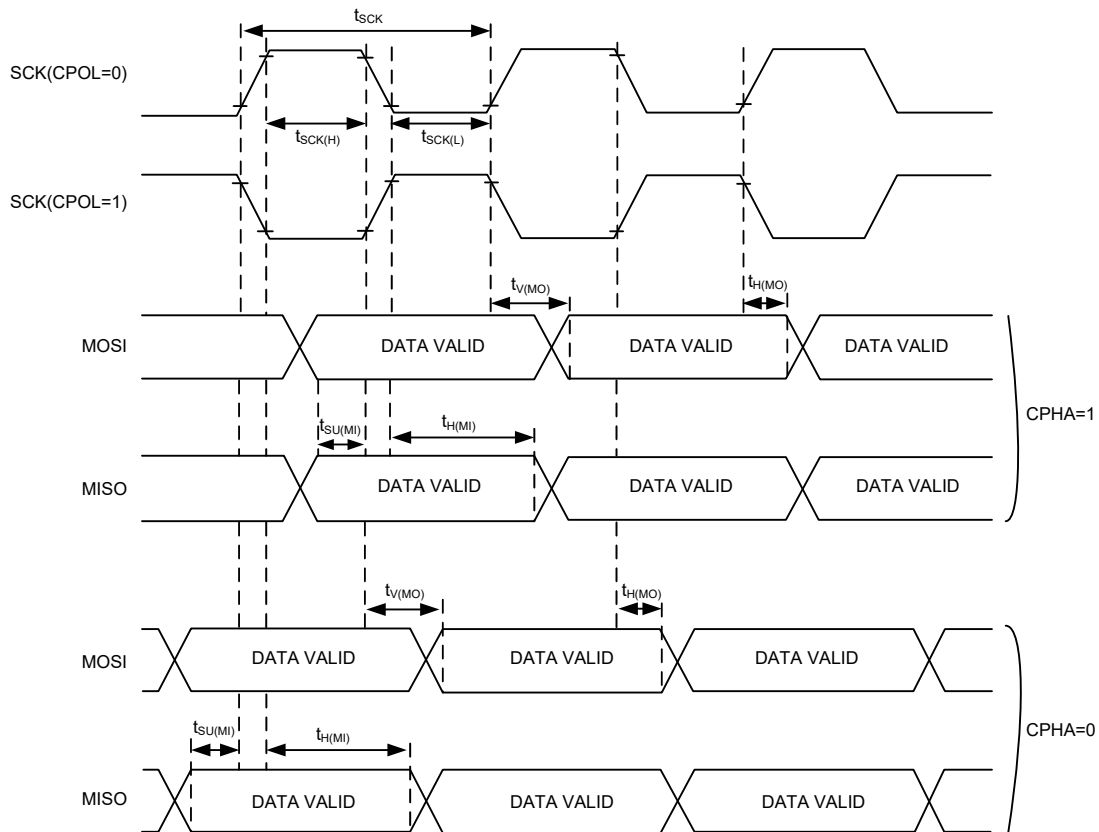


Figure 9. SPI Timing Diagrams – SPI Master Mode

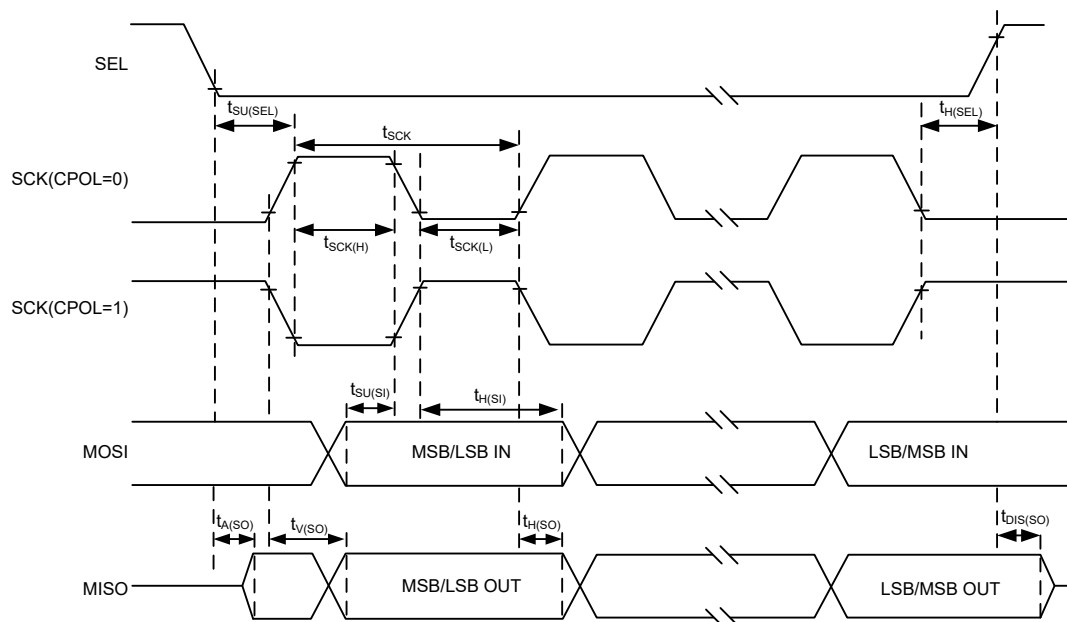


Figure 10. SPI Timing Diagrams – SPI Slave Mode with CPHA=1

I²S Characteristics

Table 23. I²S Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I²S Master Mode						
$t_{WSD(MO)}$	WS Output to BCLK Delay	—	—	TBD	—	ns
$t_{DOD(MO)}$	Data Output to BCLK Delay	—	—	TBD	—	ns
$t_{DIS(MI)}$	Data Input Setup Time	—	—	TBD	—	ns
$t_{DIH(MI)}$	Data Input Hold Time	—	—	TBD	—	ns
I²S Slave Mode						
$t_{BCH(SI)}$	BCLK High Pulse Width	—	—	TBD	—	ns
$t_{BCL(SI)}$	BCLK Low Pulse Width	—	—	TBD	—	ns
$t_{WSS(SI)}$	WS Input Setup Time	—	—	TBD	—	ns
$t_{DOD(SO)}$	Data Output to BCLK Delay	—	—	TBD	—	ns
$t_{DIS(SI)}$	Data Input Setup Time	—	—	TBD	—	ns
$t_{DIH(SI)}$	Data Input Hold Time	—	—	TBD	—	ns

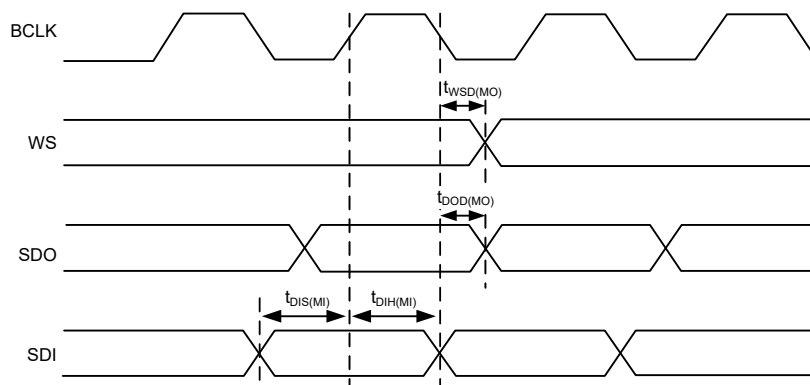


Figure 11. Timing of I²S Master Mode

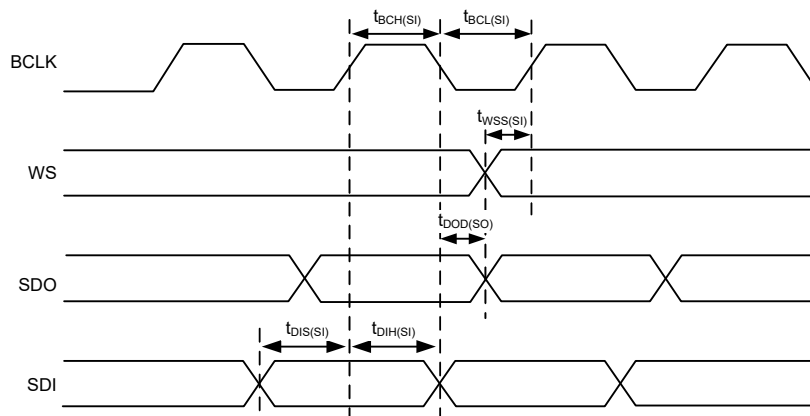


Figure 12. Timing of I²S Slave Mode

USB Characteristics

The USB interface is USB-IF certified - Full Speed.

Table 24. USB DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	USB Operating Voltage	—	3.0	—	3.6	V
V_{DI}	Differential Input Sensitivity	USBDP-USBDM	0.2	—	—	V
V_{CM}	Common Mode Voltage Range	—	0.8	—	2.5	V
V_{SE}	Single-ended Receiver Threshold	—	0.8	—	2.0	V
V_{OL}	Pad Output Low Voltage	R_L of 1.5 k Ω to V_{DD}	0	—	0.3	V
V_{OH}	Pad Output High Voltage		2.8	—	3.6	V
V_{CRS}	Differential Output Signal Cross-point Voltage		1.3	—	2.0	V
Z_{DRV}	Driver Output Resistance	—	—	10	—	Ω
C_{IN}	Transceiver Pad Capacitance	—	—	—	20	pF

Note: 1. Data based on characterization results only, not tested in production.

2. The USB functionality is ensured down to 2.7 V but not for the full USB electrical characteristics which will experience degradation in the 2.7 V to 3.0 V V_{DD} voltage range.

3. R_L is the load connected to the USB driver USBDP.

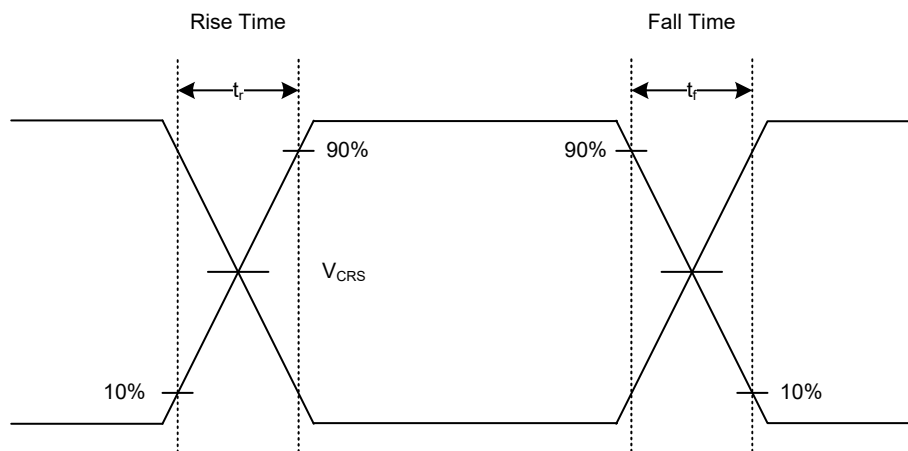


Figure 13. USB Signal Rise Time and Fall Time and Cross-Point Voltage (V_{CRS}) Definition

Table 25. USB AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_r	Rise Time	$C_L = 50$ pF	4	—	20	ns
t_f	Fall Time	$C_L = 50$ pF	4	—	20	ns
$t_{r/f}$	Rise Time / Fall Time Matching	$t_{r/f} = t_r / t_f$	90	—	110	%

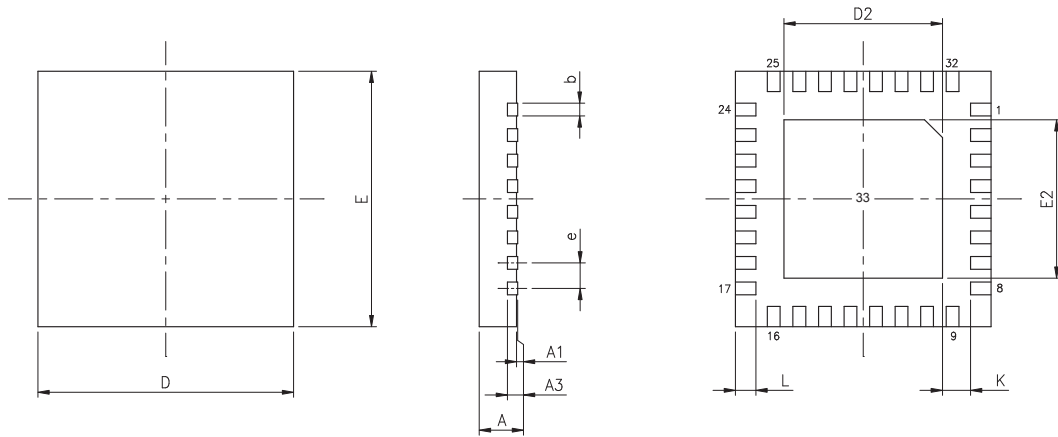
6 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the [Holtek website](#) for the latest version of the [Package Information](#).

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- [Package Information \(include Outline Dimensions, Product Tape and Reel Specifications\)](#)
- [The Operation Instruction of Packing Materials](#)
- [Carton information](#)

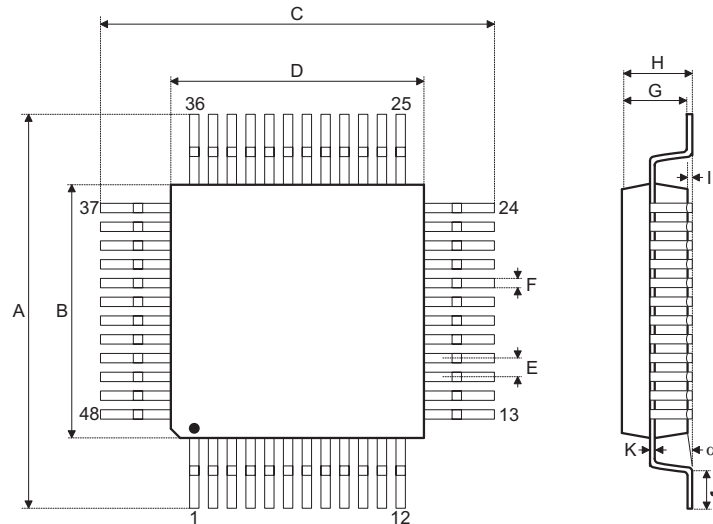
SAW Type 33-pin QFN (4mm × 4mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008 REF	—
b	0.006	0.008	0.010
D	—	0.157 BSC	—
E	—	0.157 BSC	—
e	—	0.016 BSC	—
D2	0.100	—	0.108
E2	0.100	—	0.108
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	—	0.203 REF	—
b	0.15	0.20	0.25
D	—	4.00 BSC	—
E	—	4.00 BSC	—
e	—	0.40 BSC	—
D2	2.55	—	2.75
E2	2.55	—	2.75
L	0.35	0.40	0.45
K	0.20	—	—

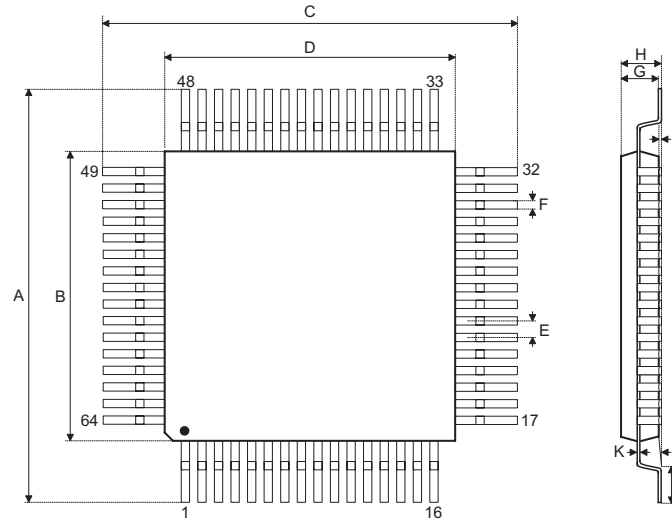
48-pin LQFP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.020 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.0 BSC	—
B	—	7.0 BSC	—
C	—	9.0 BSC	—
D	—	7.0 BSC	—
E	—	0.5 BSC	—
F	0.17	0.22	0.27
G	1.35	1.4	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

64-pin LQFP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.016 BSC	—
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.40 BSC	—
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

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