Glucose Meter Flash MCU with LCD

BH67F2470

Revision: V1.80   Date: June 14, 2023

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Features

CPU Features

- Operating Voltage
    - f_{SYS}=4MHz: 2.2V~5.5V
    - f_{SYS}=8MHz: 2.2V~5.5V
    - f_{SYS}=12MHz: 2.7V~5.5V
    - f_{SYS}=16MHz: 3.3V~5.5V
- Up to 0.25μs instruction cycle with 16MHz system clock at V_{DD}=5V
- Power down and wake-up functions to reduce power consumption
- Four Oscillators:
    - External High Speed Crystal – HXT
    - External 32.768kHz Crystal – LXT
    - Internal High Speed RC – HIRC
    - Internal 32kHz RC – LIRC
- Multi-mode operation: FAST, SLOW, IDLE and SLEEP
- Fully integrated internal oscillators require no external components
- All instructions executed in 1~3 instruction cycles
- Table read instructions
- 115 powerful instructions
- 8-level subroutine nesting
- Bit manipulation instruction

Peripheral Features

- Flash Program Memory: 32K×16
- RAM Data Memory: 768×8
- True EEPROM Memory: 64×8
- Watchdog Timer function
- In Application Programming – IAP
- 46 bidirectional I/O lines
- Programmable I/O port source current for LED applications
- 2 pin-shared external interrupts
- Multiple Timer Modules for time measure, input capture, compare match output, PWM output or single pulse output function
    - 1 Standard type 16-bit Timer Module – STM
    - 3 Periodic type 10-bit Timer Modules – PTM0~PTM2
- Dual Time-Base functions for generation of fixed time interrupt signals
- 4 external channels 12-bit resolution A/D Converter
- Internal Reference Voltage Generator
- 10-bit D/A Converter
- Internal Operational Amplifier
- Over Voltage Protection function with interrupt

- Serial Interface Module with SPI or I²C interface

- Single Serial Peripheral Interface – SPIA

- Two Fully-duplex Universal Asynchronous Receiver and Transmitter Interfaces

- 16-bit Multiplication Division Unit

- LCD Driver function

- Low Voltage Reset function

- Low Voltage Detect function

- Package types: 64/80-pin LQFP

General Description

The BH67F2470 is a Flash Memory A/D type 8-bit high performance RISC architecture microcontroller designed specifically for Glucose Meter with LCD display applications.

Offering users the convenience of Flash Memory multi-programming features, this device also includes a wide range of functions and features. Other memory includes an area of RAM Data Memory as well as an area of true EEPROM memory for storage of non-volatile data such as serial numbers, calibration data etc. By using the In Application Programming technoloty, users have a convenient means to directly store their measured data in the Flash Promgram Memory as well as having the ability to easily update their application programs.

Analog features include a multi-channel 12-bit A/D converter and an internal operational amplifier. Multiple and extremely flexible Timer Modules provide timing, pulse generation and PWM generation functions. Communication with the outside world is catered for by including fully integrated SPI or I²C, SPIA and UART interface functions, some popular interfaces which provide designers with a means of easy communication with external peripheral hardware. Protective features such as an internal Watchdog Timer, Low Voltage Reset and Low Voltage Detector coupled with excellent noise immunity and ESD protection ensure that reliable operation is maintained in hostile electrical environments.

A full choice of external, internal and high and low oscillator functions are provided including two fully integrated system oscillators which require no external components for their implementation. The ability to operate and switch dynamically between a range of operating modes using different clock sources gives users the ability to optimise microcontroller operation and minimise power consumption.

With regard to Glucose Meter applications, the device has integratd many of the functions required by these products. These include functions such as Internal Reference Voltage generator, 10-bit D/A Converter, LCD driver function, Over Voltage Protection, Multiplication/Division Unit etc. The inclusion of flexible I/O programming features, Time-Base functions along with many other features ensure that the device will be highly capable of providing MCU solutions for Glucose Meter applications which include an LCD display.

Block Diagram

Pin Assignment

BH67F2470/BH67V2470
64 LQFP-A

Left pins:
Pin	Name
1	PC4/$\overline{SCSA}$/RX1
2	PC5/SDOA/TX1
3	OPO
4	OPS0
5	OPS1
6	OPS2
7	OPN
8	PB7/VG
9	DACO
10	DACVREF
11	PLCD
12	PG0/C1/SEG45
13	PG1/C2/SEG46
14	V1
15	PG2/V2/SEG47
16	VMAX

Right pins:
Pin	Name
48	PB2/$\overline{SCS}$/SCKA/SEG41
47	PB3/SDO/SDIA/SEG40
46	PD7/SEG39
45	PD6/SEG38
44	PD5/SEG37
43	PD4/SEG36
42	PF7/SEG27
41	PF6/SEG26
40	PF5/SEG25
39	PF4/SEG24
38	PF3/SEG23
37	PF2/SEG22
36	PF1/SEG21
35	PF0/SEG20
34	SEG19
33	SEG18

Top pins (64–49):
- 64 PC1/AN3/PTCK1
- 63 PC0/AN2/PTP1/PTP1I
- 62 PC3/AN1/PTCK2
- 61 PC2/AN0/VREF/PTP2/PTP2I
- 60 VSS
- 59 PA0/XT1/PTP0/PTP0I/ICPDA/OCDSDA
- 58 PA2/XT2/PTCK0/ICPCK/OCDSCK
- 57 VDD
- 56 PA1/INT0/LVDIN/OVP/PVR/PTP0B/STCK
- 55 PA3/OSC2/SDOA/PTP1/PTP1I
- 54 PA4/OSC1/SCSA/PTP2/PTP2I
- 53 PA5/TX0/SCKA/STP/STPI
- 52 PA6/RX0/SDIA/STCK/OVPI
- 51 PA7/SDI/SDA/PTCK2/OVPI/SEG44
- 50 PB0/SCK/SCL/OVPI/SEG43
- 49 PB1/INT1/STPB/OVPI/SEG42

Bottom pins (17–32):
- 17 VDDIO
- 18 VSSIO
- 19 COM0
- 20 COM1
- 21 COM2
- 22 COM3
- 23 PD0/SEG0/COM4
- 24 PD1/SEG1/COM5
- 25 PD2/SEG2/COM6
- 26 PD3/SEG3/COM7
- 27 SEG4
- 28 SEG5
- 29 SEG6
- 30 SEG7
- 31 SEG16
- 32 SEG17

Left side pins (top to bottom):
PC4/SCSA/RX1 — 1
PC5/SDOA/TX1 — 2
OPO — 3
OPS0 — 4
OPS1 — 5
OPS2 — 6
OPN — 7
PB7/VG — 8
DACO — 9
DACVREF — 10
PLCD — 11
PG0/C1/SEG45 — 12
PG1/C2/SEG46 — 13
V1 — 14
PG2/V2/SEG47 — 15
VMAX — 16
VDDIO — 17
VSSIO — 18
COM0 — 19
COM1 — 20

Center label:
BH67F2470/BH67V2470
80 LQFP-A

Top side pins (left to right, pins 80–61):
PC1/AN3/PTCK1
PC0/AN2/PTP1/PTP1I
PC2/AN0/VREF/PTP2/PTP2I
PC3/AN1/PTCK2
PA2/XT2/PTCK0/ICPCK/OCDSCK
PA0/XT1/PTP0/PTP0I/ICPDA/OCDSDA
VSS
VDD
PA1/INT0/LVDIN/OVPVR/PTP0B/STCK
PA3/OSC2/SDOA/PTP1/PTP1
PA4/OSC1/SCSA/PTP2/PTP2I
PA5/TX0/SCKA/STP/STPI
PA6/RX0/SDIA/STCK/OVPI
PA7/SDI/SDA/PTCK2/OVPI/SEG44
PB0/SCK/SCL/OVPI/SEG43
PB1/INT1/STPB/OVPI/SEG42
PB2/SCS/SCKA/SEG41
PB3/SDO/SDIA/SEG40
PD7/SEG39
PD6/SEG38

Right side pins (top to bottom):
60 — PD5/SEG37
59 — PD4/SEG36
58 — PE7/SEG35
57 — PE6/SEG34
56 — PE5/SEG33
55 — PE4/SEG32
54 — PE3/SEG31
53 — PE2/SEG30
52 — PE1/SEG29
51 — PE0/SEG28
40 — PF7/SEG27
49 — PF6/SEG26
48 — PF5/SEG25
47 — PF4/SEG24
46 — PF3/SEG23
45 — PF2/SEG22
44 — PF1/SEG21
43 — PF0/SEG20
42 — SEG19
41 — SEG18

Bottom side pins (left to right, pins 21–40):
COM2
COM3
PD0/SEG0/COM4
PD1/SEG1/COM5
PD2/SEG2/COM6
PD3/SEG3/COM7
SEG4
SEG5
SEG6
SEG7
SEG8
SEG9
SEG10
SEG11
SEG12
SEG13
SEG14
SEG15
SEG16
SEG17

Note: 1. If the pin-shared pin functions have multiple outputs, the desired pin-shared function is determined by the corresponding software control bits.

2. The OCDSDA and OCDSCK pins are supplied as the OCDS dedicated pins and as such only available for the BH67V2470 device which is the OCDS EV chip for the BH67F2470 device.

3. For less pin-count package types there will be unbonded pins which should be properly configured to avoid unwanted current consumption resulting from floating input conditions. Refer to the "Standby Current Considerations" and "Input/Output Ports" sections.

Pin Description

With the exception of power and some LCD COM and SEG pins, all pins on the device can be referenced by its Port name, e.g. PA0, PA1 etc., which refer to the digital I/O function of the pins. However these Port pins are also shared with other functions such as the Analog to Digital Converter, Timer Modules etc. The function of each pin is listed in the following table, however the details behind how each pin is configured is contained in other sections of the datasheet.

Note that the pin description refers to the largest package size, as a result some pins may not exist on smaller package types.

Pin Name	Function	OPT	I/T	O/T	Description
PA0/XT1/PTP0/ PTP0I/ ICPDA/OCDSDA	PA0	PAPU PAWU PAS0	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	XT1	PAS0	LXT	—	LXT oscillator pin
	PTP0	IFS0 PAS0	—	CMOS	PTM0 ouput
	PTP0I	IFS0 PAS0	ST	—	PTM0 capture input
	ICPDA	—	ST	CMOS	ICP address/data pin
	OCDSDA	—	ST	CMOS	OCDS data/address pin, for EV chip only.
PA1/INT0/LVDIN/ OVPVR/PTP0B/ STCK	PA1	PAPU PAWU PAS0	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	INT0	PAS0 INTEG INTC0	ST	—	External interrupt 0 input
	LVDIN	PAS0	AN	—	LVD input
	OVPVR	PAS0	AN	—	OVP reference voltage input
	PTP0B	PAS0	—	CMOS	PTM0 inverting ouput
	STCK	PAS0 IFS0	ST	—	STM clock input
PA2/XT2/PTCK0/ ICPCK/OCDSCK	PA2	PAPU PAWU PAS0	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	XT2	PAS0	—	LXT	LXT oscillator pin
	PTCK0	PAS0	ST	—	PTM0 clock input
	ICPCK	—	ST	—	ICP clock pin
	OCDSCK	—	ST	—	OCDS clock pin, for EV chip only
PA3/OSC2/SDOA/ PTP1/PTP1I	PA3	PAPU PAWU PAS0	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	OSC2	PAS0	—	HXT	HXT oscillator pin
	SDOA	PAS0	—	CMOS	SPIA serial data output
	PTP1	PAS0	—	CMOS	PTM1 ouput
	PTP1I	PAS0 IFS0	ST	—	PTM1 capture input

Pin Name	Function	OPT	I/T	O/T	Description
PA4/OSC1/$\overline{SCSA}$/ PTP2/PTP2I	PA4	PAPU PAWU PAS1	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	OSC1	PAS1	HXT	—	HXT oscillator pin
	$\overline{SCSA}$	PAS1 IFS1	ST	CMOS	SPIA slave select
	PTP2	PAS1	—	CMOS	PTM2 ouput
	PTP2I	PAS1 IFS0	ST	—	PTM2 capture input
PA5/TX0/SCKA/ STP/STPI	PA5	PAPU PAWU PAS1	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TX0	PAS1 U0CR1 U0CR2	—	CMOS	UART0 data transmit pin
	SCKA	IFS1 PAS1	ST	CMOS	SPIA serial clock input
	STP	PAS1	—	CMOS	STM ouput
	STPI	PAS1	ST	—	STM capture input
PA6/RX0/SDIA/ STCK/OVPI	PA6	PAPU PAWU PAS1	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	RX0	IFS1 PAS1 U0CR1 U0CR2	ST	—	UART0 data receive pin
	SDIA	PAS1 IFS1	ST	—	SPIA serial data input
	STCK	PAS1 IFS0	ST	—	STM clock input
	OVPI	PAS1	AN	—	OVP signal input
PA7/SDI/SDA/ PTCK2/OVPI/ SEG44	PA7	PAPU PAWU PAS1	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	SDI	PAS1	ST	—	SIM SPI serial data input
	SDA	PAS1	ST	NMOS	SIM I^{2}C data line
	PTCK2	IFS1 PAS1	ST	—	PTM2 clock input
	OVPI	PAS1	AN	—	OVP signal input
	SEG44	PAS1	—	SEG	LCD segment output
PB0/SCK/SCL/ OVPI/SEG43	PB0	PBPU PBS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	SCK	PBS0	ST	CMOS	SIM SPI serial clock
	SCL	PBS0	ST	NMOS	SIM I^{2}C clock line
	OVPI	PBS0	AN	—	OVP signal input
	SEG43	PBS0	—	SEG	LCD segment output

Pin Name	Function	OPT	I/T	O/T	Description
PB1/INT1/STPB/ OVPI/SEG42	PB1	PBPU PBS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	INT1	PBS0 INTEG INTC0	ST	—	External interrupt input
	STPB	PBS0	—	CMOS	STM inverting ouput
	OVPI	PBS0	AN	—	OVP signal input
	SEG42	PBS0	—	SEG	LCD segment output
PB2/$\overline{SCS}$/SCKA/ SEG41	PB2	PBPU PBS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	$\overline{SCS}$	PBS0	ST	CMOS	SIM SPI slave chip select
	SCKA	IFS1 PBS0	ST	CMOS	SPIA serial clock
	SEG41	PBS0	—	SEG	LCD segment output
PB3/SDO/SDIA/ SEG40	PB3	PBPU PBS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	SDO	PBS0	—	CMOS	SIM SPI serial data output
	SDIA	PBS0 IFS1	ST	—	SPIA serial data input
	SEG40	PBS0	—	SEG	LCD segment output
PB7/VG	PB7	PBPU PBS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	VG	PBS1	AN	—	Virtual Ground
PC0/AN2/PTP1/ PTP1I	PC0	PCPU PCS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	AN2	PCS0	AN	—	A/D Converter external input channel 2
	PTP1	PCS0	—	CMOS	PTM1 ouput
	PTP1I	IFS0 PCS0	ST	—	PTM1 capture input
PC1/AN3/PTCK1	PC1	PCPU PCS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	AN3	PCS0	AN	—	A/D Converter external input channel 3
	PTCK1	PCS0	ST	—	PTM1 clock input
PC2/AN0/VREF/ PTP2/PTP2I	PC2	PCPU PCS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	AN0	PCS0	AN	—	A/D Converter external input channel 0
	VREF	PCS0	AN	—	A/D Converter external reference voltage input
	PTP2	PCS0	—	CMOS	PTM2 ouput
	PTP2I	IFS0 PCS0	ST	—	PTM2 capture input
PC3/AN1/PTCK2	PC3	PCPU PCS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	AN1	PCS0	AN	—	A/D Converter external input channel 1
	PTCK2	PCS0 IFS0	ST	—	PTM2 clock input
PC4/$\overline{SCSA}$/RX1	PC4	PCPU PCS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	$\overline{SCSA}$	PCS1 IFS1	ST	CMOS	SPIA slave chip select
	RX1	IFS1 PCS1 U1CR1 U1CR2	ST	—	UART1 data receive pin

Pin Name	Function	OPT	I/T	O/T	Description
PC5/SDOA/TX1	PC5	PCPU PCS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	SDOA	PCS1	—	CMOS	SPIA serial data output
	TX1	PCS1 U1CR1 U1CR2	—	CMOS	UART1 data transmit pin
PD0/SEG0/COM4	PD0	PDPU PDS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	SEG0	PDS0	—	SEG	LCD segment output
	COM4	PDS0	—	COM	LCD common output
PD1/SEG1/COM5	PD1	PDPU PDS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	SEG1	PDS0	—	SEG	LCD segment output
	COM5	PDS0	—	COM	LCD common output
PD2/SEG2/COM6	PD2	PDPU PDS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	SEG2	PDS0	—	SEG	LCD segment output
	COM6	PDS0	—	COM	LCD common output
PD3/SEG3/COM7	PD3	PDPU PDS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	SEG3	PDS0	—	SEG	LCD segment output
	COM7	PDS0	—	COM	LCD common output
PD4/SEG36	PD4	PDPU PDS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	SEG36	PDS1	—	SEG	LCD segment output
PD5/SEG37	PD5	PDPU PDS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	SEG37	PDS1	—	SEG	LCD segment output
PD6/SEG38	PD6	PDPU PDS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	SEG38	PDS1	—	SEG	LCD segment output
PD7/SEG39	PD7	PDPU PDS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	SEG39	PDS1	—	SEG	LCD segment output
PE0/SEG28~ PE7/SEG35	PE0~PE7	PEPU PES0/ PES1	ST	CMOS	General purpose I/O. Register enabled pull-up
	SEG28~ SEG35	PES0/ PES1	—	SEG	LCD segment output
PF0/SEG20~ PF7/SEG27	PF0~PF7	PFPU PFS0/ PFS1	ST	CMOS	General purpose I/O. Register enabled pull-up
	SEG20~ SEG27	PFS0/ PFS1	—	SEG	LCD segment output
PG0/C1/SEG45	PG0	PGPU PGS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	C1	PGS0	AN	—	LCD voltage pump
	SEG45	PGS0	—	SEG	LCD segment output
PG1/C2/SEG46	PG1	PGPU PGS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	C2	PGS0	AN	—	LCD voltage pump
	SEG46	PGS0	—	SEG	LCD segment output

Pin Name	Function	OPT	I/T	O/T	Description
PG2/V2/SEG47	PG2	PGPU PGS0	ST	CMOS	General purpose I/O. Register enabled pull-up
	V2	PGS0	PWR	AN	LCD voltage pump
	SEG47	PGS0	—	SEG	LCD segment output
COM0~COM3	COMn	—	—	COM	LCD common output
SEG4~SEG19	SEGn	—	—	SEG	LCD segment output
VMAX	VMAX	—	PWR	—	IC maximum voltage, connected to VDD or V1
PLCD	PLCD	—	PWR	AN	LCD power supply
V1	V1	—	PWR	AN	LCD voltage pump
OPN	OPN	—	AN	—	OPA negative input
OPS0	OPS0	—	AN	—	OPA external resistor 0
OPS1	OPS1	—	AN	—	OPA external resistor 1
OPS2	OPS2	—	AN	—	OPA external resistor 2
OPO	OPO	—	—	AN	OPA output
DACVREF	DACVREF	—	—	AN	DAC Reference Voltage output
DACO	DACO	—	—	AN	DAC Output
VDDIO	VDDIO	—	PWR	—	Positive power supply
VSSIO	VSSIO	—	PWR	—	Negative power supply, ground.
VDD	VDD	—	PWR	—	Positive power supply
VSS	VSS	—	PWR	—	Negative power supply, ground.

Legend: I/T: Input type;   O/T: Output type;
OPT: Optional by register option;   PWR: Power;
ST: Schmitt Trigger input;   CMOS: CMOS output;
NMOS: NMOS output;   AN: Analog signal;
SEG: LCD SEG output;   COM: LCD COM output;
HXT: High frequency crystal oscillator;
LXT: Low frequency crystal oscillator.

Absolute Maximum Ratings

Supply Voltage .... V_{SS}−0.3V to V_{SS}+6.0V

Input Voltage .... V_{SS}−0.3V to V_{DD}+0.3V

Storage Temperature..-60°C to 150°C

Operating Temperature...-40°C to 85°C

I_{OL} Total 80mA

I_{OH} Total ....-80mA

Total Power Dissipation 500mW

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of the device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Electrical Characteristics

For data in the following tables, note that factors such as oscillator type, operating voltage, operating frequency, pin load conditions, temperature and program instruction type, can all exert an influence on the measured values.

Operating Voltage Characteristics

Ta=-40°C~85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating voltage (HXT)	—	$f_{SYS}=f_{HXT}=4MHz$	2.2	—	5.5	V
			$f_{SYS}=f_{HXT}=8MHz$	2.2	—	5.5	
			$f_{SYS}=f_{HXT}=12MHz$	2.7	—	5.5	
			$f_{SYS}=f_{HXT}=16MHz$	3.3	—	5.5	
	Operating voltage (HIRC)	—	$f_{SYS}=f_{HIRC}=4MHz$	2.2	—	5.5	V
			$f_{SYS}=f_{HIRC}=8MHz$	2.2	—	5.5	
			$f_{SYS}=f_{HIRC}=12MHz$	2.7	—	5.5	
	Operating voltage (LXT)	—	$f_{SYS}=f_{LXT}=32.768kHz$	2.2	—	5.5	V
	Operating voltage (LIRC)	—	$f_{SYS}=f_{LIRC}=32kHz$	2.2	—	5.5	V

Operating Current Characteristics

Ta=25°C

Symbol	Normal Operation	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
I_{DD}	SLOW Mode (LIRC)	3V	$f_{SYS}=32kHz$	—	10	20	µA
		5V		—	30	50	
	SLOW Mode (LXT)	3V	$f_{SYS}=f_{LXT}=32768Hz$	—	10	20	µA
		5V		—	30	50	
	FAST Mode (HIRC)	3V	$f_{SYS}=f_{HIRC}=4MHz$	—	0.4	0.6	mA
		5V		—	0.8	1.2	
		3V	$f_{SYS}=f_{HIRC}=8MHz$	—	0.8	1.2	mA
		5V		—	1.6	2.4	
		3V	$f_{SYS}=f_{HIRC}=12MHz$	—	1.2	1.8	mA
		5V		—	2.4	3.6	
	FAST Mode (HXT)	3V	$f_{SYS}=f_{HXT}=4MHz$	—	0.5	0.75	mA
		5V		—	1.0	1.5	
		3V	$f_{SYS}=f_{HXT}=8MHz$	—	1.0	1.5	mA
		5V		—	2.0	3.0	
		3V	$f_{SYS}=f_{HXT}=12MHz$	—	1.5	2.75	mA
		5V		—	3.0	4.5	
		5V	$f_{SYS}=f_{HXT}=16MHz$	—	4.0	6.0	mA

Note: When using the characteristic table data, the following notes should be taken into consideration:

1. Any digital input is setup in a non-floating condition.

2. All measurements are taken under conditions of no load and with all peripherals in an off state.

3. There are no DC current paths.

4. All Operating Current values are measured using a continuous NOP instruction program loop.

Standby Current Characteristics

Ta=25°C

Symbol	Standby Mode	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
I_{STB}	SLEEP Mode	3V	WDT off	—	0.11	0.15	μA
		5V		—	0.18	0.38	
		3V	WDT on	—	1.5	3.0	μA
		5V		—	3.0	5.0	
	IDLE0 Mode (LIRC / LXT)	3V	f_{SUB} on	—	2.0	3.0	μA
		5V		—	3.0	5.0	
	IDLE1 Mode (HIRC)	3V	f_{SUB} on, f_{SYS}=4MHz	—	250	360	μA
		5V		—	450	720	
		3V	f_{SUB} on, f_{SYS}=8MHz	—	420	600	μA
		5V		—	800	1200	
		3V	f_{SUB} on, f_{SYS}=12MHz	—	600	900	μA
		5V		—	1200	1800	
	IDLE1 Mode (HXT)	3V	f_{SUB} on, f_{SYS}=4MHz	—	250	360	μA
		5V		—	450	720	
		3V	f_{SUB} on, f_{SYS}=8MHz	—	420	600	μA
		5V		—	800	1200	
		3V	f_{SUB} on, f_{SYS}=12MHz	—	600	900	μA
		5V		—	1200	1800	
		5V	f_{SUB} on, f_{SYS}=16MHz	—	1.8	2.4	mA

Note: When using the characteristic table data, the following notes should be taken into consideration:
1. Any digital input is setup in a non-floating condition.
2. All measurements are taken under conditions of no load and with all peripherals in an off state.
3. There are no DC current paths.
4. All Standby Current values are taken after a HALT instruction executed thus stopping all instruction execution.

A.C. Electrical Characteristics

For data in the following tables, note that factors such as oscillator type, operating voltage, operating frequency and temperature, can all exert an influence on the measured values.

High Speed Internal Oscillator Frequency Accuracy

During the program writing operation the writer will trim the HIRC oscillator at a user selected HIRC frequency and user selected voltage of either 3V or 5V.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Temp.				
f_{HIRC}	4MHz Writer Trimmed HIRC Frequency	3V/5V	25°C	- 1.0%	4	+1.0%	MHz
			-40°C~85°C	-2.0%	4	+2.0%	
		2.2V~5.5V	25°C	-2.5%	4	+2.5%	
			-40°C~85°C	-3.0%	4	+3.0%	
	8MHz Writer Trimmed HIRC Frequency	3V/5V	25°C	-1.0%	8	+1.0%	MHz
			-40°C~85°C	-2.0%	8	+2.0%	
		2.2V~5.5V	25°C	-2.5%	8	+2.5%	
			-40°C~85°C	-3.0%	8	+3.0%	

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_DD	Temp.				
f_HIRC	12MHz Writer Trimmed HIRC Frequency	5V	25°C	-1.0%	12	+1.0%	MHz
			-40°C~85°C	-2.0%	12	+2.0%	
		2.7V~5.5V	25°C	-2.5%	12	+2.5%	
			-40°C~85°C	-3.0%	12	+3.0%	

Note: 1. The 3V/5V values for V_DD are provided as these are the two selectable fixed voltages at which the HIRC frequency is trimmed by the writer.

   2. The row below the 3V/5V trim voltage row is provided to show the values for the full V_DD range operating voltage. It is recommended that the trim voltage is fixed at 3V for application voltage ranges from 2.2V to 3.6V and fixed at 5V for application voltage ranges from 3.3V to 5.5V.

   3. The minimum and maximum tolerance values provided in the table are only for the frequency at which the writer trims the HIRC oscillator. After trimming at this chosen specific frequency any change in HIRC oscillator frequency using the oscillator register control bits by the application program will give a frequency tolerance to within ±20%.

Low Speed Internal Oscillator Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_DD	Temp.				
f_LIRC	LIRC Frequency	2.2V~5.5V	25°C	-5%	32	+5%	kHz
		3V	-40°C~85°C	-10%	32	+10%	
t_START	LIRC Start Up Time	—	—	—	—	100	µs

Operating Frequency Characteristic Curves

System Start Up Time Characteristics

Ta=-40°C~85°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{SST}	System Start-up Time (Wake-up from condition where f_{SYS} is off)	$f_{SYS}=f_H \sim f_H/64$, $f_H=f_{HXT}$	128	—	—	t_{HXT}
		$f_{SYS}=f_H \sim f_H/64$, $f_H=f_{HIRC}$	16	—	—	t_{HIRC}
		$f_{SYS}=f_{SUB}=f_{LXT}$	1024	—	—	t_{LXT}
		$f_{SYS}=f_{SUB}=f_{LIRC}$	2	—	—	t_{LIRC}
	System Start-up Time Wake-up from condition where f_{SYS} is on.	$f_{SYS}=f_H \sim f_H/64$, $f_H=f_{HXT}$ or f_{HIRC}	2	—	—	t_H
		$f_{SYS}=f_{SUB}=f_{LXT}$ or f_{LIRC}	2	—	—	t_{SUB}
	System Speed Switch Time (FAST Mode ↔ SLOW Mode or $f_H=f_{HXT} \leftrightarrow f_{HIRC}$ or $f_{SUB}=f_{LXT} \leftrightarrow f_{LIRC}$)	f_{HXT} switches from off → on	1024	—	—	t_{HXT}
		f_{HIRC} switches from off → on	16	—	—	t_{HIRC}
		f_{LXT} switches from off → on	1024	—	—	t_{LXT}
t_{RSTD}	System Reset Delay Time (Power-on reset or LVR hardware reset)	RR_{POR}=5V/ms	42	48	54	ms
	System Reset Delay Time (LVRC/WDTC/RSTC software reset)	—				
	System Reset Delay Time (WDT overflow reset)	—	14	16	18	ms
t_{SRESET}	Minimum Software Reset Width to Reset	—	45	90	120	µs

Note: 1. For the System Start-up time values, whether f_{SYS} is on or off depends upon the mode type and the chosen f_{SYS} system oscillator. Details are provided in the System Operating Modes section.

2. The time units, shown by the symbols t_{HXT}, t_{HIRC} etc. are the inverse of the corresponding frequency values as provided in the frequency tables. For example $t_{HIRC}=1/f_{HIRC}$, $t_{SYS}=1/f_{SYS}$ etc.

3. If the LIRC is used as the system clock and if it is off when in the SLEEP Mode, then an additional LIRC start up time, t_{START}, as provided in the LIRC frequency table, must be added to the t_{SST} time in the table above.

4. The System Speed Switch Time is effectively the time taken for the newly activated oscillator to start up.

Input/Output Characteristics

Ta=-40°C~85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{IL}	Input Low Voltage for I/O Ports	5V	—	0	—	1.5	V
		—	—	0	—	$0.2V_{DD}$	
V_{IH}	Input High Voltage for I/O Ports	5V	—	3.5	—	5	V
		—	—	$0.8V_{DD}$	—	V_{DD}	
I_{OL}	Sink Current for I/O Ports	3V	V_{OL}=0.1V_{DD}	16	32	—	mA
		5V		32	65	—	
I_{OH}	Source current for I/O ports	3V	V_{OH}=0.9V_{DD}, SLEDCn[m+1, m]=00B (n=0, 1, 2, 3; m=0, 2, 4, 6)	-0.7	-1.5	—	mA
		5V		-1.5	-2.9	—	
		3V	V_{OH}=0.9V_{DD}, SLEDCn[m+1, m]=01B (n=0, 1, 2, 3; m=0, 2, 4, 6)	-1.3	-2.5	—	mA
		5V		-2.5	-5.1	—	
		3V	V_{OH}=0.9V_{DD}, SLEDCn[m+1, m]=10B (n=0, 1, 2, 3; m=0, 2, 4, 6)	-1.8	-3.6	—	mA
		5V		-3.6	-7.3	—	
		3V	V_{OH}=0.9V_{DD}, SLEDCn[m+1, m]=11B (n=0, 1, 2, 3; m=0, 2, 4, 6)	-4	-8	—	mA
		5V		-8	-16	—	

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{OL}	Output Low Voltage for I/O Ports	3V	I_{OL}=16mA	—	—	0.3	V
		5V	I_{OL}=32mA	—	—	0.5	V
V_{OH}	Output High Voltage for I/O Ports	3V	I_{OH}=-0.7mA, SLEDCn[m+1, m]=00B (n=0, 1, 2, 3; m=0, 2, 4, 6)	2.7	—	—	V
		5V	I_{OH}=-1.5mA, SLEDCn[m+1, m]=00B (n=0, 1, 2, 3; m=0, 2, 4, 6)	4.5	—	—	V
		3V	I_{OH}=-1.3mA, SLEDCn[m+1, m]=01B (n=0, 1, 2, 3; m=0, 2, 4, 6)	2.7	—	—	V
		5V	I_{OH}=-2.5mA, SLEDCn[m+1, m]=01B (n=0, 1, 2, 3; m=0, 2, 4, 6)	4.5	—	—	V
		3V	I_{OH}=-1.8mA, SLEDCn[m+1, m]=10B (n=0, 1, 2, 3; m=0, 2, 4, 6)	2.7	—	—	V
		5V	I_{OH}=-3.6mA, SLEDCn[m+1, m]=10B (n=0, 1, 2, 3; m=0, 2, 4, 6)	4.5	—	—	V
		3V	I_{OH}=-4mA, SLEDCn[m+1, m]=11B (n=0, 1, 2, 3; m=0, 2, 4, 6)	2.7	—	—	V
		5V	I_{OH}=-8mA, SLEDCn[m+1, m]=11B (n=0, 1, 2, 3; m=0, 2, 4, 6)	4.5	—	—	V
R_{PH}	Pull-high Resistance for I/O Ports[Note]	3V	—	20	60	100	kΩ
		5V	—	10	30	50	
I_{LEAK}	Input Leakage Current	3V	V_{IN}=V_{DD} or V_{SS}	—	—	±1	μA
		5V		—	—	±1	
t_{TCK}	PTCKn, STCK Input Pin Minimum Pulse Width	—	—	0.3	—	—	μs
t_{TPI}	PTPnI, STPI Input Pin Minimum Pulse Width	—	—	0.3	—	—	μs
t_{INT}	External Interrupt Minimum Pulse Width	—	—	10	—	—	μs

Note: The R_{PH} internal pull high resistance value is calculated by connecting to ground and enabling the input pin with a pull-high resistor and then measuring the input sink current at the specified supply voltage level. Dividing the voltage by this measured current provides the R_{PH} value.

Memory Characteristics

Ta=-40°C~85°C, unless otherwise specify

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{RW}	V_{DD} for Read / Write	—	—	V_{DDmin}	—	V_{DDmax}	V
Program Flash / Data EEPROM Memory							
t_{DEW}	Erase / Write Cycle Time – Flash Program Memory	—	—	—	2	3	ms
	Write Cycle Time – Data EEPROM Memory	—	—	—	4	6	ms
I_{DDPGM}	Programming / Erase current on V_{DD}	—	—	—	—	5.0	mA
E_P	Cell Endurance – Flash Program Memory	—	—	10K	—	—	E/W
	Cell Endurance – Data EEPROM Memory	—	—	100K	—	—	E/W
t_{RETD}	ROM Data Retention time	—	Ta=25°C	—	40	—	Year
RAM Data Memory							
V_{DR}	RAM Data Retention voltage	—	—	1.0	—	—	V

LVR/LVD Electrical Characteristics

Ta=-40°C~85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.2	—	5.5	V
V_{LVR}	Low Voltage Reset Voltage	—	LVR enable, voltage select 2.10V	-5%	2.10	+5%	V
		—	LVR enable, voltage select 2.55V		2.55		
		—	LVR enable, voltage select 3.15V		3.15		
		—	LVR enable, voltage select 3.80V		3.80		
V_{LVD}	Low Voltage Detection Voltage	—	LVD enable, voltage select 1.04V	-10%	1.04	+10%	V
		—	LVD enable, voltage select 2.20V	-5%	2.20	+5%	
		—	LVD enable, voltage select 2.40V		2.40		
		—	LVD enable, voltage select 2.70V		2.70		
		—	LVD enable, voltage select 3.00V		3.00		
		—	LVD enable, voltage select 3.30V		3.30		
		—	LVD enable, voltage select 3.60V		3.60		
		—	LVD enable, voltage select 4.00V		4.00		
$I_{LVRLVDBG}$	Operating Current	3V	LVD enable, LVR enable, VBGEN=0	—	—	18	µA
		5V		—	20	25	
		3V	LVD enable, LVR enable, VBGEN=1	—	—	150	µA
		5V		—	180	200	
I_{LVR}	Additional Current for LVR Enable	—	LVD disable, VBGEN=0	—	—	24	µA
I_{LVD}	Additional Current for LVD Enable	—	LVR disable, VBGEN=0	—	—	24	µA
t_{LVDS}	LVDO Stable Time	—	For LVR enable, VBGEN=0, LVD off → on	—	—	15	µs
		—	For LVR disable, VBGEN=0, LVD off → on	—	—	150	µs
t_{LVR}	Minimum Low Voltage Width to Reset	—	—	120	240	480	µs
t_{LVD}	Minimum Low Voltage Width to Interrupt	—	—	60	120	240	µs
I_{BG}	Additional Current for Bandgap Reference Enable	—	LVR disable, LVD disable	—	—	180	µA
V_{BG}	Bandgap Reference Voltage	—	—	-5%	1.25	+5%	V
t_{BGS}	V_{BG} Turn On Stable Time	—	—	—	—	150	µs

Note: If V_{LVD} select 1.04V, it is used to detect the LVDIN pin input voltage. Other V_{LVD} choices are used to detect the power supply V_{DD}.

OVP Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
I_{OVP}	Operating Current	5V	OVPEN=1, DAC V_{REF}=2.5V	—	280	400	µA
V_{OS}	Input Offset Voltage	5V	With calibration	-4	—	4	mV
V_{HYS}	Hysteresis	5V	—	20	40	60	mV
V_{CM}	Common Mode Voltage Range	5V	—	V_{SS}	—	V_{DD} - 1.4	V
Ro	R2R Output Resistance	5V	—	—	10	—	kΩ
DNL	Differential Non-linearity	5V	DAC V_{REF}=V_{DD}	—	—	±1	LSB
INL	Integral Non-linearity	5V	DAC V_{REF}=V_{DD}	—	—	±1.5	LSB

LCD Characteristics

Ta=-40°C~85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{IN}	LCD Operating Voltage	—	Power supply from PLCD pin (for R type)	3.0	—	5.5	V
		—	Power supply from PLCD pin (for C type)	2.0	—	3.7	V
		—	Power supply from V1 pin (for C type)	3.0	—	5.5	V
		—	Power supply from V2 pin (for C type)	1.0	—	1.8	V
		—	Power supply from V_A (for C type)	3.0	—	5.5	V
		3.3V~5.5V	Power supply from V_B (for C type)	-10%	3.0	+10%	V
		2.2V~5.5V	Power supply from V_C (for C type)	-10%	1.08	+10%	V
I_{LCD1}	Additional Current for LCD Enable(R type), LCD Clock=4kHz	5V	No load, VA=PLCD=V_{DD}, 1/3 Bias, RCT=0, LCDPR=0, LCDIS[1:0]=00B	—	25	37.5	µA
			No load, VA=PLCD=V_{DD}, 1/4 Bias, RCT=0, LCDPR=0, LCDIS[1:0]=00B	—	18	28	µA
			No load, VA=PLCD=V_{DD}, 1/3 Bias, RCT=0, LCDPR=0, LCDIS[1:0]=01B	—	50	75	µA
			No load, VA=PLCD=V_{DD}, 1/4 Bias, RCT=0, LCDPR=0, LCDIS[1:0]=01B	—	37.5	56	µA
			No load, VA=PLCD=V_{DD}, 1/3 Bias, RCT=0, LCDPR=0, LCDIS[1:0]=10B	—	100	150	µA
			No load, VA=PLCD=V_{DD}, 1/4 Bias, RCT=0, LCDPR=0, LCDIS[1:0]=10B	—	75	112.5	µA
			No load, VA=PLCD=V_{DD}, 1/3 Bias, RCT=0, LCDPR=0, LCDIS[1:0]=11B	—	200	300	µA
			No load, VA=PLCD=V_{DD}, 1/4 Bias, RCT=0, LCDPR=0, LCDIS[1:0]=11B	—	150	225	µA
	Additional Current for LCD Enable(C type)	3V	No load, V_A=V1=V_{DD}, 1/3 Bias	—	10	15	µA
		5V		—	13.5	20	
I_{LCDOL}	LCD Common and Segment Sink Current	3V	V_{OL}=0.1V_{DD}	210	420	—	µA
		5V		350	700	—	
I_{LCDOH}	LCD Common and Segment Source Current	3V	V_{OH}=0.9V_{DD}	-80	-160	—	µA
		5V		-180	-360	—	
V_{LCD}	PLCD Comes from Charge Pump	2.2V~5.5V	RCT=0, LCDPR=1, CPVS[1:0]=00B	-10%	3.3	+10%	V
			RCT=0, LCDPR=1, CPVS[1:0]=01B		3.0		
			RCT=0, LCDPR=1, CPVS[1:0]=10B		2.7		
			RCT=0, LCDPR=1, CPVS[1:0]=11B		4.5		

OPA Electrical Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
I_{OPA}	OPA Operating Current	3V	$V_P=V_N=1/2\ V_{DD}$	—	—	650	µA
A_{OL}	OPA Open Loop Gain	3V	—	80	100	—	dB
Ro	Output Resistance	2.4V~3.6V	Ta=0°C~50°C, R_{LOAD}=50kΩ 0.2V < V_{OP} < V_{DD} -1.4V (Voltage Follower Configuration)	—	—	260	Ω
I_{OS}	Input Offset Current	2.4V~3.6V	Ta=0°C~50°C	—	±5	—	nA
TC	Temperature Coefficient of Offset Voltage	3V	Ta=0°C~50°C	—	—	±0.2	µV/°C
GBW	Gain Bandwidth	3V	R_L=1MΩ, C_L=60pf, V_{IN}=V_{CM}/2	100	—	—	kHz
V_{OS}	Input Offset Voltage	3V	Without calibration	-15	—	15	mV
V_{CM}	OPA Common Mode Voltage Range	3V	—	0.1	—	V_{DD} -1.4	V
V_{OR}	OPA Maximum Output Voltage Range	3V	—	V_{SS} +0.1	—	V_{DD} -0.1	V
t_{START}	OPA Turn On Stable Time	—	—	—	—	150	µs

Internal Reference Voltage Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{IREF}	Internal Reference Voltage	3V	IREFEN=1, PVREF[7:0]=10000000B	-3%	2.0	+3%.	V
I_{IREF}	Additional Current for Internal Reference Voltage Enable	—	IREFEN=1	—	650	850	µA
TC_{IREF}	Temperature Coefficient of Internal Reference Voltage	3V	Ta=10°C~40°C	—	±40	—	ppm/°C

Analog Switch Electrical Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
R_{OP}	On Resistance (OPS0, OPS1 or OPS2)	3V	Ta=10°C~40°C, (I_{SW}=200µA)	—	—	1300	Ω
R_{VG}	On Resistance (VG)	3V	Ta=10°C~40°C, GSW3=1	—	—	20	Ω
I_{LEAK}	Leakage Current(VG)	3V	Ta=10°C~40°C	—	±0.5	—	nA

10-bit D/A Converter Electrical Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
DNL	Differential Non-linearity	3V	—	—	—	±7	LSB
INL	Integral Non-linearity	3V	—	—	—	±12	LSB
V_{DACO}	Output Voltage Range	—	—	0.00	—	1.00	1/2 $V_{DACVREF}$
V_{DACO_RIPPLE}	Output Voltage Ripple	3V	DACVRS[1:0]=10B	-0.6	—	+0.6	mV

A/D Converter Electrical Characteristics

Ta= -40°C~85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	—	5.5	V
V_{ADI}	Input Voltage	—	—	0	—	V_{REF}	V
V_{REF}	Reference Voltage	—	—	2	—	V_{DD}	V
DNL	Differential Non-linearity	3V	$V_{REF}=V_{DD}$, $t_{ADCK}=0.5\mu s$	—	—	±3	LSB
		5V					
		3V	$V_{REF}=V_{DD}$, $t_{ADCK}=10\mu s$				
		5V					
INL	Integral Non-linearity	3V	$V_{REF}=V_{DD}$, $t_{ADCK}=0.5\mu s$	—	—	±4	LSB
		5V					
		3V	$V_{REF}=V_{DD}$, $t_{ADCK}=10\mu s$				
		5V					
I_{ADC}	Additional Current Consumption for A/D Converter Enable	3V	No load ($t_{ADCK}=0.5\mu s$)	—	1	2	mA
		5V		—	1.5	3	
t_{ADCK}	Clock Period	—	—	0.5	—	10	µs
t_{ON2ST}	A/D Converter on-to-start Time	—	—	4	—	—	µs
t_{ADS}	Sampling Time	—	—	—	4	—	t_{ADCK}
t_{ADC}	Conversion Time (Including A/D Sample and Hold Time)	—	—	—	16	—	t_{ADCK}

Power-on Reset Characteristics

Ta=25°C

| Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	—	—	—	—	100	mV
RR_{POR}	V_{DD} Rising Rate to Ensure Power-on Reset	—	—	0.035	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} Stays at V_{POR} to Ensure Power-on Reset	—	—	1	—	—	ms
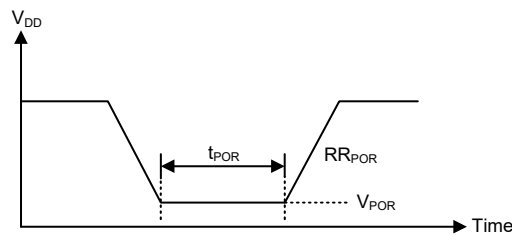
System Architecture

A key factor in the high-performance features of the range of microcontrollers is attributed to their internal system architecture. The device takes advantage of the usual features found within RISC microcontrollers providing increased speed of operation and enhanced performance. The pipelining scheme is implemented in such a way that instruction fetching and instruction execution are overlapped, hence instructions are effectively executed in one or two cycles for most of the standard or extended instructions respectively. The exceptions to this are branch or call instructions which need one more cycle. An 8-bit wide ALU is used in practically all instruction set operations, which carries out arithmetic operations, logic operations, rotation, increment, decrement, branch decisions, etc. The internal data path is simplified by moving data through the Accumulator and the ALU. Certain internal registers are implemented in the Data Memory and can be directly or indirectly addressed. The simple addressing methods of these registers along with additional architectural features ensure that a minimum of external components is required to provide a functional I/O and A/D control system with maximum reliability and flexibility. This makes the device suitable for low-cost, high-volume production for controller applications.
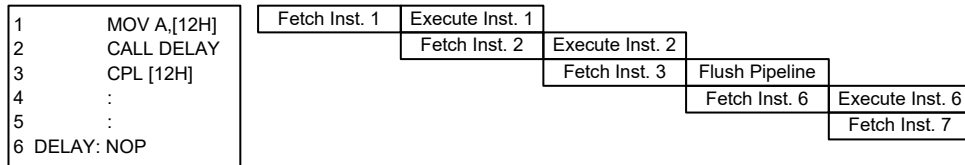
Clocking and Pipelining

The main system clock, derived from either a HXT, LXT, HIRC or LIRC oscillator is subdivided into four internally generated non-overlapping clocks, T1~T4. The Program Counter is incremented at the beginning of the T1 clock during which time a new instruction is fetched. The remaining T2~T4 clocks carry out the decoding and execution functions. In this way, one T1~T4 clock cycle forms one instruction cycle. Although the fetching and execution of instructions takes place in consecutive instruction cycles, the pipelining structure of the microcontroller ensures that instructions are effectively executed in one instruction cycle. The exception to this are instructions where the contents of the Program Counter are changed, such as subroutine calls or jumps, in which case the instruction will take one more instruction cycle to execute.
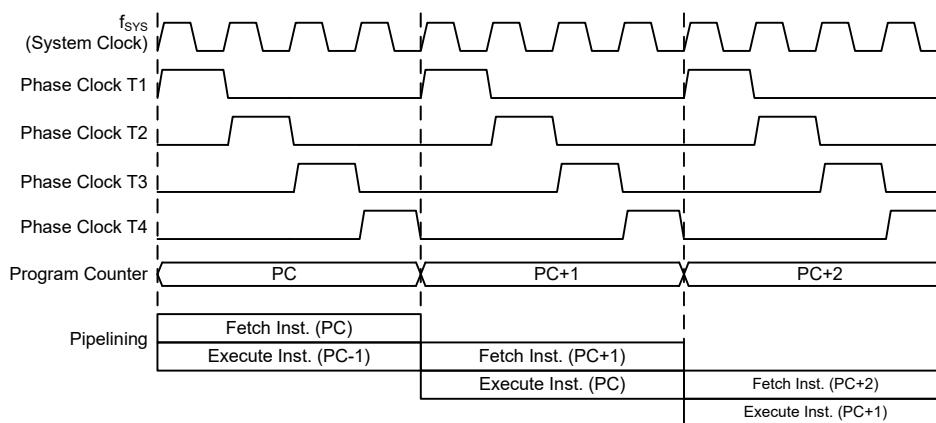
System Clocking and Pipelining

For instructions involving branches, such as jump or call instructions, two machine cycles are required to complete instruction execution. An extra cycle is required as the program takes one cycle to first obtain the actual jump or call address and then another cycle to actually execute the branch. The requirement for this extra cycle should be taken into account by programmers in timing sensitive applications.

1	MOV A,[12H]
2	CALL DELAY
3	CPL [12H]
4	:
5	:
6 DELAY: NOP	

```
Fetch Inst. 1   Execute Inst. 1
      Fetch Inst. 2   Execute Inst. 2
            Fetch Inst. 3   Flush Pipeline
                  Fetch Inst. 6   Execute Inst. 6
                        Fetch Inst. 7
```

Instruction Fetching

Program Counter

During program execution, the Program Counter is used to keep track of the address of the next instruction to be executed. It is automatically incremented by one each time an instruction is executed except for instructions, such as "JMP" or "CALL" that demands a jump to a non-consecutive Program Memory address. Only the lower 8 bits, known as the Program Counter Low Register, are directly addressable by the application program. As the device Program Memory is divided into four Banks, the PBP register is provided for selecting the required program memory bank.

When executing instructions requiring jumps to non-consecutive addresses such as a jump instruction, a subroutine call, interrupt or reset, etc., the microcontroller manages program control by loading the required address into the Program Counter. For conditional skip instructions, once the condition has been met, the next instruction, which has already been fetched during the present instruction execution, is discarded and a dummy cycle takes its place while the correct instruction is obtained.
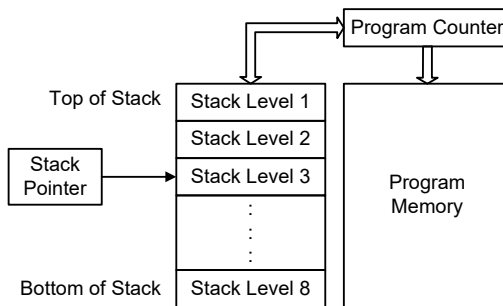
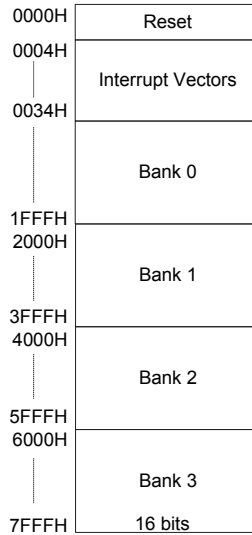| Program Counter	
Program Counter High Byte	**Program Counter Low Register**
PBP1~PBP0, PC12~PC8	PCL7~PCL0

Program Counter

The lower byte of the Program Counter, known as the Program Counter Low register or PCL, is available for program control and is a readable and writeable register. By transferring data directly into this register, a short program jump can be executed directly. However, as only this low byte is available for manipulation, the jumps are limited to the present page of memory, that is 256 locations. When such program jumps are executed it should also be noted that a dummy cycle will be inserted. Manipulating the PCL register may cause program branching, so an extra cycle is needed to pre-fetch.

Stack

This is a special part of the memory which is used to save the contents of the Program Counter only. The stack is organized into 8 levels and is neither part of the data nor part of the program space, and is neither readable nor writeable. The activated level is indexed by the Stack Pointer, and is neither readable nor writeable. At a subroutine call or interrupt acknowledge signal, the contents of the Program Counter are pushed onto the stack. At the end of a subroutine or an interrupt routine, signaled by a return instruction, RET or RETI, the Program Counter is restored to its previous value from the stack. After a device reset, the Stack Pointer will point to the top of the stack.

```
                              ┌──────────────────┐
                    ┌────────▶│ Program Counter  │
                    │    │    └──────────────────┘
                    │    ▼              ║
  Top of Stack   ┌──────────────┐   ┌──────────────┐
                 │ Stack Level 1│   │              │
                 ├──────────────┤   │              │
                 │ Stack Level 2│   │              │
  ┌───────┐      ├──────────────┤   │   Program    │
  │ Stack │─────▶│ Stack Level 3│   │   Memory     │
  │Pointer│      ├──────────────┤   │              │
  └───────┘      │      :       │   │              │
                 │      :       │   │              │
                 │      :       │   │              │
                 ├──────────────┤   │              │
  Bottom of Stack│ Stack Level 8│   └──────────────┘
                 └──────────────┘
```

If the stack is full and an enabled interrupt takes place, the interrupt request flag will be recorded but the acknowledge signal will be inhibited. When the Stack Pointer is decremented, by RET or RETI, the interrupt will be serviced. This feature prevents stack overflow allowing the programmer to use the structure more easily. However, when the stack is full, a CALL subroutine instruction can still be executed which will result in a stack overflow. Precautions should be taken to avoid such cases which might cause unpredictable program branching. If the stack is overflow, the first Program Counter save in the stack will be lost.

Arithmetic and Logic Unit – ALU

The arithmetic-logic unit or ALU is a critical area of the microcontroller that carries out arithmetic and logic operations of the instruction set. Connected to the main microcontroller data bus, the ALU receives related instruction codes and performs the required arithmetic or logical operations after which the result will be placed in the specified register. As these ALU calculation or operations may result in carry, borrow or other status changes, the status register will be correspondingly updated to reflect these changes. The ALU supports the following functions:

- Arithmetic operations: ADD, ADDM, ADC, ADCM, SUB, SUBM, SBC, SBCM, DAA, LADD, LADDM, LADC, LADCM, LSUB, LSUBM, LSBC, LSBCM, LDAA

- Logic operations: AND, OR, XOR, ANDM, ORM, XORM, CPL, CPLA, LAND, LANDM, LOR, LORM, LXOR, LXORM, LCPL, LCPLA

- Rotation: RRA, RR, RRCA, RRC, RLA, RL, RLCA, RLC, LRR, LRRA, LRRCA, LRRC, LRLA, LRL, LRLCA, LRLC

- Increment and Decrement: INCA, INC, DECA, DEC, LINCA, LINC, LDECA, LDEC

- Branch decision: JMP, SZ, SZA, SNZ, SIZ, SDZ, SIZA, SDZA, CALL, RET, RETI, LSNZ, LSZ, LSZA, LSIZ, LSIZA, LSDZ, LSDZA

Flash Program Memory

The Program Memory is the location where the user code or program is stored. For this device the Program Memory is Flash type, which means it can be programmed and re-programmed a large number of times, allowing the user the convenience of code modification on the same device. By using the appropriate programming tools, the Flash device offers users the flexibility to conveniently debug and develop their applications while also offering a means of field programming and updating.

Structure

The Program Memory has a capacity of 32K×16 bits. The Program Memory is addressed by the Program Counter and also contains data, table information and interrupt entries. Table data, which can be setup in any location within the Program Memory, is addressed by a separate table pointer register.

The Program Memory is divided into four banks which are Bank0, Bank1, Bank2 and Bank3. The required Bank is selected using bit1~bit0 of the PBP register.

```
0000H    Reset
0004H
         Interrupt Vectors
0034H

         Bank 0

1FFFH
2000H
         Bank 1

3FFFH
4000H
         Bank 2

5FFFH
6000H
         Bank 3
7FFFH    16 bits
```

Program Memory Structure

Special Vectors

Within the Program Memory, certain locations are reserved for the reset and interrupts. The location 0000H is reserved for use by the device reset for program initialisation. After a device reset is initiated, the program will jump to this location and begin execution.

Look-up Table

Any location within the Program Memory can be defined as a look-up table where programmers can store fixed data. To use the look-up table, the table pointer must first be setup by placing the address of the look up data to be retrieved in the table pointer registers, TBLP and TBHP. These registers define the total address of the look-up table.

After setting up the table pointer, the table data can be retrieved from the Program Memory using the corresponding table read instruction such as "TABRD [m]" or "TABRDL [m]" respectively when the memory [m] is located in sector 0. If the memory [m] is located in other sectors, the data can be retrieved from the program memory using the corresponding extended table read instruction such as "LTABRD [m]" or "LTABRDL [m]" respectively. When the instruction is executed, the lower order table byte from the Program Memory will be transferred to the user defined Data Memory register [m] as specified in the instruction. The higher order table data byte from the Program Memory will be transferred to the TBLH special register.

The accompanying diagram illustrates the addressing data flow of the look-up table.

```
                                    Program Memory
  Last Page or
  TBHP Register  ─┐        ┌──────┬──────────────┐
                  ├──────► │Address│   Data       │
  TBLP Register  ─┘        │      │  16 bits      │
                           └──────┴──────────────┘
                                  │        │
                          ┌───────┘        └───────┐
                          ▼                         ▼
                 ┌─────────────┐         ┌─────────────┐
                 │Register TBLH│         │User Selected│
                 │             │         │  Register   │
                 └─────────────┘         └─────────────┘
                   High Byte                Low Byte
```
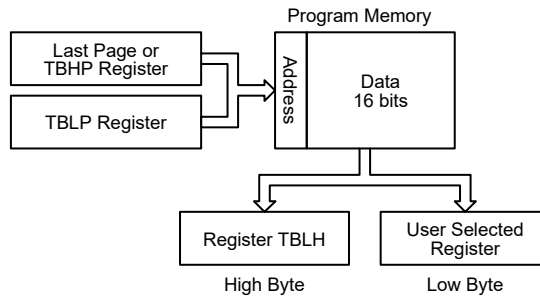
Table Program Example

The following example shows how the table pointer and table data is defined and retrieved from the microcontroller. This example uses raw table data located in the Program Memory which is stored there using the ORG statement. The value at this ORG statement is "1F00H" which refers to the start address of the last page in Bank 3 within the 32K Program Memory of the device. The table pointer low byte register is setup here to have an initial value of "06H". This will ensure that the first data read from the data table will be at the Program Memory address "7F06H" or 6 locations after the start of the last page. Note that the value for the table pointer is referenced to the first address specified by TBLP and TBHP if the "TABRD [m]" or "LTABRD [m]" instruction is being used. The high byte of the table data which in this case is equal to zero will be transferred to the TBLH register automatically when the "TABRD [m]" or "LTABRD [m]" instruction is executed.

Because the TBLH register is a read/write register and can be restored, care should be taken to ensure its protection if both the main routine and Interrupt Service Routine use table read instructions. If using the table read instructions, the Interrupt Service Routines may change the value of the TBLH and subsequently cause errors if used again by the main routine. As a rule it is recommended that simultaneous use of the table read instructions should be avoided. However, in situations where simultaneous use cannot be avoided, the interrupts should be disabled prior to the execution of any main routine table-read instructions. Note that all table related instructions require two instruction cycles to complete their operation.

Table Read Program Example

```
rombank3 code1
ds .section'data'
tempreg1 db ?        ; temporary register #1
tempreg2 db ?        ; temporary register #2
code0 .section 'code'
mov a,06h            ; initialise low table pointer - note that this address is referenced
mov tblp,a           ; to the last page or the page that tbhp pointed
mov a,07Fh           ; initialise high table pointer
mov tbhp,a           ; it is not necessary to set tbhp if executing tabrdl or ltabrdl
:
:
tabrd tempreg1       ; transfers value in table referenced by table pointer data at program
                     ; memory address "7F06H" transferred to tempreg1 and TBLH
dec tblp             ; reduce value of table pointer by one
tabrd tempreg2       ; transfers value in table referenced by table pointer
                     ; data at program memory address "7F05H" transferred to
                     ; tempreg2 and TBLH in this example the data "1AH" is
                     ; transferred to tempreg1 and data "0FH" to register tempreg2
:
:
code1 .section 'code'
org 1F00h            ; sets initial address of program memory last page
dc 00Ah, 00Bh, 00Ch, 00Dh, 00Eh, 00Fh, 01Ah, 01Bh
```

In Circuit Programming – ICP

The provision of Flash type Program Memory provides the user with a means of convenient and easy upgrades and modifications to their programs on the same device. As an additional convenience, a means of programming the microcontroller in-circuit has provided using a 4-pin interface. This provides manufacturers with the possibility of manufacturing their circuit boards complete with a programmed or un-programmed microcontroller, and then programming or upgrading the program at a later stage. This enables product manufacturers to easily keep their manufactured products supplied with the latest program releases without removal and re-insertion of the device.

The Flash MCU to Writer Programming Pin correspondence table is as follows:

Holtek Writer Pins	MCU Programming Pins	Pin Description
ICPDA	PA0	Programming Serial Data/Address
ICPCK	PA2	Programming Clock
VDD	VDD	Power Supply
VSS	VSS	Ground

The Program Memory can be programmed serially in-circuit using this 4-wire interface. Data is downloaded and uploaded serially on a single pin with an additional line for the clock. Two additional lines are required for the power supply. The technical details regarding the in-circuit programming of the device are beyond the scope of this document and will be supplied in supplementary literature.

During the programming process, taking control of the ICPDA and ICPCK pins for data and clock programming purposes. The user must there take care to ensure that no other outputs are connected to these two pins.
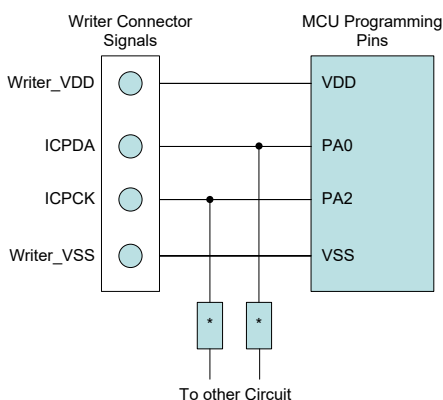
Note: * may be resistor or capacitor. The resistance of * must be greater than 1kΩ or the capacitance of * must be less than 1nF.

In Application Programming – IAP

This device offers IAP function to update data or application program to Flash ROM. Users can define any ROM location for IAP, but there are some features which users must notice in using IAP function.

Configurations	
Erase Page	64 words / page
Writing Word	64 words / time
Reading Word	1 word / time

In Application Programming Control Registers

The Address registers, FARL and FARH, and the Data registers, FD0L/FD0H, FD1L/FD1H, FD2L/FD2H, FD3L/FD3H, together with the Control registers, FC0, FC1 and FC2 are the corresponding Flash access registers for IAP and all located in Data Memory Sector 1. If using indirect addressing to access all these registers, all read and write operations to the registers must be performed using the Indirect Addressing Register, IAR1 or IAR2, and the Memory Pointer pair, MP1L/MP1H or MP2L/MP2H. Because the data, address and control registers are located at the address of 43H~4FH in Data Memory Sector 1, the desired value ranged from 43H~4FH must be written into the MP1L or MP2L Memory Pointer low byte and the value "01H" must also be written into the MP1H or MP2H Memory Pointer high byte.

Register Name	Bit							
	7	6	5	4	3	2	1	0
FC0	CFWEN	FMOD2	FMOD1	FMOD0	FWPEN	FWT	FRDEN	FRD
FC1	D7	D6	D5	D4	D3	D2	D1	D0
FC2	—	—	—	—	—	—	—	CLWB
FARL	A7	A6	A5	A4	A3	A2	A1	A0
FARH	—	A14	A13	A12	A11	A10	A9	A8
FD0L	D7	D6	D5	D4	D3	D2	D1	D0
FD0H	D15	D14	D13	D12	D11	D10	D9	D8
FD1L	D7	D6	D5	D4	D3	D2	D1	D0
FD1H	D15	D14	D13	D12	D11	D10	D9	D8
FD2L	D7	D6	D5	D4	D3	D2	D1	D0
FD2H	D15	D14	D13	D12	D11	D10	D9	D8
FD3L	D7	D6	D5	D4	D3	D2	D1	D0
FD3H	D15	D14	D13	D12	D11	D10	D9	D8

IAP Register List

- **FC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	CFWEN	FMOD2	FMOD1	FMOD0	FWPEN	FWT	FRDEN	FRD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7   **CFWEN**: Flash Memory Write enable control

         0: Flash Memory write function is disabled

         1: Flash Memory write function has been successfully enabled

When this bit is cleared to 0 by application program, the Flash Memory write function is disabled. Note that writing a "1" into this bit results in no action. This bit is used to indicate that the Flash Memory write function status. When this bit is set to 1 by hardware, it means that the Flash Memory write function is enabled successfully. Otherwise, the Flash Memory write function is disabled as the bit content is zero.

Bit 6~4   **FMOD2~FMOD0**: Mode selection

         000: Write Program ROM

         001: Page erase Program ROM

         010: Reserved

         011: Read Program ROM

         100: Reserved

         101: Reserved

         110: FWEN (Flash ROM Write Enable) mode

         111: Reserved

Bit 3   **FWPEN**: Flash ROM Write procedure enable control

         0: Disable

         1: Enable

When this bit is set to 1 and the FMOD field is set to "110", the IAP controller will execute the "Flash ROM Write Enable" procedure. Once the Flash memory write function is successfully enabled, it is not necessary to set the FWPEN bit any more. This bit can be set by software only, when 300μs counter overflows, hardware will clear the FWPEN bit.

Bit 2   **FWT**: Flash ROM Write control bit

         0: Do not initiate Flash ROM Write or Flash ROM Write process is completed

         1: Initiate Flash ROM write process

This bit can be set by software only, when the write process is completed, hardware will clear the FWT bit.

Bit 1   **FRDEN**: Flash ROM Read enabled bit
        0: Flash ROM read disable
        1: Flash ROM read enable

Bit 0   **FRD**: Flash ROM Read control bit
        0: Do not initiate Flash ROM Read or Flash ROM Read process is completed
        1: Initiate Flash ROM Read process
      This bit can be set by software only, when the read process is completed, hardware will clear the FRD bit.

- **FC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   whole chip reset control
      When users write 55H to this register, it will generate a reset signal to reset whole chip.

- **FC2 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	CLWB
R/W	—	—	—	—	—	—	—	R/W
POR	—	—	—	—	—	—	—	0

Bit 7~1   Unimplemented, read as "0"

Bit 0   **CLWB**: Flash ROM Write Buffer clear control
        0: Do not initiate Write Buffer Clear or Write Buffer Clear process is completed
        1: Initiate Write Buffer Clear process
      This bit can be set by software only, when the clear write buffer process is completed, hardware will clear the CLWB bit.

- **FARL Register**

Bit	7	6	5	4	3	2	1	0
Name	A7	A6	A5	A4	A3	A2	A1	A0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   Flash ROM Address [7:0]

- **FARH Register**

Bit	7	6	5	4	3	2	1	0
Name	—	A14	A13	A12	A11	A10	A9	A8
R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	0	0	0	0	0	0	0

Bit 7   Unimplemented, read as "0"

Bit 6~0   Flash ROM Address [14:8]

- **FD0L Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   The first Flash ROM data [7:0]
      Note that the data written into the low byte data register FD0L will only be stored in the FD0L register and not loaded into the lower 8-bit write buffer.

- **FD0H Register**

Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   The first Flash ROM data [15:8]

Note that when the 8-bit data is written into the high byte data register FD0H, the whole 16-bit data stored in the FD0H and FD0L register pair will simultaneously be loaded into the 16-bit write buffer and then the content of the Flash Memory address register pair, FARH and FARL, will be incremented by one.

- **FD1L Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   The second Flash ROM data [7:0]

- **FD1H Register**

Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   The second Flash ROM data [15:8]

- **FD2L Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   The third Flash ROM data [7:0]

- **FD2H Register**

Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   The third Flash ROM data [15:8]

- **FD3L Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   The fourth Flash ROM data [7:0]

- **FD3H Register**

Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   The fourth Flash ROM data [15:8]

Flash Memory Write Function Enable Procedure

In order to allow users to change the Flash ROM data through the IAP control registers, users must first enable the Flash Memory Write operation by the following procedure:

Step 1. Write "110" into the FMOD2~FMOD0 bits to select the FWEN mode.

Step 2. Set the FWPEN bit to "1". The step 1 and step 2 can be executed simultaneously.

Step 3. The pattern data with a sequence of 00H, 04H, 0DH, 09H, C3H and 40H must be written into the FD1L, FD1H, FD2L, FD2H, FD3L and FD3H registers respectively.

Step 4. A counter with a time-out period of 300μs will be activated to allow users writing the correct pattern data into the FD1L/FD1H~FD3L/FD3H register pairs. The counter clock is derived from the f$_{SUB}$ clock.

Step 5. If the counter overflows or the pattern data is incorrect, the Flash ROM Write operation will not be enabled and users must again repeat the above procedure. Then the FWPEN bit will automatically be cleared to 0 by hardware when 300μs counter overflows.

Step 6. If the pattern data is correct before the counter overflows, the Flash ROM Write operation will be enabled. The CFWEN bit will also be set to 1 by hardware to indicate that the Flash ROM Write operation is successfully enabled.

Step 7. Once the Flash ROM write operation is enabled, the user can change the Flash ROM data through the Flash control registers.

Step 8. To disable the Flash ROM Write operation, the user can clear the CFWEN bit to 0.
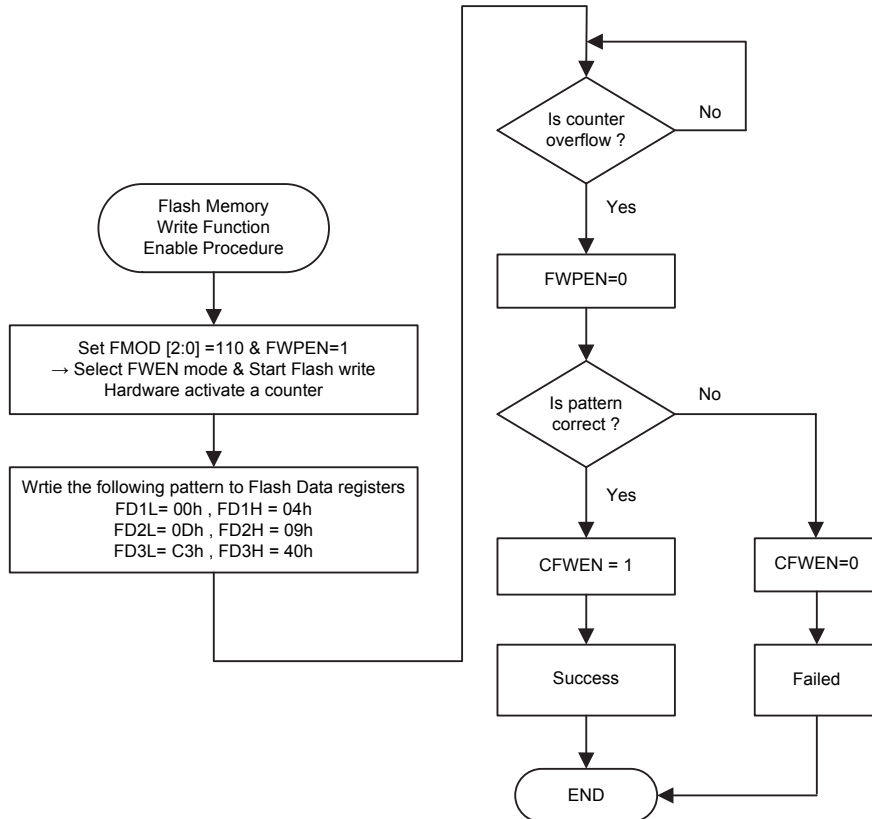
Flash ROM Write Function Enable Procedure

Flash ROM Read/Write Procedure

After the Flash ROM Write function is successfully enabled through the preceding IAP procedure, users must first erase the corresponding Flash ROM page and then initiate the Flash ROM write operation. For the device the number of the page erase operation is 64 words per page, the available page erase address is only specified by FARH register and the content of the FARL[7:6] bit field.

Erase Page	FARH	FARL[7:6]	FARL[5:0]
0	0000 0000	00	
1	0000 0000	01	
2	0000 0000	10	
3	0000 0000	11	
4	0000 0001	00	
5	0000 0001	01	xx xxxx
: :	: :	: :	
510	0111 1111	10	
511	0111 1111	11	

"x": don't care

Erase Page Number and Selection
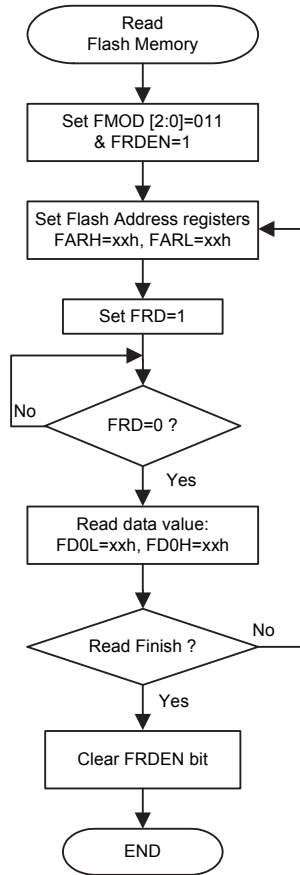
Read Flash ROM Procedure
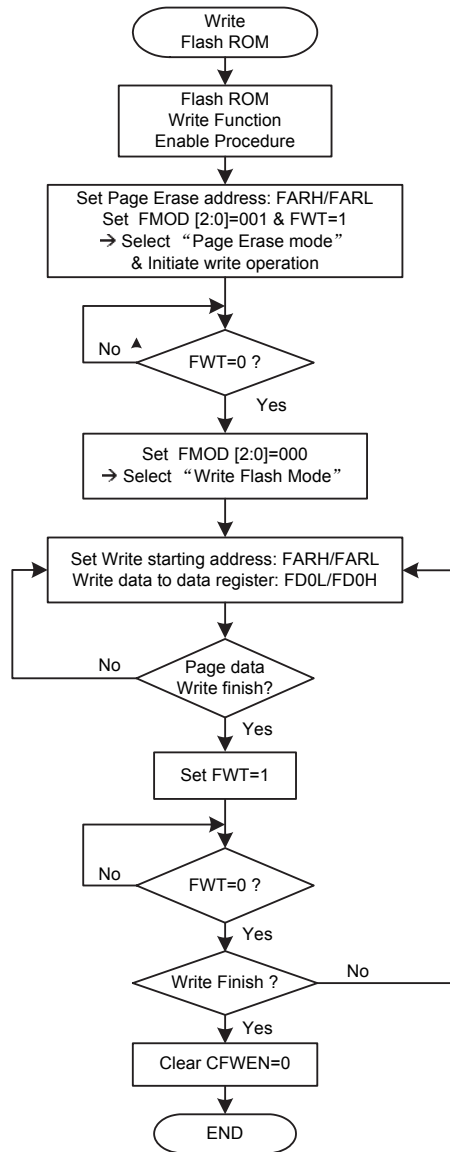
Write Flash ROM Procedure

On-Chip Debug Support – OCDS

An EV chip exists for the purposes of device emulation. This EV chip device also provides an "On-Chip Debug" function to debug the device during the development process. The EV chip and the actual MCU device are almost functionally compatible except for the "On-Chip Debug" function. Users can use the EV chip device to emulate the real chip device behavior by connecting the OCDSDA and OCDSCK pins to the HT-IDE development tools. The OCDSDA pin is the OCDS Data/Address input/output pin while the OCDSCK pin is the OCDS clock input pin. When users use the EV chip for debugging, other functions which are shared with the OCDSDA and OCDSCK pins in the actual MCU device will have no effect in the EV chip. However, the two OCDS pins which are pin-shared with the ICP programming pins are still used as the Flash Memory programming pins for ICP. For a more detailed OCDS description, refer to the corresponding document.

e-Link Pins	EV Chip Pins	Pin Description
OCDSDA	OCDSDA	On-chip Debug Support Data/Address input/output
OCDSCK	OCDSCK	On-chip Debug Support Clock input
VDD	VDD	Power Supply
VSS	VSS	Ground

RAM Data Memory

The Data Memory is a volatile area of 8-bit wide RAM internal memory and is the location where temporary information is stored.

Categorised into two types, the first of these is an area of RAM named Special Purpose Data Memory where special function registers are located. These registers have fixed locations and are necessary for correct operation of the device. Many of these registers can be read from and written to directly under program control, however, some remain protected from user manipulation. The second area of Data Memory named General Purpose Data Memory is reserved for general purpose use. All locations within this area are read and write accessible under program control.

There is an area of the Data Memory is reserved for the LCD Memory. This area is mapped directly to the LCD display so data written into this memory area will directly affect the displayed data. The addresses of the LCD Memory area overlap those in the area of 00H~2FH of Sector 4. Switching between the different Data Memory Sectors is achieved by setting the Memory Pointers high byte to correct value.

Structure

The Data Memory is subdivided into several sectors, all of which are implemented in 8-bit wide RAM. Each of the Data Memory Sector is categorized into two types, the special Purpose Data Memory and the General Purpose Data Memory. The address range of the Special Purpose Data Memory for the device is from 00H to 7FH while the General Purpose Data Memory address range is from 80H to FFH.

Special Purpose Data Memory	General Purpose Data Memory		LCD Display Data Memory
Located Sectors	Capacity	Sector: Address	Sector: Address
0, 1	768×8	0: 80H~FFH 1: 80H~FFH 2: 80H~FFH 3: 80H~FFH 4: 80H~FFH 5: 80H~FFH	4: 00H~2FH

Data Memory Summary

Data Memory Structure
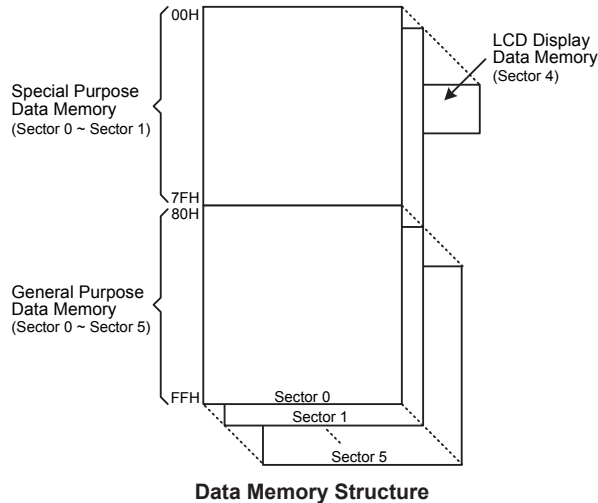
Data Memory Addressing

For this device that supports the extended instructions, there is no Bank Pointer for Data Memory Sectors selection. The desired Sector is pointed by the MP1H or MP2H register and the certain Data Memory address in the selected sector is specified by the MP1L or MP2L register when using indirect addressing access.

Direct Addressing can be used in all sectors using the extended instruction which can address all available data memory space. For the accessed data memory which is located in any data memory sector except sector 0, the extended instructions can be used to access the data memory instead of using the indirect addressing access. The main difference between standard instructions and extended instructions is that the data memory address "m" in the extended instructions has 11 valid bits for this device, the high byte indicates a sector and the low byte indicates a specific address.

General Purpose Data Memory

All microcontroller programs require an area of read/write memory where temporary data can be stored and retrieved for use later. It is this area of RAM memory that is known as General Purpose Data Memory. This area of Data Memory is fully accessible by the user programing for both reading and writing operations. By using the bit operation instructions individual bits can be set or reset under program control giving the user a large range of flexibility for bit manipulation in the Data Memory.

Special Purpose Data Memory

This area of Data Memory is where registers, necessary for the correct operation of the microcontroller, are stored. Most of the registers are both readable and writeable but some are protected and are readable only, the details of which are located under the relevant Special Function Register section. Note that for locations that are unused, any read instruction to these addresses will return the value "00H".

	Sector 0	Sector 1			Sector 0	Sector 1
00H	IAR0			40H		EEC
01H	MP0			41H	EEA	
02H	IAR1			42H	EED	
03H	MP1L			43H		FC0
04H	MP1H			44H	U1SR	FC1
05H	ACC			45H	U1CR1	FC2
06H	PCL			46H	U1CR2	FARL
07H	TBLP			47H	TXR_RXR1	FARH
08H	TBLH			48H	BRG1	FD0L
09H	TBHP			49H	STMC0	FD0H
0AH	STATUS			4AH	STMC1	FD1L
0BH	PBP			4BH	STMDL	FD1H
0CH	IAR2			4CH	STMDH	FD2L
0DH	MP2L			4DH	STMAL	FD2H
0EH	MP2H			4EH	STMAH	FD3L
0FH	RSTFC			4FH	STMRP	FD3H
10H	SCC			50H	PTM0C0	IFS0
11H	HIRCC			51H	PTM0C1	IFS1
12H	HXTC			52H	PTM0DL	
13H	LXTC			53H	PTM0DH	PAS0
14H	PA			54H	PTM0AL	PAS1
15H	PAC			55H	PTM0AH	PBS0
16H	PAPU			56H	PTM0RPL	PBS1
17H	PAWU			57H	PTM0RPH	PCS0
18H	RSTC			58H		PCS1
19H	LVRC			59H	MDUWR0	PDS0
1AH	LVDC			5AH	MDUWR1	PDS1
1BH	MFI0			5BH	MDUWR2	PES0
1CH	MFI1			5CH	MDUWR3	PES1
1DH	MFI2			5DH	MDUWR4	PFS0
1EH	WDTC			5EH	MDUWR5	PFS1
1FH	INTEG			5FH	MDUWCTRL	PGS0
20H	INTC0	PTM1C0		60H	OVPC0	SLEDC0
21H	INTC1	PTM1C1		61H	OVPC1	SLEDC1
22H	INTC2	PTM1DL		62H	OVPDA	SLEDC2
23H	INTC3	PTM1DH		63H		SLEDC3
24H	PB	PTM1AL		64H	SADOL	
25H	PBC	PTM1AH		65H	SADOH	
26H	PBPU	PTM1RPL		66H	SADC0	
27H	PC	PTM1RPH		67H	SADC1	
28H	PCC	PTM2C0		68H	IREFC	
29H	PCPU	PTM2C1		69H	PVREF	
2AH		PTM2DL		6AH	OPAC	
2BH		PTM2DH		6BH	GSC	
2CH	PSCR	PTM2AL		6CH	AFEDAC	
2DH	TB0C	PTM2AH		6DH	AFEDAL	
2EH	TB1C	PTM2RPL		6EH	AFEDAH	
2FH	U0SR	PTM2RPH		6FH		
30H	U0CR1			70H	LCDC0	
31H	U0CR2			71H	LCDCP	
32H	TXR_RXR0			72H	LCDC2	
33H	BRG0			73H		
34H	SIMC0			74H	PD	
35H	SIMC1			75H	PDC	
36H	SIMD			76H	PDPU	
37H	SIMA/SIMC2			77H	PE	
38H	SIMTOC			78H	PEC	
39H				79H	PEPU	
3AH	SPIAC0			7AH	PF	
3BH	SPIAC1			7BH	PFC	
3CH	SPIAD			7CH	PFPU	
3DH				7DH	PG	
3EH				7EH	PGC	
3FH				7FH	PGPU	

☐ : Unused, read as 00H

Special Purpose Data Memory

Special Function Register Description

Most of the Special Function Register details will be described in the relevant functional sections however several registers require a separate description in this section.

Indirect Addressing Registers – IAR0, IAR1, IAR2

The Indirect Addressing Registers, IAR0, IAR1 and IAR2, although having their locations in normal RAM register space, do not actually physically exist as normal registers. The method of indirect addressing for RAM data manipulation uses these Indirect Addressing Registers and Memory Pointers, in contrast to direct memory addressing, where the actual memory address is specified. Actions on the IAR0, IAR1 and IAR2 registers will result in no actual read or write operation to these registers but rather to the memory location specified by their corresponding Memory Pointers, MP0, MP1L/MP1H or MP2L/MP2H. Acting as a pair, IAR0 and MP0 can together access data only from Sector 0 while the IAR1 register together with the MP1L/MP1H register pair and IAR2 register together with the MP2L/MP2H register pair can access data from any Data Memory Sector. As the Indirect Addressing Registers are not physically implemented, reading the Indirect Addressing Registers will return a result of "00H" and writing to the registers will result in no operation.

Memory Pointers – MP0, MP1L, MP1H, MP2L, MP2H

Five Memory Pointers, known as MP0, MP1L, MP1H, MP2L, MP2H, are provided. These Memory Pointers are physically implemented in the Data Memory and can be manipulated in the same way as normal registers providing a convenient way with which to address and track data. When any operation to the relevant Indirect Addressing Registers is carried out, the actual address that the microcontroller is directed to is the address specified by the related Memory Pointer. MP0, together with Indirect Addressing Register, IAR0, are used to access data from Sector 0, while MP1L/MP1H together with IAR1 and MP2L/MP2H together with IAR2 are used to access data from all sectors according to the corresponding MP1H or MP2H register. Direct Addressing can be used in all sectors using the extended instruction which can address all available Data Memory space.

The following example shows how to clear a section of four Data Memory locations already defined as locations adres1 to adres4.

Indirect Addressing Program Example 1

```
data .section ´data´
adres1   db ?
adres2   db ?
adres3   db ?
adres4   db ?
block    db ?
code .section at 0 ´code´
org 00h
start:
    mov a, 04h              ; setup size of block
    mov block, a
    mov a, offset adres1    ; Accumulator loaded with first RAM address
    mov mp0, a              ; setup memory pointer with first RAM address
loop:
    clr IAR0               ; clear the data at address defined by MP0
    inc mp0               ; increment memory pointer
    sdz block             ; check if last memory location has been cleared
    jmp loop
continue:
```

Indirect Addressing Program Example 2

```
data .section ´data´
adres1  db ?
adres2  db ?
adres3  db ?
adres4  db ?
block   db ?
code .section at 0 ´code´
org 00h
start:
    mov a, 04h              ; setup size of block
    mov block, a
    mov a, 01h              ; setup the memory sector
    mov mp1h, a
    mov a, offset adres1    ; Accumulator loaded with first RAM address
    mov mp1l, a             ; setup memory pointer with first RAM address
loop:
    clr IAR1               ; clear the data at address defined by MP1L
    inc mp1l              ; increment memory pointer MP1L
    sdz block            ; check if last memory location has been cleared
    jmp loop
continue:
```

The important point to note here is that in the example shown above, no reference is made to specific Data Memory addresses.

Direct Addressing Program Example using extended instructions

```
data .section ´data´
temp  db ?
code .section at 0 ´code´
org 00h
start:
    lmov a, [m]            ; move [m] data to acc
    lsub a, [m+1]          ; compare [m] and [m+1] data
    snz c                  ; [m]>[m+1]?
    jmp continue           ; no
    lmov a, [m]            ; yes, exchange [m] and [m+1] data
    mov temp, a
    lmov a, [m+1]
    lmov [m], a
    mov a, temp
    lmov [m+1], a
continue:
```

Note: here "m" is a data memory address located in any data memory sectors. For example, m=1F0H, it indicates address 0F0H in Sector 1.

Program Memory Bank Pointer – PBP

For this device the Program Memory is divided into several banks. Selecting the required Program Memory area is achieved using the Program Memory Bank Pointer, PBP. The PBP register should be properly configured before the device executes the "Branch" operation using the "JMP" or "CALL" instruction. After that a jump to a non-consecutive Program Memory address which is located in a certain bank selected by the program memory bank pointer bits will occur.

- **PBP Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	PBP1	PBP0
R/W	—	—	—	—	—	—	R/W	R/W
POR	—	—	—	—	—	—	0	0

Bit 7~2   Unimplemented, read as "0"

Bit 1~0   **PBP1~PBP0**: Select Program Memory Bank
    00: Bank 0
    01: Bank 1
    10: Bank 2
    11: Bank 3

Accumulator – ACC

The Accumulator is central to the operation of any microcontroller and is closely related with operations carried out by the ALU. The Accumulator is the place where all intermediate results from the ALU are stored. Without the Accumulator it would be necessary to write the result of each calculation or logical operation such as addition, subtraction, shift, etc., to the Data Memory resulting in higher programming and timing overheads. Data transfer operations usually involve the temporary storage function of the Accumulator; for example, when transferring data between one user-defined register and another, it is necessary to do this by passing the data through the Accumulator as no direct transfer between two registers is permitted.

Program Counter Low Register – PCL

To provide additional program control functions, the low byte of the Program Counter is made accessible to programmers by locating it within the Special Purpose area of the Data Memory. By manipulating this register, direct jumps to other program locations are easily implemented. Loading a value directly into this PCL register will cause a jump to the specified Program Memory location, however, as the register is only 8-bit wide, only jumps within the current Program Memory page are permitted. When such operations are used, note that a dummy cycle will be inserted.

Look-up Table Registers – TBLP, TBHP, TBLH

These three special function registers are used to control operation of the look-up table which is stored in the Program Memory. TBLP and TBHP are the table pointers and indicate the location where the table data is located. Their value must be setup before any table read commands are executed. Their value can be changed, for example using the "INC" or "DEC" instructions, allowing for easy table data pointing and reading. TBLH is the location where the high order byte of the table data is stored after a table read data instruction has been executed. Note that the lower order table data byte is transferred to a user defined location.

Status Register – STATUS

This 8-bit register contains the SC flag, CZ flag, zero flag (Z), carry flag (C), auxiliary carry flag (AC), overflow flag (OV), power down flag (PDF), and watchdog time-out flag (TO). These arithmetic/ logical operation and system management flags are used to record the status and operation of the microcontroller.

With the exception of the TO and PDF flags, bits in the status register can be altered by instructions like most other registers. Any data written into the status register will not change the TO or PDF flag. In addition, operations related to the status register may give different results due to the different instruction operations. The TO flag can be affected only by a system power-up, a WDT time-out or by executing the "CLR WDT" or "HALT" instruction. The PDF flag is affected only by executing the "HALT" or "CLR WDT" instruction or during a system power-up.

The Z, OV, AC, C, SC and CZ flags generally reflect the status of the latest operations.

- C is set if an operation results in a carry during an addition operation or if a borrow does not take place during a subtraction operation; otherwise C is cleared. C is also affected by a rotate through carry instruction.

- AC is set if an operation results in a carry out of the low nibbles in addition, or no borrow from the high nibble into the low nibble in subtraction; otherwise AC is cleared.

- Z is set if the result of an arithmetic or logical operation is zero; otherwise Z is cleared.

- OV is set if an operation results in a carry into the highest-order bit but not a carry out of the highest-order bit, or vice versa; otherwise OV is cleared.

- PDF is cleared by a system power-up or executing the "CLR WDT" instruction. PDF is set by executing the "HALT" instruction.

- TO is cleared by a system power-up or executing the "CLR WDT" or "HALT" instruction. TO is set by a WDT time-out.

- CZ is the operational result of different flags for different instructions. Refer to register definitions for more details.

- SC is the result of the "XOR" operation which is performed by the OV flag and the MSB of the current instruction operation result.

In addition, on entering an interrupt sequence or executing a subroutine call, the status register will not be pushed onto the stack automatically. If the contents of the status registers are important and if the subroutine can corrupt the status register, precautions must be taken to correctly save it.

- **STATUS Register**

Bit	7	6	5	4	3	2	1	0
Name	SC	CZ	TO	PDF	OV	Z	AC	C
R/W	R	R	R	R	R/W	R/W	R/W	R/W
POR	x	x	0	0	x	x	x	x

"x": unknown

Bit 7   **SC**: XOR Operation Result - performed by the OV flag and the MSB of the instruction operation result.

Bit 6   **CZ**: Operational Result of Different Flags for Different Instructions.

For SUB/SUBM/LSUB/LSUBM instructions, the CZ flag is equal to the Z flag.

For SBC/ SBCM/ LSBC/ LSBCM instructions, the CZ flag is the "AND" operation result which is performed by the previous operation CZ flag and current operation zero flag.

For other instructions, the CZ flag will not be affected.

Bit 5   **TO**: Watchdog Time-Out Flag
      0: After power up or executing the "CLR WDT" or "HALT" instruction
      1: A watchdog time-out occurred.

Bit 4   **PDF**: Power Down Flag
      0: After power up or executing the "CLR WDT" instruction
      1: By executing the "HALT" instruction

Bit 3   **OV**: Overflow Flag
      0: No overflow
      1: An operation results in a carry into the highest-order bit but not a carry out of the highest-order bit or vice versa.

Bit 2   **Z**: Zero Flag
      0: The result of an arithmetic or logical operation is not zero
      1: The result of an arithmetic or logical operation is zero

Bit 1   **AC**: Auxiliary flag
      0: No auxiliary carry
      1: An operation results in a carry out of the low nibbles in addition, or no borrow from the high nibble into the low nibble in subtraction

Bit 0   **C**: Carry Flag
      0: No carry-out
      1: An operation results in a carry during an addition operation or if a borrow does not take place during a subtraction operation

C is also affected by a rotate through carry instruction.

EEPROM Data Memory

This device contains an area of internal EEPROM Data Memory. EEPROM, which stands for Electrically Erasable Programmable Read Only Memory, is by its nature a non-volatile form of re-programmable memory, with data retention even when its power supply is removed. By incorporating this kind of data memory, a whole new host of application possibilities are made available to the designer. The availability of EEPROM storage allows information such as product identification numbers, calibration values, specific user data, system setup data or other product information to be stored directly within the product microcontroller. The process of reading and writing data to the EEPROM memory has been reduced to a very trivial affair.

EEPROM Data Memory Structure

The EEPROM Data Memory capacity is 64×8 bits for the device. Unlike the Program Memory and RAM Data Memory, the EEPROM Data Memory is not directly mapped into memory space and is therefore not directly addressable in the same way as the other types of memory. Read and Write operations to the EEPROM are carried out in single byte operations using an address and a data register in Sector 0 and a single control register in Sector 1.

EEPROM Registers

Three registers control the overall operation of the internal EEPROM Data Memory. These are the address register, EEA, the data register, EED and a single control register, EEC. As both the EEA and EED registers are located in Sector 0, they can be directly accessed in the same was as any other Special Function Register. The EEC register however, being located in Sector 1, can be read from or written to indirectly using the MP1L/MP1H or MP2L/MP2H Memory Pointer and Indirect Addressing Register, IAR1/IAR2. Because the EEC control register is located at address 40H in Sector 1, the MP1L or MP2L Memory Pointer must first be set to the value 40H and the MP1H or MP2H Memory Pointer high byte set to the value, 01H, before any operations on the EEC register are executed.

Register Name	Bit							
	7	6	5	4	3	2	1	0
EEA	—	—	EEA5	EEA4	EEA3	EEA2	EEA1	EEA0
EED	EED7	EED6	EED5	EED4	EED3	EED2	EED1	EED0
EEC	—	—	—	—	WREN	WR	RDEN	RD

EEPROM Register List

- **EEA Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	EEA5	EEA4	EEA3	EEA2	EEA1	EEA0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

Bit 7~6   Unimplemented, read as "0"

Bit 5~0   **EEA5~EEA0**: Data EEPROM Address
                   Data EEPROM address bit 5~bit 0

• **EED Register**

Bit	7	6	5	4	3	2	1	0
Name	EED7	EED6	EED5	EED4	EED3	EED2	EED1	EED0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   **EED7~EED0**: Data EEPROM Data

Data EEPROM data bit 7~bit 0

• **EEC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	WREN	WR	RDEN	RD
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	—	—	—	—	0	0	0	0

Bit 7~4   Unimplemented, read as "0"

Bit 3   **WREN**: Data EEPROM Write Enable

0: Disable

1: Enable

This is the Data EEPROM Write Enable Bit which must be set high before Data EEPROM write operations are carried out. Clearing this bit to zero will inhibit Data EEPROM write operations.

Bit 2   **WR**: EEPROM Write Control

0: Write cycle has finished

1: Activate a write cycle

This is the Data EEPROM Write Control Bit and when set high by the application program will activate a write cycle. This bit will be automatically reset to zero by the hardware after the write cycle has finished. Setting this bit high will have no effect if the WREN has not first been set high.

Bit 1   **RDEN**: Data EEPROM Read Enable

0: Disable

1: Enable

This is the Data EEPROM Read Enable Bit which must be set high before Data EEPROM read operations are carried out. Clearing this bit to zero will inhibit Data EEPROM read operations.

Bit 0   **RD**: EEPROM Read Control

0: Read cycle has finished

1: Activate a read cycle

This is the Data EEPROM Read Control Bit and when set high by the application program will activate a read cycle. This bit will be automatically reset to zero by the hardware after the read cycle has finished. Setting this bit high will have no effect if the RDEN has not first been set high.

Note: The WREN, WR, RDEN and RD cannot be set high at the same time in one instruction. The WR and RD cannot be set high at the same time.

Reading Data from the EEPROM

To read data from the EEPROM, the read enable bit, RDEN, in the EEC register must first be set high to enable the read function. The EEPROM address of the data to be read must then be placed in the EEA register. If the RD bit in the EEC register is now set high, a read cycle will be initiated. Setting the RD bit high will not initiate a read operation if the RDEN bit has not been set. When the read cycle terminates, the RD bit will be automatically cleared to zero, after which the data can be read from the EED register. The data will remain in the EED register until another read or write operation is executed. The application program can poll the RD bit to determine when the data is valid for reading.

Writing Data to the EEPROM

The EEPROM address of the data to be written must first be placed in the EEA register and the data placed in the EED register. To write data to the EEPROM, the write enable bit, WREN, in the EEC register must first be set high to enable the write function. After this, the WR bit in the EEC register must be immediately set high to initiate a write cycle. These two instructions must be executed consecutively. The global interrupt bit EMI should also first be cleared before implementing any write operations, and then set again after the write cycle has started. Note that setting the WR bit high will not initiate a write cycle if the WREN bit has not been set. As the EEPROM write cycle is controlled using an internal timer whose operation is asynchronous to microcontroller system clock, a certain time will elapse before the data will have been written into the EEPROM. Detecting when the write cycle has finished can be implemented either by polling the WR bit in the EEC register or by using the EEPROM interrupt. When the write cycle terminates, the WR bit will be automatically cleared to zero by the microcontroller, informing the user that the data has been written to the EEPROM. The application program can therefore poll the WR bit to determine when the write cycle has ended.

Write Protection

Protection against inadvertent write operation is provided in several ways. After the device is powered-on the Write Enable bit in the control register will be cleared preventing any write operations. Also at power-on the Memory Pointer high byte register, MP1H or MP2H, will be reset to zero, which means that Data Memory Sector 0 will be selected. As the EEPROM control register is located in Sector 1, this adds a further measure of protection against spurious write operations. During normal program operation, ensuring that the Write Enable bit in the control register is cleared will safeguard against incorrect write operations.

EEPROM Interrupt

The EEPROM write interrupt is generated when an EEPROM write cycle has ended. The EEPROM interrupt must first be enabled by setting the DEE bit in the relevant interrupt register. However as the EEPROM is contained within a Multi-function Interrupt, the associated multi-function interrupt enable bit must also be set. When an EEPROM write cycle ends, the DEF request flag and its associated multi-function interrupt request flag will both be set. If the global, EEPROM and Multi-function interrupts are enabled and the stack is not full, a jump to the associated Multi-function Interrupt vector will take place. When the interrupt is serviced only the Multi-function interrupt flag will be automatically reset, the EEPROM interrupt flag must be manually reset by the application program. More details can be obtained in the Interrupt section.

Programming Considerations

Care must be taken that data is not inadvertently written to the EEPROM. Protection can be enhanced by ensuring that the Write Enable bit is normally cleared to zero when not writing. Also the Memory Pointer high byte register, MP1H or MP2H, could be normally cleared to zero as this would inhibit access to Sector 1 where the EEPROM control register exist. Although certainly not necessary, consideration might be given in the application program to the checking of the validity of new write data by a simple read back process.

When writing data the WR bit must be set high immediately after the WREN bit has been set high, to ensure the write cycle executes correctly. The global interrupt bit EMI should also be cleared before a write cycle is executed and then re-enabled after the write cycle starts. Note that the device should not enter the IDLE or SLEEP mode until the EEPROM read or write operation is totally complete. Otherwise, the EEPROM read or write operation will fail.

Programming Examples

- **Reading data from the EEPROM – polling method**

```
MOV  A, EEPROM_ADRES       ; user defined address
MOV  EEA, A
MOV  A, 40H                ; setup memory pointer MP1L
MOV  MP1L, A
MOV  A, 01H                ; setup memory pointer MP1H
MOV  MP1H, A               ; MP1H&MP1L point to EEC register
SET  IAR1.1               ; set RDEN bit, enable read operations
SET  IAR1.0               ; start Read Cycle - set RD bit
BACK:
SZ   IAR1.0               ; check for read cycle end
JMP  BACK
CLR  IAR1                 ; disable EEPROM read/write
CLR  MP1H
MOV  A, EED                ; move read data to register
MOV  READ_DATA, A
```

- **Writing Data to the EEPROM – polling method**

```
MOV  A, EEPROM_ADRES       ; user defined address
MOV  EEA, A
MOV  A, EEPROM_DATA        ; user defined data
MOV  EED, A
MOV  A, 040H               ; setup memory pointer MP1L
MOV  MP1L, A
MOV  A, 01H                ; setup memory pointer MP1H
MOV  MP1H, A               ; MP1H&MP1L point to EEC register
CLR  EMI
SET  IAR1.3               ; set WREN bit, enable write operations
SET  IAR1.2               ; start Write Cycle - set WR bit – executed immediately
                          ; after set WREN bit high
SET  EMI
BACK:
SZ   IAR1.2               ; check for write cycle end
JMP  BACK
CLR  IAR1                 ; disable EEPROM read/write
CLR  MP1H
```

Oscillators

Various oscillator options offer the user a wide range of functions according to their various application requirements. The flexible features of the oscillator functions ensure that the best optimisation can be achieved in terms of speed and power saving. Oscillator selections and operation are selected through the application program and relevant control registers.

Oscillator Overview

In addition to being the source of the main system clock the oscillators also provide clock sources for the Watchdog Timer and Time Base Interrupts. External oscillators requiring some external components as well as fully integrated internal oscillators, requiring no external components, are provided to form a wide range of both fast and slow system oscillators. All oscillator options are selected through the relevant control registers. The higher frequency oscillators provide higher performance but carry with it the disadvantage of higher power requirements, while the opposite is of course true for the lower frequency oscillators. With the capability of dynamically switching between fast and slow system clock, the device has the flexibility to optimize the performance/power ratio, a feature especially important in power sensitive portable applications.

Type	Name	Frequency	Pins
External High Speed Crystal	HXT	400kHz~16MHz	OSC1/OSC2
Internal High Speed RC	HIRC	4/8/12MHz	—
External Low Speed Crystal	LXT	32.768kHz	XT1/XT2
Internal Low Speed RC	LIRC	32kHz	—

Oscillator Types

System Clock Configurations

There are several methods of generating the system clock, two high speed oscillators and two low speed oscillators. The high speed oscillators are sourced from the external crystal/ceramic oscillator and the internal 4/8/12MHz RC oscillator. The low speed oscillators are the external 32.768kHz crystal oscillator and the internal 32kHz RC oscillator, LIRC. Selecting whether the low or high speed oscillator is used as the system oscillator is implemented using the CKS2~CKS0 bits in the SCC register and as the system clock can be dynamically selected.

The actual source clock used for the low speed oscillator is chosen via the FSS bit in the SCC register while for the high speed oscillator the source clock is selected via the FHS bit in the SCC register. The frequency of the slow speed or high speed system clock is also determined using the CKS2~CKS0 bits in the SCC register. Note that two oscillator selections must be made namely one high speed and one low speed system oscillators. It is not possible to choose a no-oscillator selection for either the high or low speed oscillator.

System Clock Configurations
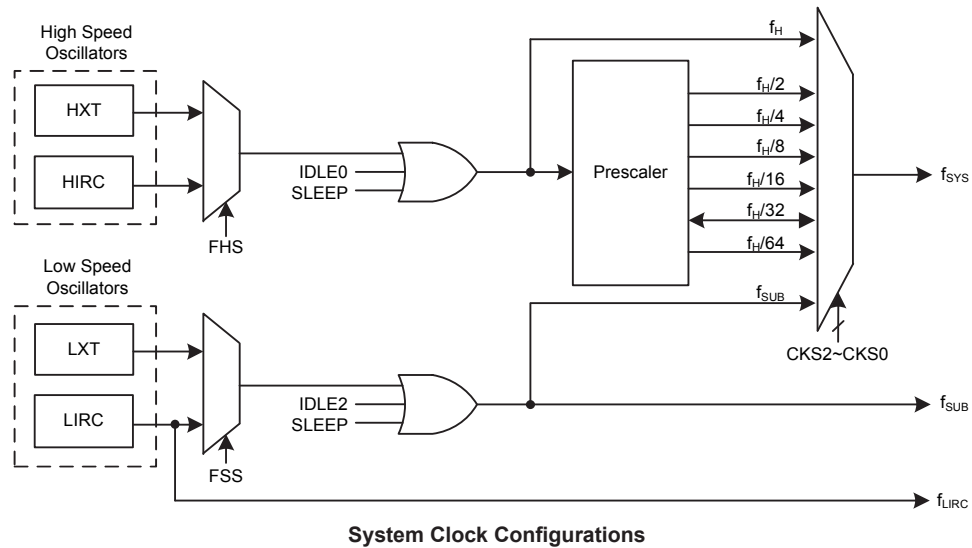
External Crystal/Ceramic Oscillator – HXT

The External Crystal/Ceramic System Oscillator is one of the high frequency oscillators. For most crystal oscillator configurations, the simple connection of a crystal across OSC1 and OSC2 will create the necessary phase shift and feedback for oscillation, without requiring external capacitors. However, for some crystal types and frequencies, to ensure oscillation, it may be necessary to add two small value capacitors, C1 and C2. Using a ceramic resonator will usually require two small value capacitors, C1 and C2, to be connected as shown for oscillation to occur. The values of C1 and C2 should be selected in consultation with the crystal or resonator manufacturer's specification.

For oscillator stability and to minimise the effects of noise and crosstalk, it is important to ensure that the crystal and any associated resistors and capacitors along with interconnecting lines are all located as close to the MCU as possible.
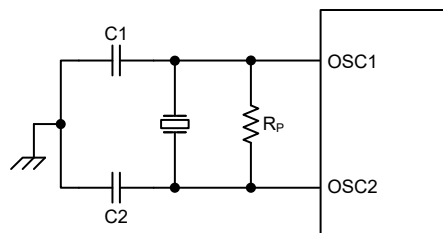
Note: 1. R$_P$ is normally not required. C1 and C2 are required.
2. Although not shown OSC1/OSC2 pins have a parasitic capacitance of around 7pF.

Crystal/Resonator Oscillator – HXT

Crystal Oscillator C1 and C2 Values		
Crystal Frequency	C1	C2
16MHz	0pF	0pF
12MHz	0pF	0pF
8MHz	0pF	0pF
6MHz	0pF	0pF
4MHz	0pF	0pF
1MHz	100pF	100pF
Note: C1 and C2 values are for guidance only.		

Crystal Recommended Capacitor Values

Internal High Speed RC Oscillator – HIRC

The internal RC oscillator is a fully integrated system oscillator requiring no external components. The internal RC oscillator has three fixed frequencies of 4MHz, 8MHz and 12MHz. Device trimming during the manufacturing process and the inclusion of internal frequency compensation circuits are used to ensure that the influence of the power supply voltage, temperature and process variations on the oscillation frequency are minimised. Note that if this internal system clock option is selected, as it requires no external pins for its operation, I/O pins are free for use as normal I/O pins.

External 32.768kHz Crystal Oscillator – LXT

The External 32.768 kHz Crystal System Oscillator is one of the low frequency oscillator choices, which is selected via a software control bit, FSS. This clock source has a fixed frequency of 32.768kHz and requires a 32.768kHz crystal to be connected between pins XT1 and XT2. The external resistor and capacitor components connected to the 32.768kHz crystal are necessary to provide oscillation. For applications where precise frequencies are essential, these components may be required to provide frequency compensation due to different crystal manufacturing tolerances. After the LXT oscillator is enabled by setting the LXTEN bit to 1, there is a time delay associated with the LXT oscillator waiting for it to start-up.

However, for some crystals, to ensure oscillation and accurate frequency generation, it is necessary to add two small value external capacitors, C1 and C2. The exact values of C1 and C2 should be selected in consultation with the crystal or resonator manufacturer's specification. The external parallel feedback resistor, R_P, and the pull high resistor, R_U, are required.

The pin-shared software control bits determine if the XT1/XT2 pins are used for the LXT oscillator or as I/O or other pin-shared functional pins.

- If the LXT oscillator is not used for any clock source, the XT1/XT2 pins can be used as normal I/O or other pin-shared function pins.

- If the LXT oscillator is used for any clock source, the 32.768 kHz crystal should be connected to the XT1/XT2 pins.

For oscillator stability and to minimise the effects of noise and crosstalk, it is important to ensure that the crystal and any associated resistors and capacitors along with interconnecting lines are all located as close to the MCU as possible.
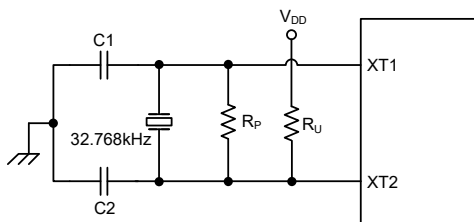
Note: 1. R_P, R_U, C1 and C2 are required.
    2. Although not shown XT1/XT2 pins have a parasitic capacitance of around 7pF.

External LXT Oscillator

LXT Oscillator C1 and C2 Values		
Crystal Frequency	C1	C2
32.768kHz	10pF	22~24pF
Note: 1. C1 and C2 values are for guidance only.		
2. R_P=5M~10MΩ is recommended.		
3. R_U=5.1MΩ is recommended.		

32.768kHz Crystal Recommended Capacitor Values

Internal 32kHz Oscillator – LIRC

The Internal 32kHz System Oscillator is one of the low frequency oscillator choices, which is selected via a software control bit, FSS. It is a fully integrated RC oscillator with a typical frequency of 32kHz at 5V, requiring no external components for its implementation. Device trimming during the manufacturing process and the inclusion of internal frequency compensation circuits are used to ensure that the influence of the power supply voltage, temperature and process variations on the oscillation frequency are minimised.

Operating Modes and System Clocks

Present day applications require that their microcontrollers have high performance but often still demand that they consume as little power as possible, conflicting requirements that are especially true in battery powered portable applications. The fast clocks required for high performance will by their nature increase current consumption and of course vice versa, lower speed clocks reduce current consumption. As Holtek has provided the device with both high and low speed clock sources and the means to switch between them dynamically, the user can optimise the operation of their microcontroller to achieve the best performance/power ratio.

System Clocks

The device has many different clock sources for both the CPU and peripheral function operation. By providing the user with a wide range of clock options using register programming, a clock system can be configured to obtain maximum application performance.

The main system clock can come from a high frequency f_H or low frequency f_{SUB} source, and is selected using the CKS2~CKS0 bits in the SCC register. The high speed system clock can be sourced from either the HXT or HIRC oscillator, selected via configuring the FHS bit in the SCC register. The low speed system clock source can be sourced from the internal clock f_{SUB}. If f_{SUB} is selected then it can be sourced by either the LXT or LIRC oscillator, selected via configuring the FSS bit in the SCC register. The other choice, which is a divided version of the high speed system oscillator has a range of $f_H/2 \sim f_H/64$.
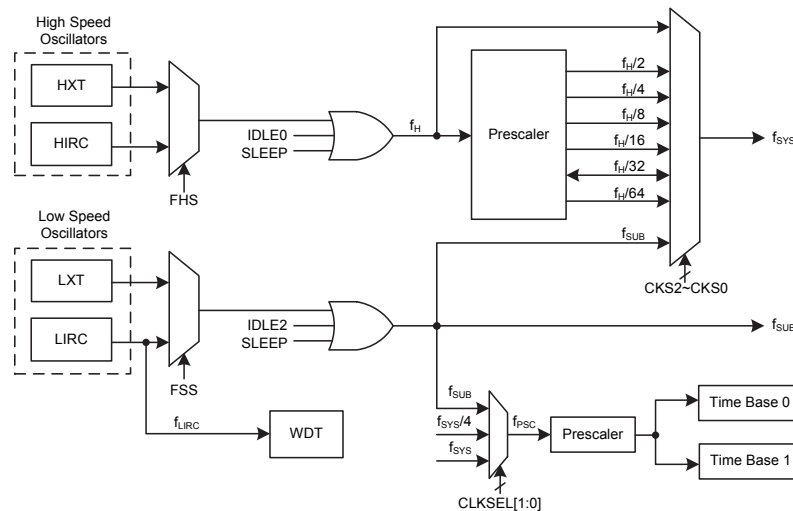
Device Clock Configurations

Note: When the system clock source f_{SYS} is switched to f_{SUB} from f_H, the high speed oscillator can be stopped to conserve the power or continue to oscillate to provide the clock source, $f_H \sim f_H/64$, for peripheral circuits to use, which is determined by configuring the corresponding high speed oscillator enable control bit.

System Operation Modes

There are six different modes of operation for the microcontroller, each one with its own special characteristics and which can be chosen according to the specific performance and power requirements of the application. There are two modes allowing normal operation of the microcontroller, the FAST Mode and SLOW Mode. The remaining four modes, the SLEEP, IDLE0, IDLE1 and IDLE2 Mode are used when the microcontroller CPU is switched off to conserve power.

Operation Mode	CPU	Register Setting			f_{SYS}	f_H	f_{SUB}	f_{LIRC}
		FHIDEN	FSIDEN	CKS2~CKS0				
FAST	On	x	x	000~110	fH~fH/64	On	On	On
SLOW	On	x	x	111	f_{SUB}	On/Off [1]	On	On
IDLE0	Off	0	1	000~110	Off	Off	On	On
				111	On			
IDLE1	Off	1	1	xxx	On	On	On	On
IDLE2	Off	1	0	000~110	On	On	Off	On
				111	Off			
SLEEP	Off	0	0	xxx	Off	Off	Off	On/Off [2]

"x": Don't care

Note: 1. The f_H clock will be switched on or off by configuring the corresponding oscillator enable bit in the SLOW mode.

2. The f_{LIRC} clock can be on or off which is controlled by the WDT function being enabled or disabled in the SLEEP mode.

FAST Mode

As the name suggests this is one of the main operating modes where the microcontroller has all of its functions operational and where the system clock is provided by one of the high speed oscillators. This mode operates allowing the microcontroller to operate normally with a clock source will come from one of the high speed oscillators, either the HXT or HIRC oscillators. The high speed oscillator will however first be divided by a ratio ranging from 1 to 64, the actual ratio being selected by the CKS2~CKS0 bits in the SCC register. Although a high speed oscillator is used, running the microcontroller at a divided clock ratio reduces the operating current.

SLOW Mode

This is also a mode where the microcontroller operates normally although now with a slower speed clock source. The clock source used will be from f_{SUB}. The f_{SUB} clock is derived from either the LIRC or LXT oscillator determined by the FSS bit in the SCC register.

SLEEP Mode

The SLEEP Mode is entered when a HALT instruction is executed and when the FHIDEN and FSIDEN bit are low. In the SLEEP mode the CPU will be stopped. The f_{SUB} clock provided to the peripheral function will also be stopped, too. However the f_{LIRC} clock can continue to operate if the WDT function is enabled.

IDLE0 Mode

The IDLE0 Mode is entered when a HALT instruction is executed and when the FHIDEN bit in the SCC register is low and the FSIDEN bit in the SCC register is high. In the IDLE0 Mode the CPU will be switched off but the low speed oscillator will be on to drive some peripheral functions.

IDLE1 Mode

The IDLE1 Mode is entered when a HALT instruction is executed and when the FHIDEN bit in the SCC register is high and the FSIDEN bit in the SCC register is high. In the IDLE1 Mode the CPU will be switched off but both the high and low speed oscillators will be on to provide a clock source to keep some peripheral functions operational.

IDLE2 Mode

The IDLE2 Mode is entered when a HALT instruction is executed and when the FHIDEN bit in the SCC register is high and the FSIDEN bit in the SCC register is low. In the IDLE2 Mode the CPU will be switched off but the high speed oscillator will be on to provide a clock source to keep some peripheral functions operational.

Control Registers

The registers, SCC, HIRCC, HXTC and LXTC, are used to control the system clock and the corresponding oscillator configurations.

Register Name	Bit							
	7	6	5	4	3	2	1	0
SCC	CKS2	CKS1	CKS0	—	FHS	FSS	FHIDEN	FSIDEN
HIRCC	—	—	—	—	HIRC1	HIRC0	HIRCF	HIRCEN
HXTC	—	—	—	—	—	HXTM	HXTF	HXTEN
LXTC	—	—	—	—	—	—	LXTF	LXTEN

System Operating Mode Control Register List

- **SCC Register**

Bit	7	6	5	4	3	2	1	0
Name	CKS2	CKS1	CKS0	—	FHS	FSS	FHIDEN	FSIDEN
R/W	R/W	R/W	R/W	—	R/W	R/W	R/W	R/W
POR	0	0	0	—	0	0	0	0

Bit 7~5   **CKS2~CKS0**: System clock selection
000: f_H
001: $f_H/2$
010: $f_H/4$
011: $f_H/8$
100: $f_H/16$
101: $f_H/32$
110: $f_H/64$
111: f_{SUB}

These three bits are used to select which clock is used as the system clock source. In addition to the system clock source directly derived from f_H or f_{SUB}, a divided version of the high speed system oscillator can also be chosen as the system clock source.

Bit 4   Unimplemented, read as "0"

Bit 3   **FHS**: High frequency clock selection
0: HIRC
1: HXT

Bit 2   **FSS**: Low frequency clock selection
0: LIRC
1: LXT

Bit 1   **FHIDEN**: High frequency oscillator control when CPU is switched off
0: Disable
1: Enable

Bit 0   This bit is used to control whether the high speed oscillator is activated or stopped when the CPU is switched off by executing an "HALT" instruction.

Bit 0   **FSIDEN**: Low frequency oscillator control when CPU is switched off
         0: Disable
         1: Enable

This bit is used to control whether the low speed oscillator is activated or stopped when the CPU is switched off by executing an "HALT" instruction. The LIRC oscillator is controlled by this bit together with the WDT function module. If this bit is cleared to 0 but the WDT function is enabled, the f_{LIRC} clock will also be enabled.

- **HIRCC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	HIRC1	HIRC0	HIRCF	HIRCEN
R/W	—	—	—	—	R/W	R/W	R	R/W
POR	—	—	—	—	0	0	0	1

Bit 7~4   Unimplemented, read as "0"

Bit 3~2   **HIRC1~HIRC0**: HIRC frequency selection
         00: 4MHz
         01: 8MHz
         10: 12MHz
         11: 4MHz

Bit 1   **HIRCF**: HIRC oscillator stable flag
         0: Unstable
         1: Stable

This bit is used to indicate whether the HIRC oscillator is stable or not. When the HIRCEN bit is set to 1 to enable the HIRC oscillator, the HIRCF bit will first be cleared to 0 and then set to 1 after the HIRC oscillator is stable.

Bit 0   **HIRCEN**: HIRC oscillator enable control
         0: Disable
         1: Enable

- **HXTC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	HXTM	HXTF	HXTEN
R/W	—	—	—	—	—	R/W	R	R/W
POR	—	—	—	—	—	0	0	0

Bit 7~3   Unimplemented, read as "0"

Bit 2   **HXTM**: HXT mode selection
         0: HXT frequency ≤ 10MHz
         1: HXT frequency > 10MHz

This bit is used to select the HXT oscillator operating mode. Note that this bit must be properly configured before the HXT is enabled. When the HXTEN bit is set to 1 to enable the HXT oscillator, it is invalid to change the value of this bit.

Bit 1   **HXTF**: HXT oscillator stable flag
         0: Unstable
         1: Stable

This bit is used to indicate whether the HXT oscillator is stable or not. When the HXTEN bit is set to 1 to enable the HXT oscillator, the HXTF bit will first be cleared to 0 and then set to 1 after the HXT oscillator is stable.

Bit 0   **HXTEN**: HXT oscillator enable control
         0: Disable
         1: Enable

• **LXTC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	LXTF	LXTEN
R/W	—	—	—	—	—	—	R	R/W
POR	—	—	—	—	—	—	0	0

Bit 7~2   Unimplemented, read as "0"

Bit 1   **LXTF**: LXT oscillator stable flag
    0: Unstable
    1: Stable

This bit is used to indicate whether the LXT oscillator is stable or not. When the LXTEN bit is set to 1 to enable the LXT oscillator, the LXTF bit will first be cleared to 0 and then set to 1 after the LXT oscillator is stable.

Bit 0   **LXTEN**: LXT oscillator enable control
    0: Disable
    1: Enable

Operating Mode Switching

The device can switch between operating modes dynamically allowing the user to select the best performance/power ratio for the present task in hand. In this way microcontroller operations that do not require high performance can be executed using slower clocks thus requiring less operating current and prolonging battery life in portable applications.

In simple terms, Mode Switching between the FAST Mode and SLOW Mode is executed using the CKS2~CKS0 bits in the SCC register while Mode Switching from the FAST/SLOW Mode to the SLEEP/IDLE Mode is executed via the HALT instruction. When a HALT instruction is executed, whether the device enters the IDLE Mode or the SLEEP Mode is determined by the condition of the FHIDEN and FSIDEN bits in the SCC register.

FAST
$f_{SYS}=f_H\sim f_H/64$
f_H on
CPU run
f_{SYS} on
f_{SUB} on

SLOW
$f_{SYS}=f_{SUB}$
f_{SUB} on
CPU run
f_{SYS} on
f_H on/off

SLEEP
HALT instruction executed
CPU stop
FHIDEN=0
FSIDEN=0
f_H off
f_{SUB} off

IDLE0
HALT instruction executed
CPU stop
FHIDEN=0
FSIDEN=1
f_H off
f_{SUB} on

IDLE2
HALT instruction executed
CPU stop
FHIDEN=1
FSIDEN=0
f_H on
f_{SUB} off

IDLE1
HALT instruction executed
CPU stop
FHIDEN=1
FSIDEN=1
f_H on
f_{SUB} on
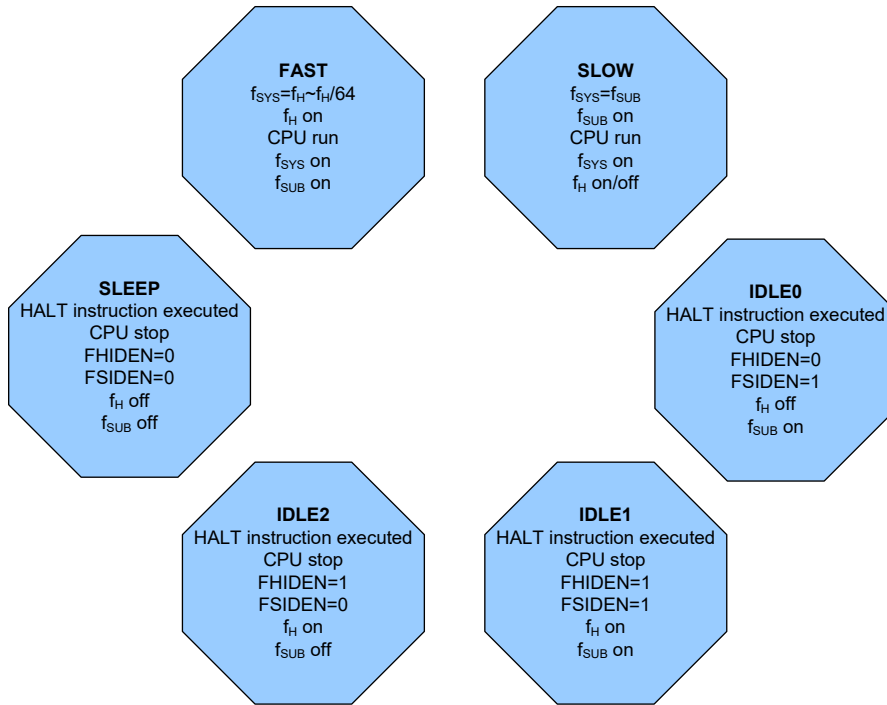
FAST Mode to SLOW Mode Switching

When running in the FAST Mode, which uses the high speed system oscillator, and therefore consumes more power, the system clock can switch to run in the SLOW Mode by set the CKS2~CKS0 bits to "111" in the SCC register. This will then use the low speed system oscillator which will consume less power. Users may decide to do this for certain operations which do not require high performance and can subsequently reduce power consumption.

The SLOW Mode is sourced from the LXT or LIRC oscillator determined by the FSS bit in the SCC register and therefore requires this oscillator to be stable before full mode switching occurs.
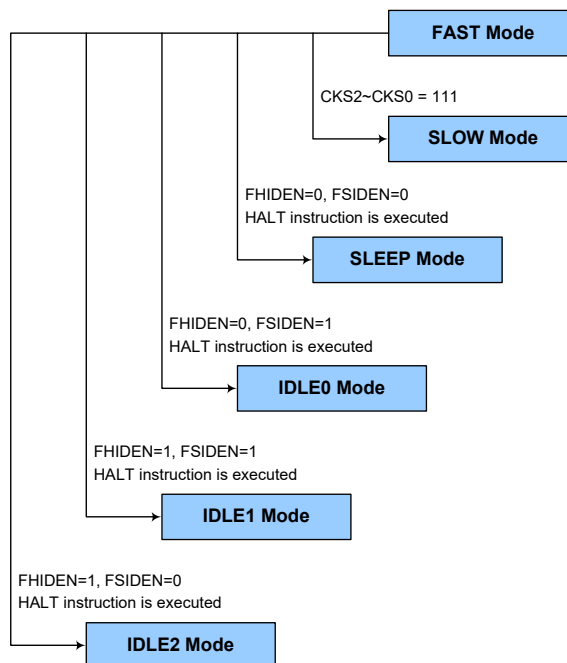
SLOW Mode to FAST Mode Switching

In SLOW mode the system clock is derived from f_{SUB}. When system clock is switched back to the FAST mode from f_{SUB}, the CKS2~CKS0 bits should be set to "000"~"110" and then the system clock will respectively be switched to f_H~$f_H/64$.

However, if f_H is not used in SLOW mode and thus switched off, it will take some time to re-oscillate and stabilise when switching to the FAST mode from the SLOW Mode. This is monitored using the HXTF bit in the HXTC register or the HIRCF bit in the HIRCC register. The time duration required for the high speed system oscillator stabilization is specified in the System Start Up Time Characteristics.
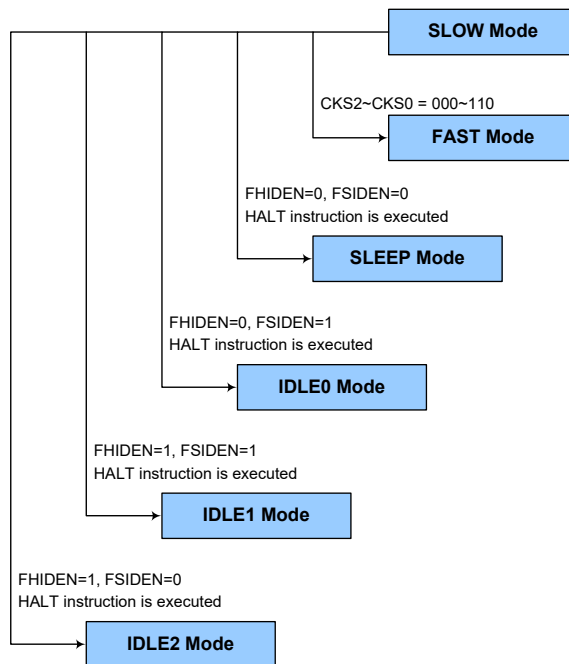
Entering the SLEEP Mode

There is only one way for the device to enter the SLEEP Mode and that is to execute the "HALT" instruction in the application program with both the FHIDEN and FSIDEN bits in the SCC register equal to "0". When this instruction is executed under the conditions described above, the following will occur:

- The system clock will be stopped and the application program will stop at the "HALT" instruction.
- The Data Memory contents and registers will maintain their present condition.
- The I/O ports will maintain their present conditions.
- In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.
- The WDT will be cleared and resume counting if the WDT function is enabled. If the WDT function is disabled, the WDT will be cleared and then stopped.

Entering the IDLE0 Mode

There is only one way for the device to enter the IDLE0 Mode and that is to execute the "HALT" instruction in the application program with the FHIDEN bit in the SCC register equal to "0" and the FSIDEN bit in the SCC register equal to "1". When this instruction is executed under the conditions described above, the following will occur:

- The f_H clock will be stopped and the application program will stop at the "HALT" instruction, but the f_{SUB} clock will be on.
- The Data Memory contents and registers will maintain their present condition.
- The I/O ports will maintain their present conditions.
- In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.
- The WDT will be cleared and resume counting if the WDT function is enabled. If the WDT function is disabled, the WDT will be cleared and then stopped.

Entering the IDLE1 Mode

There is only one way for the device to enter the IDLE1 Mode and that is to execute the "HALT" instruction in the application program with both the FHIDEN and FSIDEN bits in the SCC register equal to "1". When this instruction is executed under the conditions described above, the following will occur:

- The f_H and f_{SUB} clocks will be on but the application program will stop at the "HALT" instruction.

- The Data Memory contents and registers will maintain their present condition.

- The I/O ports will maintain their present conditions.

- In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.

- The WDT will be cleared and resume counting if the WDT function is enabled. If the WDT function is disabled, the WDT will be cleared and then stopped.

Entering the IDLE2 Mode

There is only one way for the device to enter the IDLE2 Mode and that is to execute the "HALT" instruction in the application program with the FHIDEN bit in the SCC register equal to "1" and the FSIDEN bit in the SCC register equal to "0". When this instruction is executed under the conditions described above, the following will occur:

- The f_H clock will be on but the f_{SUB} clock will be off and the application program will stop at the "HALT" instruction.

- The Data Memory contents and registers will maintain their present condition.

- The I/O ports will maintain their present conditions.

- In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.

- The WDT will be cleared and resume counting if the WDT function is enabled. If the WDT function is disabled, the WDT will be cleared and then stopped.

Standby Current Considerations

As the main reason for entering the SLEEP or IDLE Mode is to keep the current consumption of the device to as low a value as possible, perhaps only in the order of several micro-amps except in the IDLE1 and IDLE2 Mode, there are other considerations which must also be taken into account by the circuit designer if the power consumption is to be minimised. Special attention must be made to the I/O pins on the device. All high-impedance input pins must be connected to either a fixed high or low level as any floating input pins could create internal oscillations and result in increased current consumption. This also applies to the device which has different package types, as there may be unbonded pins. These must either be setup as outputs or if setup as inputs must have pull-high resistors connected.

Care must also be taken with the loads, which are connected to I/O pins, which are setup as outputs. These should be placed in a condition in which minimum current is drawn or connected only to external circuits that do not draw current, such as other CMOS inputs. Also note that additional standby current will also be required if the LXT or LIRC oscillator has enabled.

In the IDLE1 and IDLE2 Mode the high speed oscillator is on and if the system clock is from the high speed system oscillator, the additional standby current will also be perhaps in the order of several hundred micro-amps.

Wake-up

To minimise power consumption the device can enter the SLEEP or IDLE0~IDLE2 Mode, where the CPU will be switched off. However, when the device is woken up again, it will take a considerable time for the original system oscillator to restart, stabilise and allow normal operation to resume.

After the system enters the SLEEP or IDLE0~2 Mode, it can be woken up from one of various sources listed as follows:

- An external falling edge on Port A
- A system interrupt
- A WDT overflow

When the device executes the "HALT" instruction, it will enter the Power down mode and the PDF flag will be set high. The PDF flag will be cleared to 0 if the device experiences a system power-up or executes the clear Watchdog Timer instruction. If the system is woken up by a WDT overflow, a Watchdog Time-out hardware reset will be initiated and the TO flag will be set to 1. The TO flag is set if a WDT time-out occurs and causes a wake-up that only resets the Program Counter and Stack Pointer, other flags remain in their original status.

Each pin on Port A can be setup using the PAWU register to permit a negative transition on the pin to wake-up the system. When a pin wake-up occurs, the program will resume execution at the instruction following the "HALT" instruction. If the system is woken up by an interrupt, then two possible situations may occur. The first is where the related interrupt is disabled or the interrupt is enabled but the stack is full, in which case the program will resume execution at the instruction following the "HALT" instruction. In this situation, the interrupt which woke-up the device will not be immediately serviced, but will rather be serviced later when the related interrupt is finally enabled or when a stack level becomes free. The other situation is where the related interrupt is enabled and the stack is not full, in which case the regular interrupt response takes place. If an interrupt request flag is set high before entering the SLEEP or IDLE Mode, the wake-up function of the related interrupt will be disabled.

Watchdog Timer

The Watchdog Timer is provided to prevent program malfunctions or sequences from jumping to unknown locations, due to certain uncontrollable external events such as electrical noise.

Watchdog Timer Clock Source

The Watchdog Timer clock source is provided by the internal clock, f_{LIRC} which is sourced from the LIRC oscillator. The LIRC internal oscillator has an approximate frequency of 32kHz and this specified internal clock period can vary with V_{DD}, temperature and process variations. The Watchdog Timer source clock is then subdivided by a ratio of 2^8 to 2^{18} to give longer timeouts, the actual value being chosen using the WS2~WS0 bits in the WDTC register.

Watchdog Timer Control Register

A single register, WDTC, controls the required time-out period as well as the enable/disable and reset MCU operation.

- **WDTC Register**

Bit	7	6	5	4	3	2	1	0
Name	WE4	WE3	WE2	WE1	WE0	WS2	WS1	WS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	1	0	1	0	0	1	1

Bit 7~3   **WE4~WE0**: WDT function control
　　　　　10101: Disable
　　　　　01010: Enable
　　　　　Other values: Reset MCU
　　　　　When these bits are changed to any other values due to environmental noise the microcontroller will be reset; this reset operation will be activated after a delay time, t_{SRESET} and the WRF bit in the RSTFC register will be set high.

Bit 2~0   **WS2~WS0**: WDT time-out period selection
　　　　　000: $2^8/f_{LIRC}$
　　　　　001: $2^{10}/f_{LIRC}$
　　　　　010: $2^{12}/f_{LIRC}$
　　　　　011: $2^{14}/f_{LIRC}$
　　　　　100: $2^{15}/f_{LIRC}$
　　　　　101: $2^{16}/f_{LIRC}$
　　　　　110: $2^{17}/f_{LIRC}$
　　　　　111: $2^{18}/f_{LIRC}$
　　　　　These three bits determine the division ratio of the Watchdog Timer source clock, which in turn determines the time-out period.

- **RSTFC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	RSTF	LVRF	LRF	WRF
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	—	—	—	—	0	x	0	0

"x": unknown

Bit 7~4   Unimplemented, read as "0"

Bit 3   **RSTF**: Reset control register software reset flag
　　　　Described elsewhere

Bit 2   **LVRF**: LVR function reset flag
　　　　Described elsewhere

Bit 1   **LRF**: LVRC register software reset flag

           Described elsewhere

Bit 0   **WRF**: WDTC register software reset flag

             0: Not occurred

             1: Occurred

           This bit is set high by the WDTC register software reset and cleared by the application program. Note that this bit can only be cleared to 0 by the application program.

Watchdog Timer Operation

The Watchdog Timer operates by providing a device reset when its timer overflows. This means that in the application program and during normal operation the user has to strategically clear the Watchdog Timer before it overflows to prevent the Watchdog Timer from executing a reset. This is done using the clear watchdog instructions. If the program malfunctions for whatever reason, jumps to an unknown location, or enters an endless loop, these clear instructions will not be executed in the correct manner, in which case the Watchdog Timer will overflow and reset the device. There are five bits, WE4~WE0, in the WDTC register to offer the enable/disable control and reset control of the Watchdog Timer. The WDT function will be disabled when the WE4~WE0 bits are set to a value of 10101B while the WDT function will be enabled if the WE4~WE0 bits are equal to 01010B. If the WE4~WE0 bits are set to any other values, other than 01010B and 10101B, it will reset the device after a delay time, t_{SRESET}. After power on these bits will have a value of 01010B.

WE4~WE0 Bits	WDT Function
10101B	Disable
01010B	Enable
Any other value	Reset MCU

Watchdog Timer Enable/Disable Control

Under normal program operation, a Watchdog Timer time-out will initialise a device reset and set the status bit TO. However, if the system is in the SLEEP or IDLE Mode, when a Watchdog Timer time-out occurs, the TO bit in the STATUS register will be set and only the Program Counter and Stack Pointer will be reset. Three methods can be adopted to clear the contents of the Watchdog Timer. The first is a WDTC register software reset, which means a certain value except 01010B and 10101B written into the WE4~WE0 bits, the second is using the Watchdog Timer software clear instruction and the third is via a HALT instruction.

There is only one method of using software instruction to clear the Watchdog Timer. That is to use the single "CLR WDT" instruction to clear the WDT.

The maximum time-out period is when the 2^{18} division ratio is selected. As an example, with a 32kHz LIRC oscillator as its source clock, this will give a maximum watchdog period of around 8 second for the 2^{18} division ratio, and a minimum timeout of 7.8ms for the 2^8 division ration.

Watchdog Timer
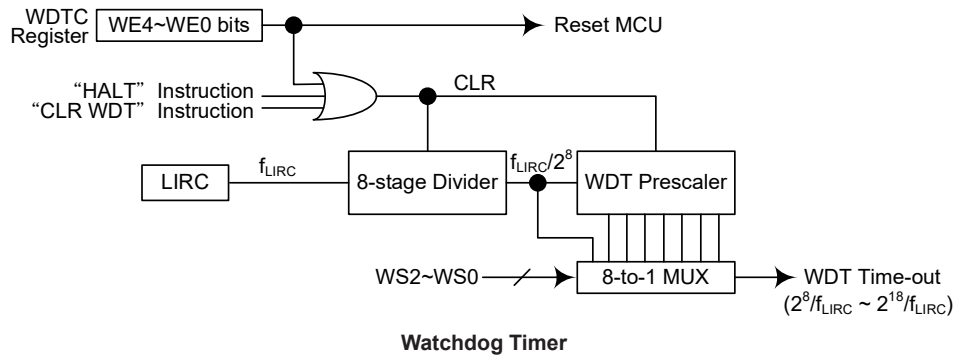
Reset and Initialisation

A reset function is a fundamental part of any microcontroller ensuring that the device can be set to some predetermined condition irrespective of outside parameters. The most important reset condition is after power is first applied to the microcontroller. In this case, internal circuitry will ensure that the microcontroller, after a short delay, will be in a well-defined state and ready to execute the first program instruction. After this power-on reset, certain important internal registers will be set to defined states before the program commences. One of these registers is the Program Counter, which will be reset to zero forcing the microcontroller to begin program execution from the lowest Program Memory address.

In addition to the power-on reset, another reset exists in the form of a Low Voltage Reset, LVR, where a full reset is implemented in situations where the power supply voltage falls below a certain threshold. Another type of reset is when the Watchdog Timer overflows and resets the microcontroller. All types of reset operations result in different register conditions being setup.

Reset Functions

There are several ways in which a microcontroller reset can occur, through events occurring internally:

Power-on Reset

The most fundamental and unavoidable reset is the one that occurs after power is first applied to the microcontroller. As well as ensuring that the Program Memory begins execution from the first memory address, a power-on reset also ensures that certain other registers are preset to known conditions. All the I/O port and port control registers will power up in a high condition ensuring that all I/O ports will be first set to inputs.
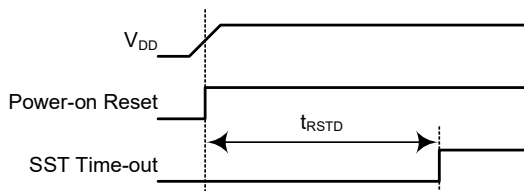
Power-on Reset Timing Chart

Internal Reset Control

There is an internal reset control register, RSTC, which is used to provide a reset when the device operates abnormally due to the environmental noise interference. If the content of the RSTC register is set to any value other than 01010101B or 10101010B, it will reset the device after a delay time, t_{SRESET}. After power on the register will have a value of 01010101B.

RSTC7~RSTC0 Bits	Reset Function
01010101B	No operation
10101010B	No operation
Any other value	Reset MCU

Internal Reset Function Control

- **RSTC Register**

Bit	7	6	5	4	3	2	1	0
Name	RSTC7	RSTC6	RSTC5	RSTC4	RSTC3	RSTC2	RSTC1	RSTC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	1	0	1	0	1	0	1

Bit 7~0   **RSTC7~RSTC0**: Reset function control
         01010101: No operation
         10101010: No operation
         Other values: Reset MCU

         If these bits are changed due to adverse environmental conditions, the microcontroller will be reset. The reset operation will be activated after a delay time, t_{SRESET} and the RSTF bit in the RSTFC register will be set to 1.

- **RSTFC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	RSTF	LVRF	LRF	WRF
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	—	—	—	—	0	x	0	0

<div align="right">"x": unknown</div>

Bit 7~4   Unimplemented, read as "0"

Bit 3   **RSTF**: RSTC register software reset flag
         0: Not occurred
         1: Occurred

         This bit is set to 1 by the RSTC control register software reset and cleared by the application program. Note that this bit can only be cleared to 0 by the application program.

Bit 2   **LVRF**: LVR function reset flag
         Described elsewhere.

Bit 1   **LRF**: LVRC register software reset flag
         Described elsewhere.

Bit 0   **WRF**: WDTC register software reset flag
         Described elsewhere.

Low Voltage Reset – LVR

The microcontroller contains a low voltage reset circuit in order to monitor the supply voltage of the device and provides an MCU reset should the value fall below a certain predefined level.

The LVR function is always enabled with a specific LVR voltage V_{LVR}. If the supply voltage of the device drops to within a range of $0.9V \sim V_{LVR}$ such as might occur when changing the battery in battery powered applications, the LVR will automatically reset the device internally and the LVRF bit in the RSTFC register will also be set to 1. For a valid LVR signal, a low supply voltage, i.e., a voltage in the range between $0.9V \sim V_{LVR}$ must exist for a time greater than that specified by t_{LVR} in the LVR/LVD characteristics. If the low supply voltage state does not exceed this value, the LVR will ignore the low supply voltage and will not perform a reset function. The actual V_{LVR} value can be selected by the LVS bits in the LVRC register. If the LVS7~LVS0 bits are changed to some different values by environmental noise, the LVR will reset the device after a delay time, t_{SRESET}. When this happens, the LRF bit in the RSTFC register will be set to 1. After power on the register will have the value of 01010101B. Note that the LVR function will be automatically disabled when the device enters the SLEEP or IDLE mode.
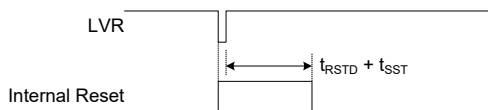
Low Voltage Reset Timing Chart

- **LVRC Register**

Bit	7	6	5	4	3	2	1	0
Name	LVS7	LVS6	LVS5	LVS4	LVS3	LVS2	LVS1	LVS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	1	0	1	0	1	0	1

Bit 7~0   **LVS7~LVS0**: LVR Voltage Select control
        01010101: 2.1V
        00110011: 2.55V
        10011001: 3.15V
        10101010: 3.8V
        Any other value: Generates MCU reset – register is reset to POR value

When an actual low voltage condition occurs, as specified by one of the four defined LVR voltage values above, an MCU reset will be generated. The reset operation will be activated after the low voltage condition keeps more than a t_{LVR} time. In this situation the register contents will remain the same after such a reset occurs.

Any register value, other than the four defined LVR values above, will also result in the generation of an MCU reset. The reset operation will be activated after a delay time, t_{SRESET}. However in this situation the register contents will be reset to the POR value.

- **RSTFC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	RSTF	LVRF	LRF	WRF
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	—	—	—	—	0	x	0	0

"x": unknown

Bit 7~4   Unimplemented, read as "0"

Bit 3   **RSTF**: RSTC register software reset flag
    Described elsewhere

Bit 2   **LVRF**: LVR function reset flag
      0: Not occur
      1: Occurred
    This bit is set to 1 when a specific Low Voltage Reset situation condition occurs. This bit can only be cleared to 0 by the application program.

Bit 1   **LRF**: LVRC register software reset flag
      0: Not occur
      1: Occurred
    This bit is set to 1 if the LVRC register contains any non-defined LVR voltage register values. This in effect acts like a software-reset function. This bit can only be cleared to 0 by the application program.

Bit 0   **WRF**: WDTC register software reset flag
    Describe elsewhere.

Watchdog Time-out Reset during Normal Operation

The Watchdog time-out Reset during normal operations in the FAST or SLOW mode is the same as a LVR reset except that the Watchdog time-out flag TO will be set to "1".
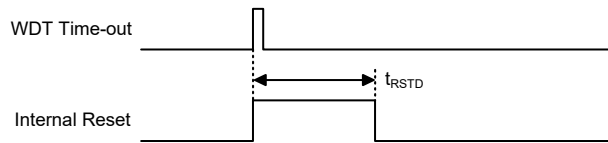
WDT Time-out Reset during Normal Operation Timing Chart

Watchdog Time-out Reset during SLEEP or IDLE Mode

The Watchdog time-out Reset during SLEEP or IDLE Mode is a little different from other kinds of reset. Most of the conditions remain unchanged except that the Program Counter and the Stack Pointer will be cleared to "0" and the TO flag will be set to "1". Refer to the System Start Up Time Characteristics for t_{SST} details.
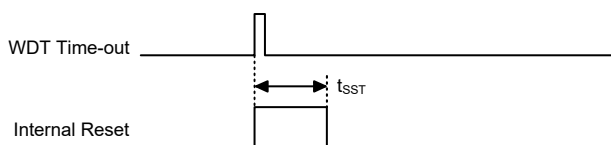
WDT Time-out Reset during SLEEP or IDLE Mode Timing Chart

Reset Initial Conditions

The different types of reset described affect the reset flags in different ways. These flags, known as PDF and TO are located in the status register and are controlled by various microcontroller operations, such as the SLEEP or IDLE Mode function or Watchdog Timer. The reset flags are shown in the table:

TO	PDF	RESET Conditions
0	0	Power-on reset
u	u	LVR reset during FAST or SLOW Mode operation
1	u	WDT time-out reset during FAST or SLOW Mode operation
1	1	WDT time-out reset during IDLE or SLEEP Mode operation

"u" stands for unchanged

The following table indicates the way in which the various components of the microcontroller are affected after a power-on reset occurs.

Item	Condition After RESET
Program Counter	Reset to zero
Interrupts	All interrupts will be disabled
WDT, Time Base	Clear after reset, WDT begins counting
Timer Modules	Timer Modules will be turned off
Input/Output Ports	I/O ports will be setup as input
Stack Pointer	Stack Pointer will point to the top of the stack

The different kinds of resets all affect the internal registers of the microcontroller in different ways. To ensure reliable continuation of normal program execution after a reset occurs, it is important to know what condition the microcontroller is in after a particular reset occurs. The following table describes how each type of reset affects each of the microcontroller internal registers.

Register Name	Power On Reset	LVR Reset	WDT Time-out (FAST/SLOW)	WDT Time-out (IDLE/SLEEP)
IAR0	0000 0000	0000 0000	0000 0000	uuuu uuuu
MP0	0000 0000	0000 0000	0000 0000	uuuu uuuu
IAR1	0000 0000	0000 0000	0000 0000	uuuu uuuu
MP1L	0000 0000	0000 0000	0000 0000	uuuu uuuu
MP1H	0000 0000	0000 0000	0000 0000	uuuu uuuu
ACC	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu
PCL	0000 0000	0000 0000	0000 0000	0000 0000
TBLP	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu
TBLH	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu
TBHP	-xxx xxxx	-uuu uuuu	-uuu uuuu	-uuu uuuu
STATUS	xx00 xxxx	uuuu uuuu	xx1u uuuu	uu11 uuuu
PBP	---- --00	---- --00	---- --00	---- --uu
IAR2	0000 0000	0000 0000	0000 0000	uuuu uuuu
MP2L	0000 0000	0000 0000	0000 0000	uuuu uuuu
MP2H	0000 0000	0000 0000	0000 0000	uuuu uuuu
RSTFC	---- 0x00	---- u1uu	---- uuuu	---- uuuu
SCC	000- 0000	000- 0000	000- 0000	uuu- uuuu
HIRCC	---- 0001	---- 0001	---- 0001	---- uuuu
HXTC	---- -000	---- -000	---- -000	---- -uuu
LXTC	---- --00	---- --00	---- --00	---- --uu
PA	1111 1111	1111 1111	1111 1111	uuuu uuuu
PAC	1111 1111	1111 1111	1111 1111	uuuu uuuu
PAPU	0000 0000	0000 0000	0000 0000	uuuu uuuu
PAWU	0000 0000	0000 0000	0000 0000	uuuu uuuu
RSTC	0101 0101	0101 0101	0101 0101	uuuu uuuu
LVRC	0101 0101	0101 0101	0101 0101	uuuu uuuu
LVDC	--00 0000	--00 0000	--00 0000	--uu uuuu
MFI0	0000 0000	0000 0000	0000 0000	uuuu uuuu
MFI1	0000 0000	0000 0000	0000 0000	uuuu uuuu
MFI2	--00 --00	--00 --00	--00 --00	--uu --uu
WDTC	0101 0011	0101 0011	0101 0011	uuuu uuuu
INTEG	---- 0000	---- 0000	---- 0000	---- uuuu
INTC0	-000 0000	-000 0000	-000 0000	-uuu uuuu
INTC1	0000 0000	0000 0000	0000 0000	uuuu uuuu
INTC2	0000 0000	0000 0000	0000 0000	uuuu uuuu
INTC3	--00 --00	--00 --00	--00 --00	--uu --uu
PB	1--- 1111	1--- 1111	1--- 1111	u--- uuuu
PBC	1--- 1111	1--- 1111	1--- 1111	u--- uuuu
PBPU	0--- 0000	0--- 0000	0--- 0000	u--- uuuu
PC	--11 1111	--11 1111	--11 1111	--uu uuuu
PCC	--11 1111	--11 1111	--11 1111	--uu uuuu
PCPU	--00 0000	--00 0000	--00 0000	--uu uuuu
PSCR	---- --00	---- --00	---- --00	---- --uu
TB0C	0--- -000	0--- -000	0--- -000	u--- -uuu
TB1C	0--- -000	0--- -000	0--- -000	u--- -uuu
U0SR	0000 1011	0000 1011	0000 1011	uuuu uuuu
U0CR1	0000 00x0	0000 00x0	0000 00x0	uuuu uuuu

Register Name	Power On Reset	LVR Reset	WDT Time-out (FAST/SLOW)	WDT Time-out (IDLE/SLEEP)
U0CR2	0000 0000	0000 0000	0000 0000	uuuu uuuu
TXR_RXR0	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
BRG0	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
SIMC0	111- 0000	111- 0000	111- 0000	uuu- uuuu
SIMC1	1000 0001	1000 0001	1000 0001	uuuu uuuu
SIMD	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
SIMA/SIMC2	0000 0000	0000 0000	0000 0000	uuuu uuuu
SIMTOC	0000 0000	0000 0000	0000 0000	uuuu uuuu
SPIAC0	111- --00	111- --00	111- --00	uuu- --uu
SPIAC1	--00 0000	--00 0000	--00 0000	--uu uuuu
SPIAD	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
EEA	--00 0000	--00 0000	--00 0000	--uu uuuu
EED	0000 0000	0000 0000	0000 0000	uuuu uuuu
U1SR	0000 1011	0000 1011	0000 1011	uuuu uuuu
U1CR1	0000 00x0	0000 00x0	0000 00x0	uuuu uuuu
U1CR2	0000 0000	0000 0000	0000 0000	uuuu uuuu
TXR_RXR1	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
BRG1	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
STMC0	0000 0---	0000 0---	0000 0---	uuuu u---
STMC1	0000 0000	0000 0000	0000 0000	uuuu uuuu
STMDL	0000 0000	0000 0000	0000 0000	uuuu uuuu
STMDH	0000 0000	0000 0000	0000 0000	uuuu uuuu
STMAL	0000 0000	0000 0000	0000 0000	uuuu uuuu
STMAH	0000 0000	0000 0000	0000 0000	uuuu uuuu
STMRP	0000 0000	0000 0000	0000 0000	uuuu uuuu
PTM0C0	0000 0---	0000 0---	0000 0---	uuuu u---
PTM0C1	0000 0000	0000 0000	0000 0000	uuuu uuuu
PTM0DL	0000 0000	0000 0000	0000 0000	uuuu uuuu
PTM0DH	---- --00	---- --00	---- --00	---- --uu
PTM0AL	0000 0000	0000 0000	0000 0000	uuuu uuuu
PTM0AH	---- --00	---- --00	---- --00	---- --uu
PTM0RPL	0000 0000	0000 0000	0000 0000	uuuu uuuu
PTM0RPH	---- --00	---- --00	---- --00	---- --uu
MDUWR0	xxxx xxxx	0000 0000	0000 0000	uuuu uuuu
MDUWR1	xxxx xxxx	0000 0000	0000 0000	uuuu uuuu
MDUWR2	xxxx xxxx	0000 0000	0000 0000	uuuu uuuu
MDUWR3	xxxx xxxx	0000 0000	0000 0000	uuuu uuuu
MDUWR4	xxxx xxxx	0000 0000	0000 0000	uuuu uuuu
MDUWR5	xxxx xxxx	0000 0000	0000 0000	uuuu uuuu
MDUWCTRL	00-- ----	00-- ----	00-- ----	uu-- ----
OVPC0	--00 -000	--00 -000	--00 -000	--uu -uuu
OVPC1	0001 0000	0001 0000	0001 0000	uuuu uuuu
OVPDA	0000 0000	0000 0000	0000 0000	uuuu uuuu
SADOL	xxxx ----	xxxx ----	xxxx ----	uuuu --- (ADRFS=0) uuuu uuuu (ADRFS=1)

Register Name	Power On Reset	LVR Reset	WDT Time-out (FAST/SLOW)	WDT Time-out (IDLE/SLEEP)
SADOH	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu (ADRFS=0) / ---- uuuu (ADRFS=1)
SADC0	0000 0000	0000 0000	0000 0000	uuuu uuuu
SADC1	0000 0000	0000 0000	0000 0000	uuuu uuuu
IREFC	---0 --00	---0 --00	---0 --00	---u --uu
PVREF	0000 0000	0000 0000	0000 0000	uuuu uuuu
OPAC	0000 0000	0000 0000	0000 0000	uuuu uuuu
GSC	---- 0000	---- 0000	---- 0000	---- uuuu
AFEDAC	---- --00	---- --00	---- --00	---- --uu
AFEDAL	00-- ----	00-- ----	00-- ----	uu-- ----
AFEDAH	0000 0000	0000 0000	0000 0000	uuuu uuuu
LCDC0	0000 -000	0000 -000	0000 -000	uuuu -uuu
LCDCP	---- 0-00	---- 0-00	---- 0-00	---- u-uu
LCDC2	000- -000	000- -000	000- -000	uuu- -uuu
PD	1111 1111	1111 1111	1111 1111	uuuu uuuu
PDC	1111 1111	1111 1111	1111 1111	uuuu uuuu
PDPU	0000 0000	0000 0000	0000 0000	uuuu uuuu
PE	1111 1111	1111 1111	1111 1111	uuuu uuuu
PEC	1111 1111	1111 1111	1111 1111	uuuu uuuu
PEPU	0000 0000	0000 0000	0000 0000	uuuu uuuu
PF	1111 1111	1111 1111	1111 1111	uuuu uuuu
PFC	1111 1111	1111 1111	1111 1111	uuuu uuuu
PFPU	0000 0000	0000 0000	0000 0000	uuuu uuuu
PG	---- -111	---- -111	---- -111	---- -uuu
PGC	---- -111	---- -111	---- -111	---- -uuu
PGPU	---- -000	---- -000	---- -000	---- -uuu
PTM1C0	0000 0---	0000 0---	0000 0---	uuuu u---
PTM1C1	0000 0000	0000 0000	0000 0000	uuuu uuuu
PTM1DL	0000 0000	0000 0000	0000 0000	uuuu uuuu
PTM1DH	---- --00	---- --00	---- --00	---- --uu
PTM1AL	0000 0000	0000 0000	0000 0000	uuuu uuuu
PTM1AH	---- --00	---- --00	---- --00	---- --uu
PTM1RPL	0000 0000	0000 0000	0000 0000	uuuu uuuu
PTM1RPH	---- --00	---- --00	---- --00	---- --uu
PTM2C0	0000 0---	0000 0---	0000 0---	uuuu u---
PTM2C1	0000 0000	0000 0000	0000 0000	uuuu uuuu
PTM2DL	0000 0000	0000 0000	0000 0000	uuuu uuuu
PTM2DH	---- --00	---- --00	---- --00	---- --uu
PTM2AL	0000 0000	0000 0000	0000 0000	uuuu uuuu
PTM2AH	---- --00	---- --00	---- --00	---- --uu
PTM2RPL	0000 0000	0000 0000	0000 0000	uuuu uuuu
PTM2RPH	---- --00	---- --00	---- --00	---- --uu
EEC	---- 0000	---- 0000	---- 0000	---- uuuu
FC0	0000 0000	0000 0000	0000 0000	uuuu uuuu
FC1	0000 0000	0000 0000	0000 0000	uuuu uuuu
FC2	---- ---0	---- ---0	---- ---0	---- ---u

Register Name	Power On Reset	LVR Reset	WDT Time-out (FAST/SLOW)	WDT Time-out (IDLE/SLEEP)
FARL	0000 0000	0000 0000	0000 0000	uuuu uuuu
FARH	-000 0000	-000 0000	-000 0000	-uuu uuuu
FD0L	0000 0000	0000 0000	0000 0000	uuuu uuuu
FD0H	0000 0000	0000 0000	0000 0000	uuuu uuuu
FD1L	0000 0000	0000 0000	0000 0000	uuuu uuuu
FD1H	0000 0000	0000 0000	0000 0000	uuuu uuuu
FD2L	0000 0000	0000 0000	0000 0000	uuuu uuuu
FD2H	0000 0000	0000 0000	0000 0000	uuuu uuuu
FD3L	0000 0000	0000 0000	0000 0000	uuuu uuuu
FD3H	0000 0000	0000 0000	0000 0000	uuuu uuuu
IFS0	000- 0-00	000- 0-00	000- 0-00	uuu- u-uu
IFS1	-000 -0--	-000 -0--	-000 -0--	-uuu -u--
PAS0	0000 0000	0000 0000	0000 0000	uuuu uuuu
PAS1	0000 0000	0000 0000	0000 0000	uuuu uuuu
PBS0	0000 0000	0000 0000	0000 0000	uuuu uuuu
PBS1	00-- ----	00-- ----	00-- ----	uu-- ----
PCS0	0000 0000	0000 0000	0000 0000	uuuu uuuu
PCS1	---- 0000	---- 0000	---- 0000	---- uuuu
PDS0	0000 0000	0000 0000	0000 0000	uuuu uuuu
PDS1	0000 0000	0000 0000	0000 0000	uuuu uuuu
PES0	0000 0000	0000 0000	0000 0000	uuuu uuuu
PES1	0000 0000	0000 0000	0000 0000	uuuu uuuu
PGS0	--00 0000	--00 0000	--00 0000	--uu uuuu
SLEDC0	0000 0000	0000 0000	0000 0000	uuuu uuuu
SLEDC1	0000 0000	0000 0000	0000 0000	uuuu uuuu
SLEDC2	0000 0000	0000 0000	0000 0000	uuuu uuuu
SLEDC3	---- --00	---- --00	---- --00	---- --uu

Note: "u" stands for unchanged

"x" stands for unknown

"-" stands for unimplemented

Input/Output Ports

Holtek microcontrollers offer considerable flexibility on their I/O ports. With the input or output designation of every pin fully under user program control, pull-high selections for all ports and wake-up selections on certain pins, the user is provided with an I/O structure to meet the needs of a wide range of application possibilities.

The device provides bidirectional input/output lines labeled with port names PA~PG. These I/O ports are mapped to the RAM Data Memory with specific addresses as shown in the Special Purpose Data Memory table. All of these I/O ports can be used for input and output operations. For input operation, these ports are non-latching, which means the inputs must be ready at the T2 rising edge of instruction "MOV A, [m]", where m denotes the port address. For output operation, all the data is latched and remains unchanged until the output latch is rewritten.

Register Name	Bit							
	7	6	5	4	3	2	1	0
PA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
PAC	PAC7	PAC6	PAC5	PAC4	PAC3	PAC2	PAC1	PAC0
PAPU	PAPU7	PAPU6	PAPU5	PAPU4	PAPU3	PAPU2	PAPU1	PAPU0
PAWU	PAWU7	PAWU6	PAWU5	PAWU4	PAWU3	PAWU2	PAWU1	PAWU0
PB	PB7	—	—	—	PB3	PB2	PB1	PB0
PBC	PBC7	—	—	—	PBC3	PBC2	PBC1	PBC0
PBPU	PBPU7	—	—	—	PBPU3	PBPU2	PBPU1	PBPU0
PC	—	—	PC5	PC4	PC3	PC2	PC1	PC0
PCC	—	—	PCC5	PCC4	PCC3	PCC2	PCC1	PCC0
PCPU	—	—	PCPU5	PCPU4	PCPU3	PCPU2	PCPU1	PCPU0
PD	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
PDC	PDC7	PDC6	PDC5	PDC4	PDC3	PDC2	PDC1	PDC0
PDPU	PDPU7	PDPU6	PDPU5	PDPU4	PDPU3	PDPU2	PDPU1	PDPU0
PE	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
PEC	PEC7	PEC6	PEC5	PEC4	PEC3	PEC2	PEC1	PEC0
PEPU	PEPU7	PEPU6	PEPU5	PEPU4	PEPU3	PEPU2	PEPU1	PEPU0
PF	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
PFC	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0
PFPU	PFPU7	PFPU6	PFPU5	PFPU4	PFPU3	PFPU2	PFPU1	PFPU0
PG	—	—	—	—	—	PG2	PG1	PG0
PGC	—	—	—	—	—	PGC2	PGC1	PGC0
PGPU	—	—	—	—	—	PGPU2	PGPU1	PGPU0

"—": Unimplemented, read as "0"

I/O Logic Function Register List

Pull-high Resistors

Many product applications require pull-high resistors for their switch inputs usually requiring the use of an external resistor. To eliminate the need for these external resistors, all I/O pins, when configured as an input have the capability of being connected to an internal pull-high resistor. These pull-high resistors are selected using registers, namely PAPU~PGPU, and are implemented using weak PMOS transistors.

Note that the pull-high resistor can be controlled by the relevant pull-high control register only when the pin-shared functional pin is selected as a logic input or NMOS output. Otherwise, the pull-high resistors cannot be enabled.

- **PxPU Register**

Bit	7	6	5	4	3	2	1	0
Name	PxPU7	PxPU6	PxPU5	PxPU4	PxPU3	PxPU2	PxPU1	PxPU0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

PxPUn: I/O Port x Pin pull-high function control
    0: Disable
    1: Enable

The PxPUn bit is used to control the pin pull-high function. Here the "x" can be A, B, C, D, E, F and G. However, the actual available bits for each I/O Port may be different.

Port A Wake-up

The HALT instruction forces the microcontroller into the SLEEP or IDLE Mode which preserves power, a feature that is important for battery and other low-power applications. Various methods exist to wake-up the microcontroller, one of which is to change the logic condition on one of the Port A pins from high to low. This function is especially suitable for applications that can be woken up via external switches. Each pin on Port A can be selected individually to have this wake-up feature using the PAWU register.

Note that the wake-up function can be controlled by the wake-up control registers only when the pin-shared function is selected as general purpose input/output and the MCU enters the Power down mode.

- **PAWU Register**

Bit	7	6	5	4	3	2	1	0
Name	PAWU7	PAWU6	PAWU5	PAWU4	PAWU3	PAWU2	PAWU1	PAWU0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   **PAWU7~PAWU0**: PA7~PA0 wake-up function control
        0: Disable
        1: Enable

I/O Port Control Registers

Each I/O port has its own control register known as PAC~PGC, to control the input/output configuration. With this control register, each CMOS output or input can be reconfigured dynamically under software control. Each pin of the I/O ports is directly mapped to a bit in its associated port control register. For the I/O pin to function as an input, the corresponding bit of the control register must be written as a "1". This will then allow the logic state of the input pin to be directly read by instructions. When the corresponding bit of the control register is written as a "0", the I/O pin will be setup as a CMOS output. If the pin is currently setup as an output, instructions can still be used to read the output register. However, it should be noted that the program will in fact only read the status of the output data latch and not the actual logic status of the output pin.

- **PxC Register**

Bit	7	6	5	4	3	2	1	0
Name	PxC7	PxC6	PxC5	PxC4	PxC3	PxC2	PxC1	PxC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

PxCn: I/O Port x Pin type selection
    0: Output
    1: Input

The PxCn bit is used to control the pin type selection. Here the "x" can be A, B, C, D, E, F and G. However, the actual available bits for each I/O Port may be different.

Source Current Selection

Each pin in this device can be configured with different output source current which is selected by the corresponding source current selection bits. These source current selection bits are available when the corresponding pin is configured as a CMOS output. Otherwise, these select bits have no effect. Users should refer to the Input/Output Characteristics section to obtain the exact value for different applications.

Register Name	Bit							
	7	6	5	4	3	2	1	0
SLEDC0	SLEDC07	SLEDC06	SLEDC05	SLEDC04	SLEDC03	SLEDC02	SLEDC01	SLEDC00
SLEDC1	SLEDC17	SLEDC16	SLEDC15	SLEDC14	SLEDC13	SLEDC12	SLEDC11	SLEDC10
SLEDC2	SLEDC27	SLEDC26	SLEDC25	SLEDC24	SLEDC23	SLEDC22	SLEDC21	SLEDC20
SLEDC3	—	—	—	—	—	—	SLEDC31	SLEDC30

I/O Port Source Current Selection Registers List

• **SLEDC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	SLEDC07	SLEDC06	SLEDC05	SLEDC04	SLEDC03	SLEDC02	SLEDC01	SLEDC00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **SLEDC07~SLEDC06**: PB7 source current selection
         00: Source current=Level 0 (Min.)
         01: Source current=Level 1
         10: Source current=Level 2
         11: Source current=Level 3 (Max.)

Bit 5~4   **SLEDC05~SLEDC04**: PB3~PB0 source current selection
         00: Source current=Level 0 (Min.)
         01: Source current=Level 1
         10: Source current=Level 2
         11: Source current=Level 3 (Max.)

Bit 3~2   **SLEDC03~SLEDC02**: PA7~PA4 source current selection
         00: Source current=Level 0 (Min.)
         01: Source current=Level 1
         10: Source current=Level 2
         11: Source current=Level 3 (Max.)

Bit 1~0   **SLEDC01~SLEDC00**: PA3~PA0 source current selection
         00: Source current=Level 0 (Min.)
         01: Source current=Level 1
         10: Source current=Level 2
         11: Source current=Level 3 (Max.)

     Note: Users should refer to the Input/Output Characteristics section to obtain the exact value for different applications

- **SLEDC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	SLEDC17	SLEDC16	SLEDC15	SLEDC14	SLEDC13	SLEDC12	SLEDC11	SLEDC10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **SLEDC17~SLEDC16**: PD7~PD4 source current selection
     00: Source current=Level 0 (Min.)
     01: Source current=Level 1
     10: Source current=Level 2
     11: Source current=Level 3 (Max.)

Bit 5~4   **SLEDC15~SLEDC14**: PD3~PD0 source current selection
     00: Source current=Level 0 (Min.)
     01: Source current=Level 1
     10: Source current=Level 2
     11: Source current=Level 3 (Max.)

Bit 3~2   **SLEDC13~SLEDC12**: PC5 and PC4 source current selection
     00: Source current=Level 0 (Min.)
     01: Source current=Level 1
     10: Source current=Level 2
     11: Source current=Level 3 (Max.)

Bit 1~0   **SLEDC11~SLEDC10**: PC3~PC0 source current selection
     00: Source current=Level 0 (Min.)
     01: Source current=Level 1
     10: Source current=Level 2
     11: Source current=Level 3 (Max.)

     Note: Users should refer to the Input/Output Characteristics section to obtain the exact value for different applications

- **SLEDC2 Register**

Bit	7	6	5	4	3	2	1	0
Name	SLEDC27	SLEDC26	SLEDC25	SLEDC24	SLEDC23	SLEDC22	SLEDC21	SLEDC20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **SLEDC27~SLEDC26**: PF7~PF4 source current selection
     00: Source current=Level 0 (Min.)
     01: Source current=Level 1
     10: Source current=Level 2
     11: Source current=Level 3 (Max.)

Bit 5~4   **SLEDC25~SLEDC24**: PF3~PF0 source current selection
     00: Source current=Level 0 (Min.)
     01: Source current=Level 1
     10: Source current=Level 2
     11: Source current=Level 3 (Max.)

Bit 3~2   **SLEDC23~SLEDC22**: PE7~PE4 source current selection
     00: Source current=Level 0 (Min.)
     01: Source current=Level 1
     10: Source current=Level 2
     11: Source current=Level 3 (Max.)

Bit 1~0   **SLEDC21~SLEDC20**: PE3~PE0 source current selection
     00: Source current=Level 0 (Min.)
     01: Source current=Level 1
     10: Source current=Level 2
     11: Source current=Level 3 (Max.)

     Note: Users should refer to the Input/Output Characteristics section to obtain the exact value for different applications

- **SLEDC3 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	SLEDC31	SLEDC30
R/W	—	—	—	—	—	—	R/W	R/W
POR	—	—	—	—	—	—	0	0

Bit 7~2   Unimplemented, read as "0"

Bit 1~0   **SLEDC31~SLEDC30**: PG2~PG0 source current selection
        00: Source current=Level 0 (Min.)
        01: Source current=Level 1
        10: Source current=Level 2
        11: Source current=Level 3 (Max.)
      Note: Users should refer to the Input/Output Characteristics section to obtain the exact
             value for different applications.

Pin-shared Functions

The flexibility of the microcontroller range is greatly enhanced by the use of pins that have more than one function. Limited numbers of pins can force serious design constraints on designers but by supplying pins with multi-functions, many of these difficulties can be overcome. For these pins, the desired function of the multi-function I/O pins is selected by a series of registers via the application program control.

Pin-shared Function Selection Registers

The limited number of supplied pins in a package can impose restrictions on the amount of functions a certain device can contain. However by allowing the same pins to share several different functions and providing a means of function selection, a wide range of different functions can be incorporated into even relatively small package sizes. The device includes Port A~Port G Output Function Selection registers and Input Function Selection registers, which can select the desired function of the multi-function pin-shared pins.

The most important point to note is to make sure that the desired pin-shared function is properly selected and also deselected. For most pin-shared functions, to select the desired pin-shared function, the pin-shared function should first be correctly selected using the corresponding pin-shared control register. After that the corresponding peripheral functional setting should be configured and then the peripheral function can be enabled. However, a special point must be noted for some digital input pins, such as INTn, xTCKn, xTPnI, etc, which share the same pin-shared control configuration with their corresponding general purpose I/O functions when setting the relevant pin-shared control bit fields. To select these pin functions, in addition to the necessary pin-shared control and peripheral functional setup aforementioned, they must also be setup as an input by setting the corresponding bit in the I/O port control register. To correctly deselect the pin-shared function, the peripheral function should first be disabled and then the corresponding pin-shared function control register can be modified to select other pin-shared function.

Register Name	Bit							
	7	6	5	4	3	2	1	0
IFS0	PTP2IPS	PTP1IPS	PTP0IPS	—	PTCK2PS	—	—	STCKPS
IFS1	—	SCSABPS	SDIAPS	SCKAPS	—	—	—	—
PAS0	PAS07	PAS06	PAS05	PAS04	PAS03	PAS02	PAS01	PAS00
PAS1	PAS17	PAS16	PAS15	PAS14	PAS13	PAS12	PAS11	PAS10
PBS0	PBS07	PBS06	PBS05	PBS04	PBS03	PBS02	PBS01	PBS00
PBS1	PBS17	PBS16	—	—	—	—	—	—

Register Name	Bit							
	7	6	5	4	3	2	1	0
PCS0	PCS07	PCS06	PCS05	PCS04	PCS03	PCS02	PCS01	PCS00
PCS1	—	—	—	—	PCS13	PCS12	PCS11	PCS10
PDS0	PDS07	PDS06	PDS05	PDS04	PDS03	PDS02	PDS01	PDS00
PDS1	PDS17	PDS16	PDS15	PDS14	PDS13	PDS12	PDS11	PDS10
PES0	PES07	PES06	PES05	PES04	PES03	PES02	PES01	PES00
PES1	PES17	PES16	PES15	PES14	PES13	PES12	PES11	PES10
PFS0	PFS07	PFS06	PFS05	PFS04	PFS03	PFS02	PFS01	PFS00
PFS1	PFS17	PFS16	PFS15	PFS14	PFS13	PFS12	PFS11	PFS10
PGS0	—	—	PGS05	PGS04	PGS03	PGS02	PGS01	PGS00

Pin-shared Function Selection Register List

• **PAS0 Register**

Bit	7	6	5	4	3	2	1	0
Name	PAS07	PAS06	PAS05	PAS04	PAS03	PAS02	PAS01	PAS00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6 **PAS07~PAS06**: PA3 Pin-Shared function selection
    00: PA3/PTP1I
    01: PTP1
    10: SDOA
    11: OSC2

Bit 5~4 **PAS05~PAS04**: PA2 Pin-Shared function selection
    00/01/10: PA2/PTCK0
    11: XT2

Bit 3~2 **PAS03~PAS02**: PA1 Pin-Shared function selection
    00: PA1/INT0/STCK
    01: OVPVR
    10: LVDIN
    11: PTP0B

Bit 1~0 **PAS01~PAS00**: PA0 Pin-Shared function selection
    00/01: PA0/PTP0I
    10: PTP0
    11: XT1

• **PAS1 Register**

Bit	7	6	5	4	3	2	1	0
Name	PAS17	PAS16	PAS15	PAS14	PAS13	PAS12	PAS11	PAS10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6 **PAS17~PAS16**: PA7 Pin-Shared function selection
    00: PA7/PTCK2
    01: SEG44
    10: OVPI
    11: SDI/SDA

Bit 5~4 **PAS15~PAS14**: PA6 Pin-Shared function selection
    00: PA6/STCK
    01: SDIA
    10: OVPI
    11: RX0

Bit 3~2   **PAS13~PAS12**: PA5 Pin-Shared function selection
        00: PA5/STPI
        01: STP
        10: SCKA
        11: TX0

Bit 1~0   **PAS11~PAS10**: PA4 Pin-Shared function selection
        00: PA4/PTP2I
        01: PTP2
        10: $\overline{\text{SCSA}}$
        11: OSC1

- **PBS0 Register**

Bit	7	6	5	4	3	2	1	0
Name	PBS07	PBS06	PBS05	PBS04	PBS03	PBS02	PBS01	PBS00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **PBS07~PBS06**: PB3 Pin-Shared function selection
        00: PB3
        01: SEG40
        10: SDIA
        11: SDO

Bit 5~4   **PBS05~PBS04**: PB2 Pin-Shared function selection
        00: PB2
        01: SEG41
        10: $\overline{\text{SCS}}$
        11: SCKA

Bit 3~2   **PBS03~PBS02**: PB1 Pin-Shared function selection
        00: PB1/INT1
        01: SEG42
        10: STPB
        11: OVPI

Bit 1~0   **PBS01~PBS00**: PB0 Pin-Shared function selection
        00: PB0
        01: SEG43
        10: SCK/SCL
        11: OVPI

- **PBS1 Register**

Bit	7	6	5	4	3	2	1	0
Name	PBS17	PBS16	—	—	—	—	—	—
R/W	R/W	R/W	—	—	—	—	—	—
POR	0	0	—	—	—	—	—	—

Bit 7~6   **PBS17~PBS16**: PB7 Pin-Shared function selection
        00/01/10: PB7
        11: VG

Bit 5~0   Unimplemented, read as "0"

- **PCS0 Register**

Bit	7	6	5	4	3	2	1	0
Name	PCS07	PCS06	PCS05	PCS04	PCS03	PCS02	PCS01	PCS00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **PCS07~PCS06**: PC3 Pin-Shared function selection
           00/01/10: PC3/PTCK2
           11:AN1

Bit 5~4   **PCS05~PCS04**: PC2 Pin-Shared function selection
           00: PC2/PTP2I
           01: PTP2
           10: VREF
           11: AN0

Bit 3~2   **PCS03~PCS02**: PC1 Pin-Shared function selection
           00/01/10: PC1/PTCK1
           11: AN3

Bit 1~0   **PCS01~PCS00**: PC0 Pin-Shared function selection
           00/01: PC0/PTP1I
           10: PTP1
           11: AN2

- **PCS1 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	PCS13	PCS12	PCS11	PCS10
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	—	—	—	—	0	0	0	0

Bit 7~4   Unimplemented, read as "0"

Bit 3~2   **PCS13~PCS12**: PC5 Pin-Shared function selection
           00/01: PC5
           10: TX1
           11: SDOA

Bit 1~0   **PCS11~PCS10**: PC4 Pin-Shared function selection
           00/01: PC4
           10: RX1
           11: SCSA

- **PDS0 Register**

Bit	7	6	5	4	3	2	1	0
Name	PDS07	PDS06	PDS05	PDS04	PDS03	PDS02	PDS01	PDS00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **PDS07~PDS06**: PD3 Pin-Shared function selection
           00/01: PD3
           10: SEG3
           11: COM7

Bit 5~4   **PDS05~PDS04**: PD2 Pin-Shared function selection
           00/01: PD2
           10: SEG2
           11: COM6

Bit 3~2   **PDS03~PDS02**: PD1 Pin-Shared function selection
             00/01: PD1
             10: SEG1
             11: COM5

Bit 1~0   **PDS01~PDS00**: PD0 Pin-Shared function selection
             00/01: PD0
             10: SEG0
             11: COM4

- **PDS1 Register**

Bit	7	6	5	4	3	2	1	0
Name	PDS17	PDS16	PDS15	PDS14	PDS13	PDS12	PDS11	PDS10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **PDS17~PDS16**: PD7 Pin-Shared function selection
             00/01/10: PD7
             11: SEG39

Bit 5~4   **PDS15~PDS14**: PD6 Pin-Shared function selection
             00/01/10: PD6
             11: SEG38

Bit 3~2   **PDS13~PDS12**: PD5 Pin-Shared function selection
             00/01/10: PD5
             11: SEG37

Bit 1~0   **PDS11~PDS10**: PD4 Pin-Shared function selection
             00/01/10: PD4
             11: SEG36

- **PES0 Register**

Bit	7	6	5	4	3	2	1	0
Name	PES07	PES06	PES05	PES04	PES03	PES02	PES01	PES00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **PES07~PES06**: PE3 Pin-Shared function selection
             00/01/10: PE3
             11: SEG31

Bit 5~4   **PES05~PES04**: PE2 Pin-Shared function selection
             00/01/10: PE2
             11: SEG30

Bit 3~2   **PES03~PES02**: PE1 Pin-Shared function selection
             00/01/10: PE1
             11: SEG29

Bit 1~0   **PES01~PES00**: PE0 Pin-Shared function selection
             00/01/10: PE0
             11: SEG28

- **PES1 Register**

Bit	7	6	5	4	3	2	1	0
Name	PES17	PES16	PES15	PES14	PES13	PES12	PES11	PES10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **PES17~PES16**: PE7 Pin-Shared function selection
             00/01/10: PE7
             11: SEG35

Bit 5~4   **PES15~PES14**: PE6 Pin-Shared function selection
00/01/10: PE6
11: SEG34

Bit 3~2   **PES13~PES12**: PE5 Pin-Shared function selection
00/01/10: PE5
11: SEG33

Bit 1~0   **PES11~PES10**: PE4 Pin-Shared function selection
00/01/10: PE4
11: SEG32

- **PFS0 Register**

Bit	7	6	5	4	3	2	1	0
Name	PFS07	PFS06	PFS05	PFS04	PFS03	PFS02	PFS01	PFS00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **PFS07~PFS06**: PF3 Pin-Shared function selection
00/01/10: PF3
11: SEG23

Bit 5~4   **PFS05~PFS04**: PF2 Pin-Shared function selection
00/01/10: PF2
11: SEG22

Bit 3~2   **PFS03~PFS02**: PF1 Pin-Shared function selection
00/01/10: PF1
11: SEG21

Bit 1~0   **PFS01~PFS00**: PF0 Pin-Shared function selection
00/01/10: PF0
11: SEG20

- **PFS1 Register**

Bit	7	6	5	4	3	2	1	0
Name	PFS17	PFS16	PFS15	PFS14	PFS13	PFS12	PFS11	PFS10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **PFS17~PFS16**: PF7 Pin-Shared function selection
00/01/10: PF7
11: SEG27

Bit 5~4   **PFS15~PFS14**: PF6 Pin-Shared function selection
00/01/10: PF6
11: SEG26

Bit 3~2   **PFS13~PFS12**: PF5 Pin-Shared function selection
00/01/10: PF5
11: SEG25

Bit 1~0   **PFS11~PFS10**: PF4 Pin-Shared function selection
00/01/10: PF4
11: SEG24

- **PGS0 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	PGS05	PGS04	PGS03	PGS02	PGS01	PGS00
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

Bit 7~6   Unimplemented, read as "0"

Bit 5~4   **PGS05~PGS04**: PG2 Pin-Shared function selection
　　　　　00/01: PG2
　　　　　10: V2
　　　　　11: SEG47

Bit 3~2   **PGS03~PGS02**: PG1 Pin-Shared function selection
　　　　　00/01: PG1
　　　　　10: C2
　　　　　11: SEG46

Bit 1~0   **PGS01~PGS00**: PG0 Pin-Shared function selection
　　　　　00/01: PG0
　　　　　10: C1
　　　　　11: SEG45

- **IFS0 Register**

Bit	7	6	5	4	3	2	1	0
Name	PTP2IPS	PTP1IPS	PTP0IPS	—	PTCK2PS	—	—	STCKPS
R/W	R/W	R/W	R/W	—	R/W	—	—	R/W
POR	0	0	0	—	0	—	—	0

Bit 7   **PTP2IPS**: PTP2I input source pin selection
　　　　0: PA4
　　　　1: PC2

Bit 6   **PTP1IPS**: PTP1I input source pin selection
　　　　0: PA3
　　　　1: PC0

Bit 5   **PTP0IPS**: PTP0I input source pin selection
　　　　0: PA0
　　　　1: Internal connected to OVPINT

Bit 4   Unimplemented, read as "0"

Bit 3   **PTCK2PS**: PTCK2 input source pin selection
　　　　0: PC3
　　　　1: PA7

Bit 2~1   Unimplemented, read as "0"

Bit 0   **STCKPS**: STCK input source pin selection
　　　　0: PA1
　　　　1: PA6

- **IFS1 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	SCSABPS	SDIAPS	SCKAPS	—	—	—	—
R/W	—	R/W	R/W	R/W	—	—	—	—
POR	—	0	0	0	—	—	—	—

Bit 7   Unimplemented, read as "0"

Bit 6   **SCSABPS**: $\overline{\text{SCSA}}$ input source pin selection
　　　　0: PA4
　　　　1: PC4

Bit 5   **SDIAPS**: SDIA input source pin selection
　　　　0: PA6
　　　　1: PB3

Bit 4   **SCKAPS**: SCKA input source pin selection
　　　　0: PA5
　　　　1: PB2

Bit 3~0   Unimplemented, read as "0"

I/O Pin Structures

The accompanying diagram illustrates the internal structure of the I/O logic function. As the exact logical construction of the I/O pin will differ from this drawing, it is supplied as a guide only to assist with the functional understanding of the I/O logic function. The wide range of pin-shared structures does not permit all types to be shown.

Logic Function Input/Output Structure
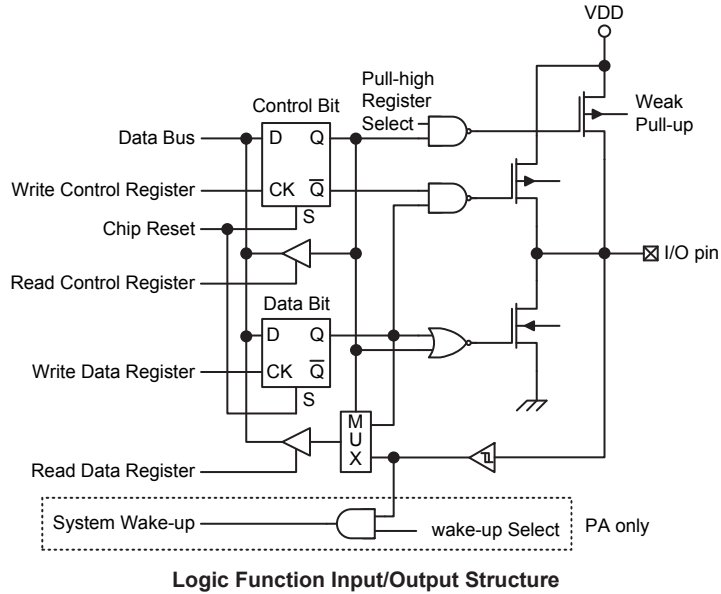
Programming Considerations

Within the user program, one of the first things to consider is port initialisation. After a reset, all of the I/O data and port control registers will be set high. This means that all I/O pins will default to an input state, the level of which depends on the other connected circuitry and whether pull-high selections have been chosen. If the port control registers are then programmed to setup some pins as outputs, these output pins will have an initial high output value unless the associated port data registers are first programmed. Selecting which pins are inputs and which are outputs can be achieved byte-wide by loading the correct values into the appropriate port control register or by programming individual bits in the port control register using the "SET [m].i" and "CLR [m].i" instructions. Note that when using these bit control instructions, a read-modify-write operation takes place. The microcontroller must first read in the data on the entire port, modify it to the required new bit values and then rewrite this data back to the output ports.

Port A has the additional capability of providing wake-up function. When the device is in the SLEEP or IDLE Mode, various methods are available to wake the device up. One of these is a high to low transition of any of the Port A pins. Single or multiple pins on Port A can be setup to have this function.

Timer Modules – TM

One of the most fundamental functions in any microcontroller devices is the ability to control and measure time. To implement time related functions the device includes several Timer Modules, generally abbreviated to the name TM. The TMs are multi-purpose timing units and serve to provide operations such as Timer/Counter, Input Capture, Compare Match Output and Single Pulse Output as well as being the functional unit for the generation of PWM signals. Each of the TMs has two interrupts. The addition of input and output pins for each TM ensures that users are provided with timing units with a wide and flexible range of features.

The common features of the different TM types are described here with more detailed information provided in the individual Standard and Periodic TM sections.

Introduction

The device contains four TMs and each individual TM can be categorised as a certain type, namely Standard Type TM or Periodic Type TM. Although similar in nature, the different TM types vary in their feature complexity. The common features to all of the Standard and Periodic TMs will be described in this section and the detailed operation regarding each of the TM types will be described in separate sections. The main features and differences between the two TM types are summarised in the accompanying table.

TM Function	STM	PTM
Timer/Counter	√	√
Input Capture	√	√
Compare Match Output	√	√
PWM Channels	1	1
Single Pulse Output	1	1
PWM Alignment	Edge	Edge
PWM Adjustment Period & Duty	Duty or Period	Duty or Period

TM Function Summary

TM Operation

The different types of TM offer a diverse range of functions, from simple timing operations to PWM signal generation. The key to understanding how the TM operates is to see it in terms of a free running count-up counter whose value is then compared with the value of pre-programmed internal comparators. When the free running count-up counter has the same value as the pre-programmed comparator, known as a compare match situation, a TM interrupt signal will be generated which can clear the counter and perhaps also change the condition of the TM output pin. The internal TM counter is driven by a user selectable clock source, which can be an internal clock or an external pin.

TM Clock Source

The clock source which drives the main counter in each TM can originate from various sources. The selection of the required clock source is implemented using the STCK2~STCK0 and PTnCK2~PTnCK0 bits in the STM and PTMn control registers, where "n" stands for the specific TM serial number. The clock source can be a ratio of the system clock, f_{SYS}, or the internal high clock, f_H, the f_{SUB} clock source or from the external STCK and PTCKn pin. The STCK and PTCKn pin clock source is used to allow an external signal to drive the TM as an external clock source for event counting.

TM Interrupts

The Standard or Periodic type TM has two internal interrupt, one for each of the internal comparator A or comparator P, which generate a TM interrupt when a compare match condition occurs. When a TM interrupt is generated, it can be used to clear the counter and also to change the state of the TM output pin.

TM External Pins

Each of the STM/PTMn has two TM input pins, with the label STCK/PTCKn and STPI/PTPnI. One of the input pins, STCK/PTCKn, is essentially a clock source for the STM/PTMn and is selected using the STCK2~STCK0/PTnCK2~PTnCK0 bits in the STMC0/PTMnC0 register. This external TM input pin allows an external clock source to drive the internal TM. The STCK/PTCKn input pin can be chosen to have either a rising or falling active edge. The STCK/PTCKn pin is also used as the external trigger input pin in single pulse output mode.

The other STM/PTMn input pin, STPI/PTPnI, is the capture input whose active edge can be a rising edge, a falling edge or both rising and falling edges and the active edge transition type is selected using the STIO1~STIO0/PTnIO1~PTnIO0 bits in the STMC1/PTMnC1 register. For PTMn capture input mode there is another capture input, PTCKn, which can be used as the external trigger input source except the PTPnI pin.

The TMs each have one or more output pins. The STPB, PTP0B is the inverted signal of the STP, PTP0 output. The TM output pins can be selected using the corresponding pin-shared function selection bits described in the Pin-shared Function section. When the TM is in the Compare Match Output Mode, these pins can be controlled by the TM to switch to a high or low level or to toggle when a compare match situation occurs. The external output pins are also the pins where the TM generates the PWM output waveform. As the TM output pins are pin-shared with other functions, the TM output function must first be setup using relevant pin-shared function selection register.

	Standard Type TM	Periodic Type TMs		
	STM	PTM0	PTM1	PTM2
Input Pins	STCK, STPI,	PTCK0, PTP0I	PTCK1, PTP1I	PTCK2, PTP2I
Output Pins	STP, STPB	PTP0B, PTP0	PTP1	PTP2

TM External Pins

TM Input/Output Pin Control Register

Selecting to have a TM input/output or whether to retain its other shared function is implemented using the relevant pin-shared function selection registers, with the corresponding selection bits in each pin-shared function register corresponding to a TM input/output pin. Configuring the selection bits correctly will setup the corresponding pin as a TM input/output. The details of the pin-shared function selection are described in the pin-shared function section.
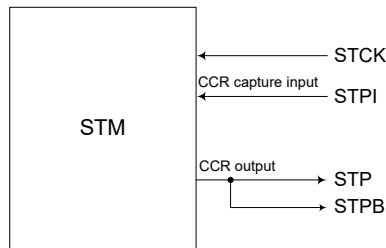
STM Function Pin Control Block Diagram
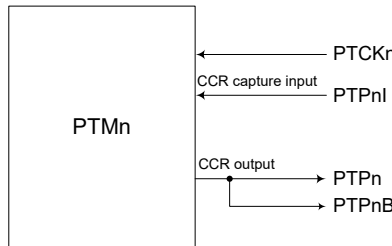
PTM Function Pin Control Block Diagram – n=0~2

Note: For the PTM1 and PTM2, there is not an external PTPnB pin

Programming Considerations

The TM Counter Registers and the Capture/Compare CCRA and CCRP registers, all have a low and high byte structure. The high bytes can be directly accessed, but as the low bytes can only be accessed via an internal 8-bit buffer, reading or writing to these register pairs must be carried out in a specific way. The important point to note is that data transfer to and from the 8-bit buffer and its related low byte only takes place when a write or read operation to its corresponding high byte is executed.

As the CCRA and CCRP registers are implemented in the way shown in the following diagram and accessing these register pairs is carried out in a specific way as described above, it is recommended to use the "MOV" instruction to access the CCRA and CCRP low byte registers, named STMAL, PTMnAL and PTMnRPL, using the following access procedures. Accessing the CCRA or CCRB low byte registers without following these access procedures will result in unpredictable values.
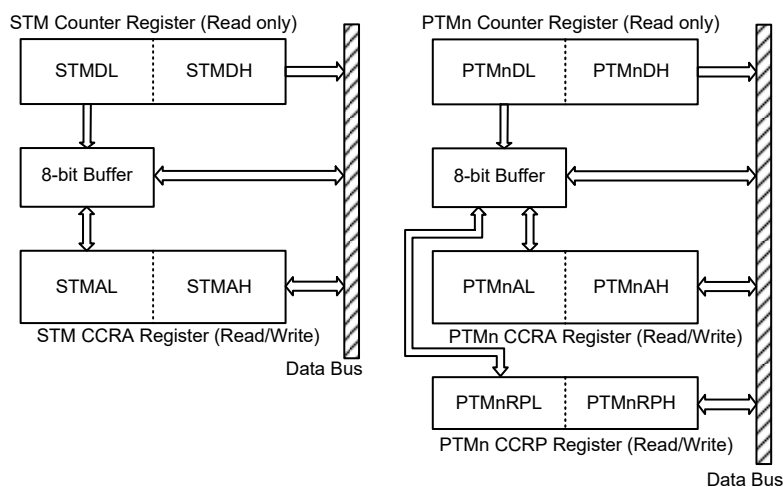
The following steps show the read and write procedures:

- Writing Data to CCRA or CCRP
  - Step 1. Write data to Low Byte STMAL, PTMnAL or PTMnRPL
    - note that here data is only written to the 8-bit buffer.
  - Step 2. Write data to High Byte STMAH, PTMnAH or PTMnRPH
    - here data is written directly to the high byte registers and simultaneously data is latched from the 8-bit buffer to the Low Byte registers.

- Reading Data from the Counter Registers and CCRA or CCRP
  - Step 1. Read data from the High Byte STMDH, PTMnDH, STMAH, PTMnAH or PTMnRPH
    - here data is read directly from the High Byte registers and simultaneously data is latched from the Low Byte register into the 8-bit buffer.
  - Step 2. Read data from the Low Byte STMDL, PTMnDL, STMAL, PTMnAL or PTMnRPL
    - this step reads data from the 8-bit buffer.

Standard Type TM – STM

The Standard Type TM contains five operating modes, which are Compare Match Output, Timer/ Event Counter, Capture Input, Single Pulse Output and PWM Output modes. The Standard TM can also be controlled with two external input pins and can drive two external output pins.
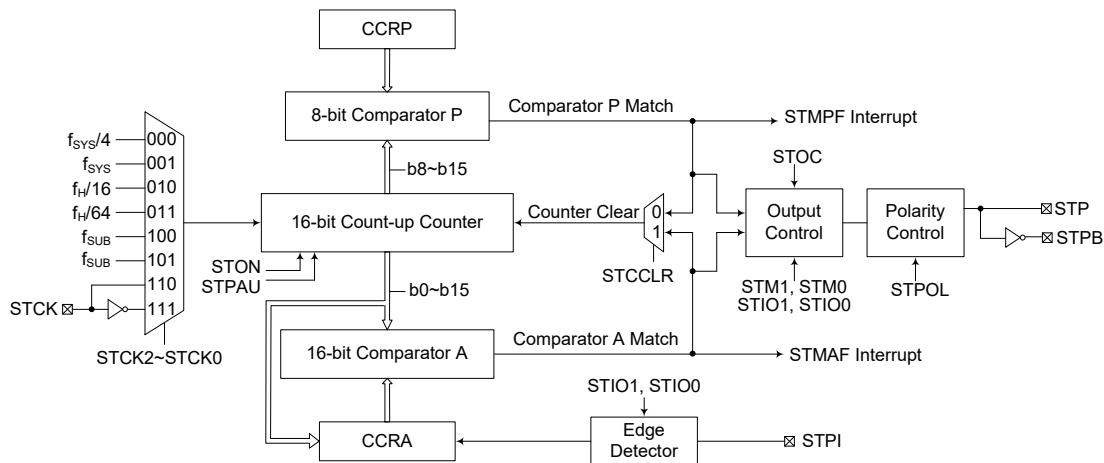
Note: The STM external pins are pin-shared with other functions and can input or output on different pins, so before using the STM function, the pin-shared function registers must be set properly.

Standard Type TM Block Diagram

Standard TM Operation

The size of Standard TM is 16-bit wide and its core is a 16-bit count-up counter which is driven by a user selectable internal or external clock source. There are also two internal comparators with the names, Comparator A and Comparator P. These comparators will compare the value in the counter with CCRP and CCRA registers. The CCRP comparator is 8-bit wide whose value is compared with the highest 8 bits in the counter while the CCRA is 16 bits and therefore compares all counter bits.

The only way of changing the value of the 16-bit counter using the application program, is to clear the counter by changing the STON bit from low to high. The counter will also be cleared automatically by a counter overflow or a compare match with one of its associated comparators. When these conditions occur, a STM interrupt signal will also usually be generated. The Standard Type TM can operate in a number of different operational modes, can be driven by different clock sources including an input pin and can also control two output pins. All operating setup conditions are selected using relevant internal registers.

Standard Type TM Register Description

Overall operation of the Standard TM is controlled using a series of registers. A read only register pair exists to store the internal counter 16-bit value, while a read/write register pair exists to store the internal 16-bit CCRA value. The STMRP register is used to store the 8-bit CCRP bits. The remaining two registers are control registers which setup the different operating and control modes.

Register	Bit							
Name	7	6	5	4	3	2	1	0
STMC0	STPAU	STCK2	STCK1	STCK0	STON	—	—	—
STMC1	STM1	STM0	STIO1	STIO0	STOC	STPOL	STDPX	STCCLR
STMDL	D7	D6	D5	D4	D3	D2	D1	D0
STMDH	D15	D14	D13	D12	D11	D10	D9	D8
STMAL	D7	D6	D5	D4	D3	D2	D1	D0
STMAH	D15	D14	D13	D12	D11	D10	D9	D8
STMRP	D7	D6	D5	D4	D3	D2	D1	D0

16-bit Standard TM Register List

- **STMC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	STPAU	STCK2	STCK1	STCK0	STON	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	—	—	—
POR	0	0	0	0	0	—	—	—

Bit 7   **STPAU**: STM Counter Pause Control

     0: Run

     1: Pause

The counter can be paused by setting this bit high. Clearing the bit to zero restores normal counter operation. When in a Pause condition the STM will remain powered up and continue to consume power. The counter will retain its residual value when this bit changes from low to high and resume counting from this value when the bit changes to a low value again.

Bit 6~4   **STCK2~STCK0**: Select STM Counter Clock

     000: $f_{SYS}/4$

     001: f_{SYS}

     010: $f_H/16$

     011: $f_H/64$

     100: f_{SUB}

     101: f_{SUB}

     110: STCK rising edge clock

     111: STCK falling edge clock

These three bits are used to select the clock source for the STM. The external pin clock source can be chosen to be active on the rising or falling edge. The clock source f_{SYS} is the system clock, while f_H and f_{SUB} are other internal clocks, the details of which can be found in the oscillator section.

Bit 3   **STON**: STM Counter On/Off Control

     0: Off

     1: On

This bit controls the overall on/off function of the STM. Setting the bit high enables the counter to run while clearing the bit disables the STM. Clearing this bit to zero will stop the counter from counting and turn off the STM which will reduce its power consumption. When the bit changes state from low to high the internal counter value will be reset to zero, however when the bit changes from high to low, the internal counter will retain its residual value until the bit returns high again. If the STM is in the Compare Match Output Mode then the STM output pin will be reset to its initial condition, as specified by the STOC bit, when the STON bit changes from low to high.

Bit 2~0   Unimplemented, read as "0"

- **STMC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	STM1	STM0	STIO1	STIO0	STOC	STPOL	STDPX	STCCLR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **STM1~STM0**: Select STM Operating Mode
         00: Compare Match Output Mode
         01: Capture Input Mode
         10: PWM Output Mode or Single Pulse Output Mode
         11: Timer/Counter Mode

         These bits setup the required operating mode for the STM. To ensure reliable operation the STM should be switched off before any changes are made to the STM1 and STM0 bits. In the Timer/Counter Mode, the STM output pin control will be disabled.

Bit 5~4   **STIO1~STIO0**: Select STM External Pin (STP or STPI) Function
         Compare Match Output Mode
         00: No change
         01: Output low
         10: Output high
         11: Toggle output
         PWM Output Mode/Single Pulse Output Mode
         00: PWM output inactive state
         01: PWM output active state
         10: PWM output
         11: Single Pulse Output
         Capture Input Mode
         00: Input capture at rising edge of STPI
         01: Input capture at falling edge of STPI
         10: Input capture at rising/falling edge of STPI
         11: Input capture disabled
         Timer/Counter Mode
         Unused

         These two bits are used to determine how the STM external pin changes state when a certain condition is reached. The function that these bits select depends upon in which mode the STM is running.

         In the Compare Match Output Mode, the STIO1 and STIO0 bits determine how the STM output pin changes state when a compare match occurs from the Comparator A. The TM output pin can be setup to switch high, switch low or to toggle its present state when a compare match occurs from the Comparator A. When the bits are both zero, then no change will take place on the output. The initial value of the STM output pin should be setup using the STOC bit in the STMC1 register. Note that the output level requested by the STIO1 and STIO0 bits must be different from the initial value setup using the STOC bit otherwise no change will occur on the STM output pin when a compare match occurs. After the STM output pin changes state, it can be reset to its initial level by changing the level of the STON bit from low to high.

         In the PWM Output Mode, the STIO1 and STIO0 bits determine how the STM output pin changes state when a certain compare match condition occurs. The PWM output function is modified by changing these two bits. It is necessary to only change the values of the STIO1 and STIO0 bits only after the STM has been switched off. Unpredictable PWM outputs will occur if the STIO1 and STIO0 bits are changed when the STM is running.

Bit 3   **STOC**: STM STP Output Control

Compare Match Output Mode
     0: Initial low
     1: Initial high

PWM Output Mode/Single Pulse Output Mode
     0: Active low
     1: Active high

This is the output control bit for the STM output pin. Its operation depends upon whether STM is being used in the Compare Match Output Mode or in the PWM Output Mode/Single Pulse Output Mode. It has no effect if the STM is in the Timer/Counter Mode. In the Compare Match Output Mode it determines the logic level of the STM output pin before a compare match occurs. In the PWM Output Mode/Single Pulse Output Mode it determines if the PWM signal is active high or active low.

Bit 2   **STPOL**: STM STP Output Polarity Control
     0: Non-inverted
     1: Inverted

This bit controls the polarity of the STP output pin. When the bit is set high the STM output pin will be inverted and not inverted when the bit is zero. It has no effect if the STM is in the Timer/Counter Mode.

Bit 1   **STDPX**: STM PWM Duty/Period Control
     0: CCRP – period; CCRA – duty
     1: CCRP – duty; CCRA – period

This bit determines which of the CCRA and CCRP registers are used for period and duty control of the PWM waveform.

Bit 0   **STCCLR**: STM Counter Clear Condition Selection
     0: Comparator P match
     1: Comparator A match

This bit is used to select the method which clears the counter. Remember that the Standard TM contains two comparators, Comparator A and Comparator P, either of which can be selected to clear the internal counter. With the STCCLR bit set high, the counter will be cleared when a compare match occurs from the Comparator A. When the bit is low, the counter will be cleared when a compare match occurs from the Comparator P or with a counter overflow. A counter overflow clearing method can only be implemented if the CCRP bits are all cleared to zero. The STCCLR bit is not used in the PWM Output, Single Pulse Output or Capture Input Mode.

- **STMDL Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R	R
POR	0	0	0	0	0	0	0	0

Bit 7~0   STM Counter Low Byte Register bit 7~bit 0
                STM 16-bit Counter bit 7~bit 0

- **STMDH Register**

Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R	R	R	R	R	R	R	R
POR	0	0	0	0	0	0	0	0

Bit 7~0   STM Counter High Byte Register bit 7~bit 0
                STM 16-bit Counter bit 15~bit 8

- **STMAL Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   STM CCRA Low Byte Register bit 7~bit 0

               STM 16-bit CCRA bit 7~bit 0

- **STMAH Register**

Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   STM CCRA High Byte Register bit 7~bit 0

               STM 16-bit CCRA bit 15~bit 8

- **STMRP Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   **D7~D0**: STM CCRP 8-bit Register, Compared with the STM Counter bit 15~bit 8

               Comparator P match period

                0: 65536 STM clocks

                1~255: (1~255) ×256 STM clocks

These eight bits are used to setup the value on the internal CCRP 8-bit register, which are then compared with the internal counter's highest eight bits. The result of this comparison can be selected to clear the internal counter if the STCCLR bit is set to zero. Setting the STCCLR bit to zero ensures that a compare match with the CCRP values will reset the internal counter. As the CCRP bits are only compared with the highest eight counter bits, the compare values exist in 256 clock cycle multiples. Clearing all eight bits to zero is in effect allowing the counter to overflow at its maximum value.

Standard Type TM Operation Modes

The Standard Type TM can operate in one of five operating modes, Compare Match Output Mode, PWM Output Mode, Single Pulse Output Mode, Capture Input Mode or Timer/Counter Mode. The operating mode is selected using the STM1 and STM0 bits in the STMC1 register.

Compare Match Output Mode

To select this mode, bits STM1 and STM0 in the STMC1 register, should be set to 00 respectively. In this mode once the counter is enabled and running it can be cleared by three methods. These are a counter overflow, a compare match from Comparator A and a compare match from Comparator P. When the STCCLR bit is low, there are two ways in which the counter can be cleared. One is when a compare match from Comparator P, the other is when the CCRP bits are all zero which allows the counter to overflow. Here both STMAF and STMPF interrupt request flags for Comparator A and Comparator P respectively, will both be generated.

If the STCCLR bit in the STMC1 register is high then the counter will be cleared when a compare match occurs from Comparator A. However, here only the STMAF interrupt request flag will be generated even if the value of the CCRP bits is less than that of the CCRA registers. Therefore when STCCLR is high no STMPF interrupt request flag will be generated. In the Compare Match Output Mode, the CCRA can not be set to "0".

As the name of the mode suggests, after a comparison is made, the STM output pin, will change state. The STM output pin condition however only changes state when a STMAF interrupt request flag is generated after a compare match occurs from Comparator A. The STMPF interrupt request flag, generated from a compare match occurs from Comparator P, will have no effect on the STM output pin. The way in which the STM output pin changes state are determined by the condition of the STIO1 and STIO0 bits in the STMC1 register. The STM output pin can be selected using the STIO1 and STIO0 bits to go high, to go low or to toggle from its present condition when a compare match occurs from Comparator A. The initial condition of the STM output pin, which is setup after the STON bit changes from low to high, is setup using the STOC bit. Note that if the STIO1 and STIO0 bits are zero then no pin change will take place.
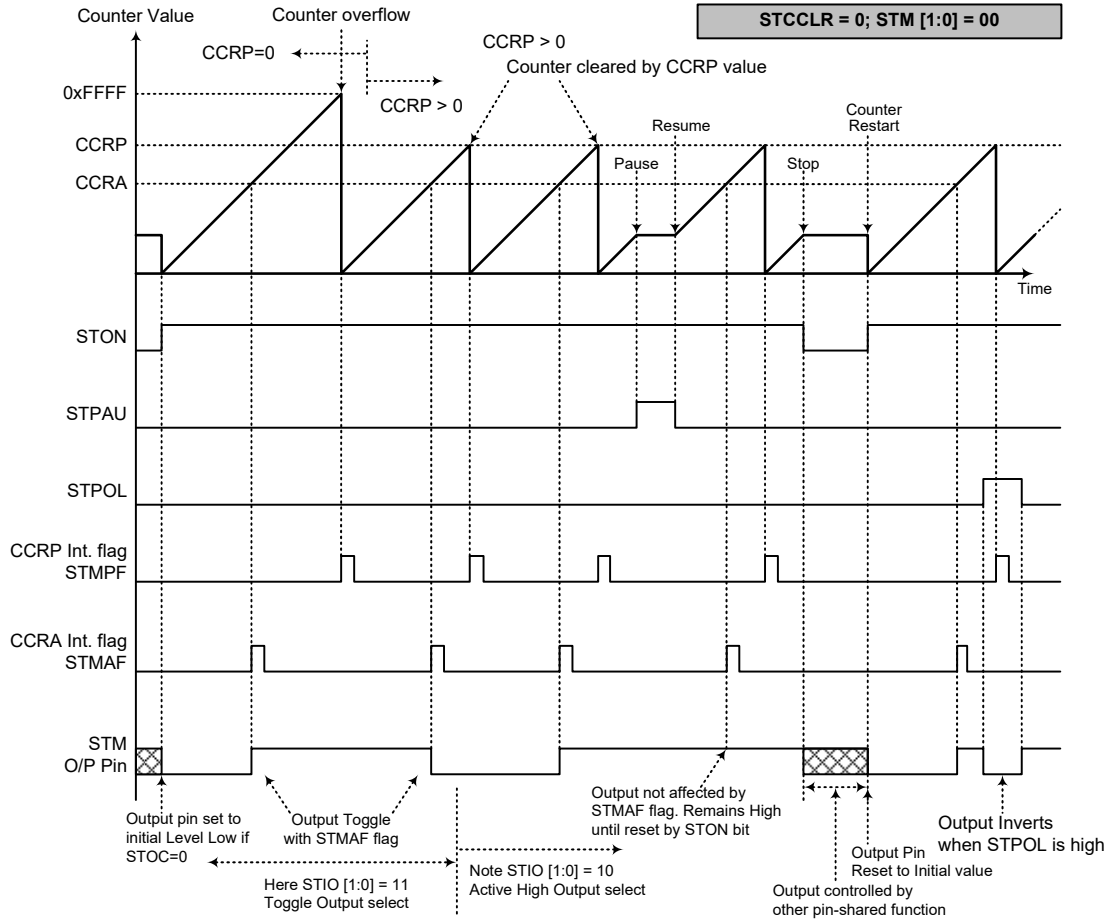
Compare Match Output Mode – STCCLR=0

Note: 1. With STCCLR=0 a Comparator P match will clear the counter
2. The STM output pin is controlled only by the STMAF flag
3. The output pin is reset to its initial state by a STON bit rising edge

| STCCLR = 1; STM [1:0] = 00 |
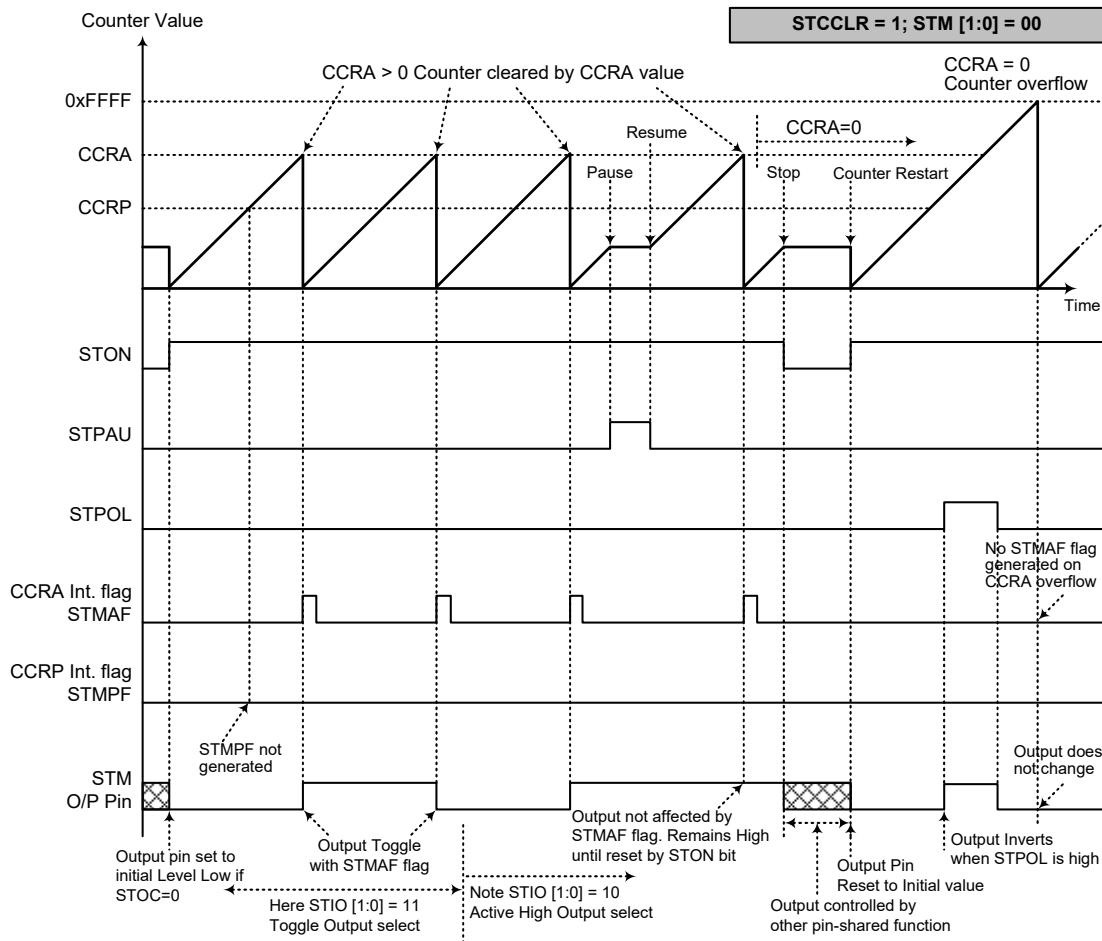
Compare Match Output Mode – STCCLR=1

Note: 1. With STCCLR=1 a Comparator A match will clear the counter

2. The STM output pin is controlled only by the STMAF flag

3. The output pin is reset to its initial state by a STON bit rising edge

4. A STMPF flag is not generated when STCCLR=1

Timer/Counter Mode

To select this mode, bits STM1 and STM0 in the STMC1 register should be set to 11 respectively. The Timer/Counter Mode operates in an identical way to the Compare Match Output Mode generating the same interrupt flags. The exception is that in the Timer/Counter Mode the STM output pin is not used. Therefore the above description and Timing Diagrams for the Compare Match Output Mode can be used to understand its function. As the STM output pin is not used in this mode, the pin can be used as a normal I/O pin or other pin-shared function.

PWM Output Mode

To select this mode, bits STM1 and STM0 in the STMC1 register should be set to 10 respectively and also the STIO1 and STIO0 bits should be set to 10 respectively. The PWM function within the STM is useful for applications which require functions such as motor control, heating control, illumination control etc. By providing a signal of fixed frequency but of varying duty cycle on the STM output pin, a square wave AC waveform can be generated with varying equivalent DC RMS values.

As both the period and duty cycle of the PWM waveform can be controlled, the choice of generated waveform is extremely flexible. In the PWM Output mode, the STCCLR bit has no effect as the PWM period. Both of the CCRA and CCRP registers are used to generate the PWM waveform, one register is used to clear the internal counter and thus control the PWM waveform frequency, while the other one is used to control the duty cycle. Which register is used to control either frequency or duty cycle is determined using the STDPX bit in the STMC1 register. The PWM waveform frequency and duty cycle can therefore be controlled by the values in the CCRA and CCRP registers.

An interrupt flag, one for each of the CCRA and CCRP, will be generated when a compare match occurs from either Comparator A or Comparator P. The STOC bit in the STMC1 register is used to select the required polarity of the PWM waveform while the two STIO1 and STIO0 bits are used to enable the PWM output or to force the STM output pin to a fixed high or low level. The STPOL bit is used to reverse the polarity of the PWM output waveform.

- **16-bit STM, PWM Output Mode, Edge-aligned Mode, STDPX=0**

CCRP	1~255	0
Period	CCRP×256	65536
Duty	CCRA	

If f_{SYS}=16MHz, TM clock source is f_{SYS}/4, CCRP=2 and CCRA=128,

The STM PWM output frequency=(f_{SYS}/4)/(2×256)=f_{SYS}/2048=7.8125kHz, duty=128/(2×256)=25%.

If the Duty value defined by the CCRA register is equal to or greater than the Period value, then the PWM output duty is 100%.

- **16-bit STM, PWM Output Mode, Edge-aligned Mode, STDPX=1**

CCRP	1~255	0
Period	CCRA	
Duty	CCRP×256	65536

The PWM output period is determined by the CCRA register value together with the TM clock while the PWM duty cycle is defined by the CCRP register value except when the CCRP value is equal to 0.
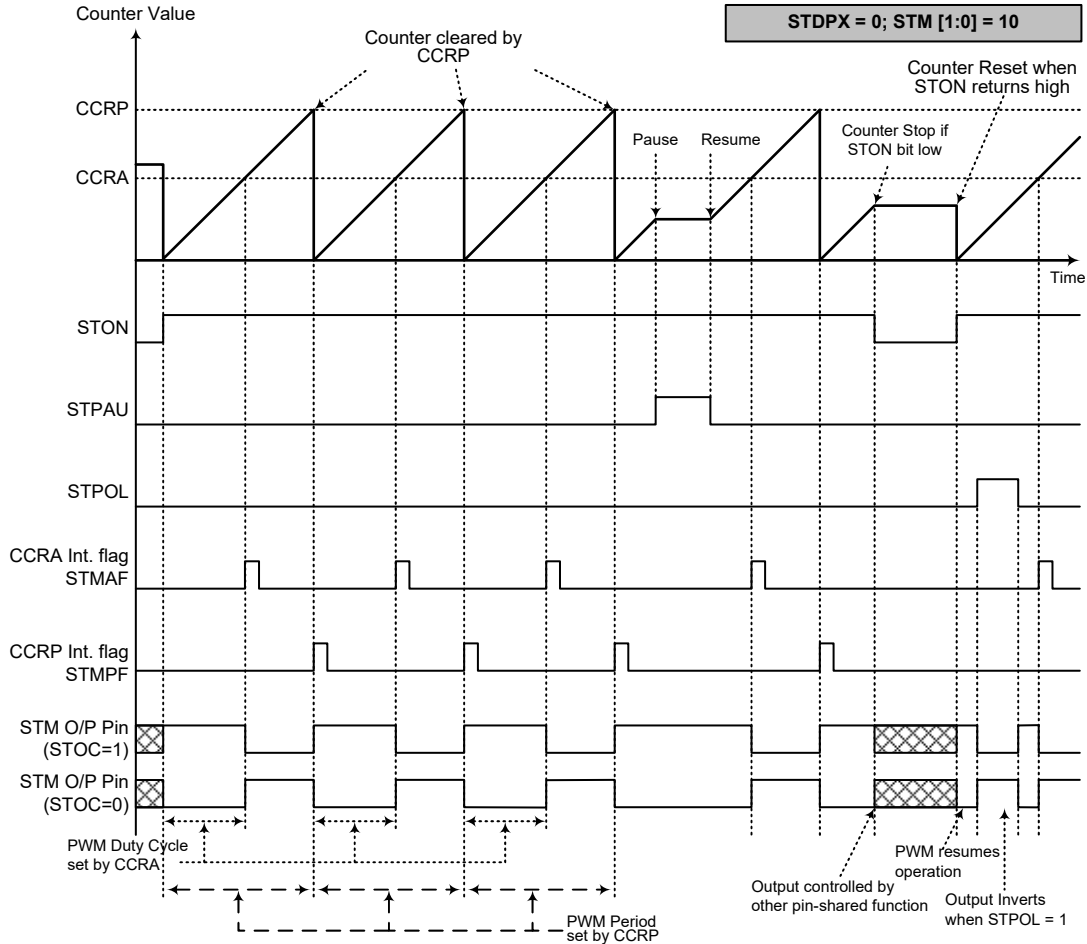
PWM Output Mode – STDPX=0

Note: 1. Here STDPX=0 – Counter cleared by CCRP

2. A counter clear sets the PWM Period

3. The internal PWM function continues running even when STIO [1:0]=00 or 01

4. The STCCLR bit has no influence on PWM operation

PWM Output Mode – STDPX=1
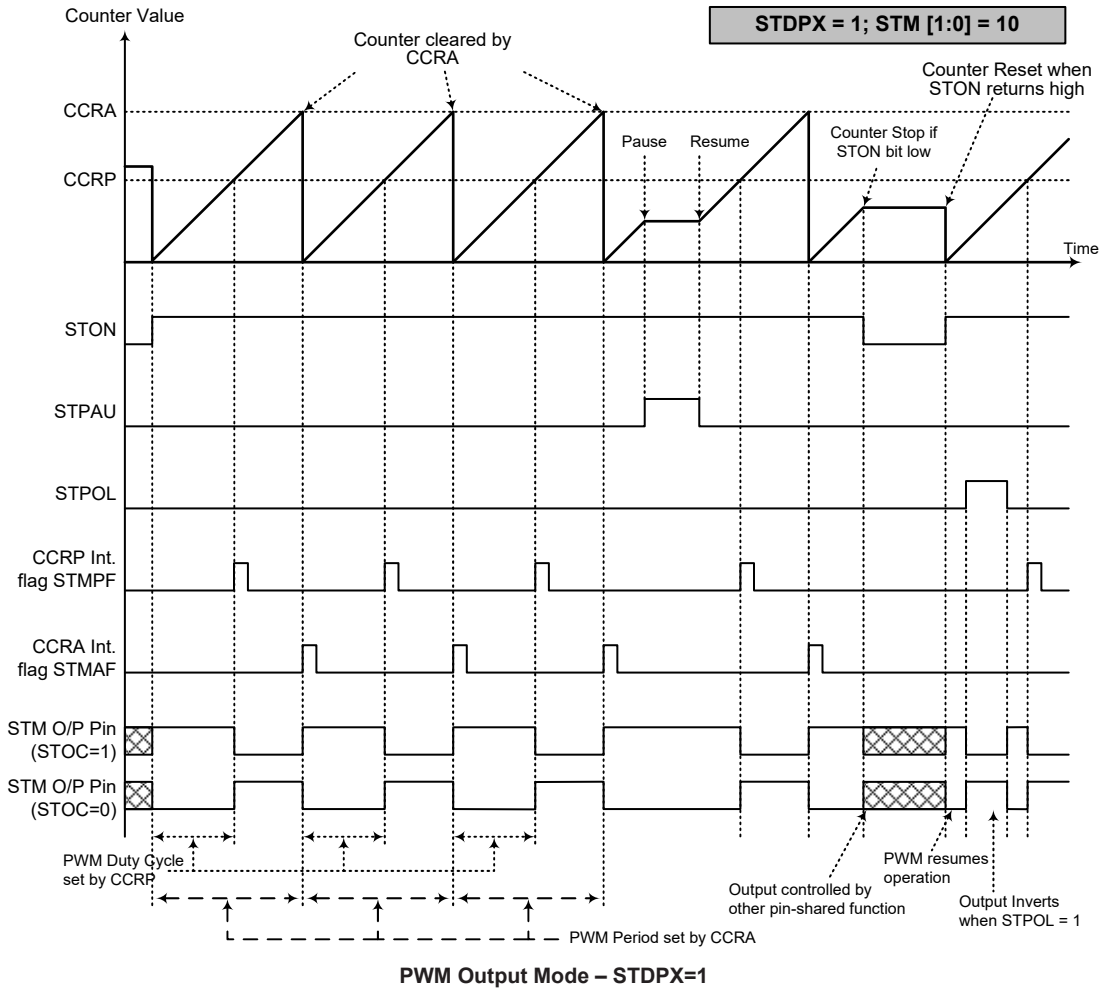
Note: 1. Here STDPX=1 – Counter cleared by CCRA

2. A counter clear sets the PWM Period

3. The internal PWM function continues even when STIO [1:0]=00 or 01

4. The STCCLR bit has no influence on PWM operation

Single Pulse Output Mode

To select this mode, bits STM1 and STM0 in the STMC1 register should be set to 10 respectively and also the STIO1 and STIO0 bits should be set to 11 respectively. The Single Pulse Output Mode, as the name suggests, will generate a single shot pulse on the STM output pin.

The trigger for the pulse output leading edge is a low to high transition of the STON bit, which can be implemented using the application program. However in the Single Pulse Mode, the STON bit can also be made to automatically change from low to high using the external STCK pin, which will in turn initiate the Single Pulse output. When the STON bit transitions to a high level, the counter will start running and the pulse leading edge will be generated. The STON bit should remain high when the pulse is in its active state. The generated pulse trailing edge will be generated when the STON bit is cleared to zero, which can be implemented using the application program or when a compare match occurs from Comparator A.

However a compare match from Comparator A will also automatically clear the STON bit and thus generate the Single Pulse output trailing edge. In this way the CCRA value can be used to control the pulse width. A compare match from Comparator A will also generate a STM interrupt. The counter can only be reset back to zero when the STON bit changes from low to high when the counter restarts. In the Single Pulse Mode CCRP is not used. The STCCLR and STDPX bits are not used in this Mode.

Single Pulse Generation
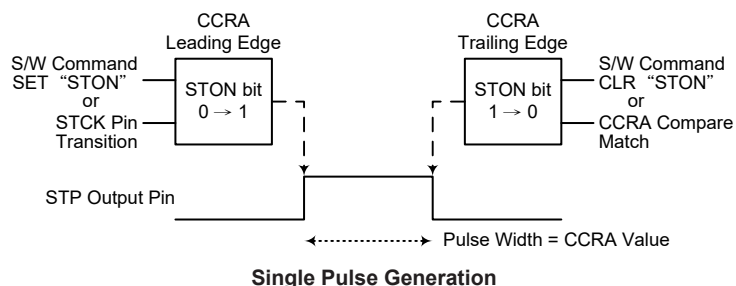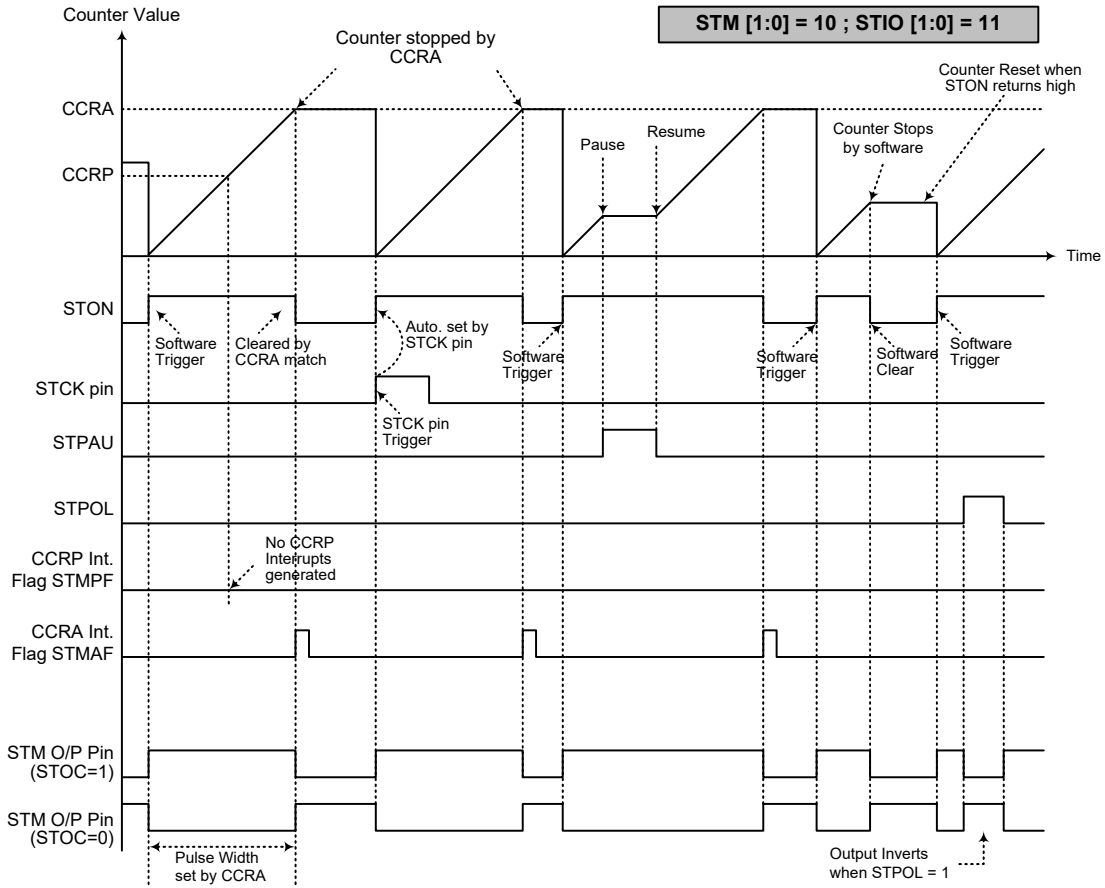
Single Pulse Mode

Note: 1. Counter stopped by CCRA

2. CCRP is not used

3. The pulse triggered by the STCK pin or by setting the STON bit high

4. A STCK pin active edge will automatically set the STON bit high.

5. In the Single Pulse Mode, STIO [1:0] must be set to "11" and can not be changed.

Capture Input Mode

To select this mode bits STM1 and STM0 in the STMC1 register should be set to 01 respectively. This mode enables external signals to capture and store the present value of the internal counter and can therefore be used for applications such as pulse width measurements. The external signal is supplied on the STPI pin, whose active edge can be a rising edge, a falling edge or both rising and falling edges; the active edge transition type is selected using the STIO1 and STIO0 bits in the STMC1 register. The counter is started when the STON bit changes from low to high which is initiated using the application program.

When the required edge transition appears on the STPI pin the present value in the counter will be latched into the CCRA registers and a STM interrupt generated. Irrespective of what events occur on the STPI pin the counter will continue to free run until the STON bit changes from high to low. When a CCRP compare match occurs the counter will reset back to zero; in this way the CCRP value can be used to control the maximum counter value. When a CCRP compare match occurs from Comparator P, a STM interrupt will also be generated. Counting the number of overflow interrupt signals from the CCRP can be a useful method in measuring long pulse widths. The STIO1 and STIO0 bits can select the active trigger edge on the STPI pin to be a rising edge, falling edge or both edge types. If the STIO1 and STIO0 bits are both set high, then no capture operation will take place irrespective of what happens on the STPI pin, however it must be noted that the counter will continue to run. The STCCLR and STDPX bits are not used in this Mode.
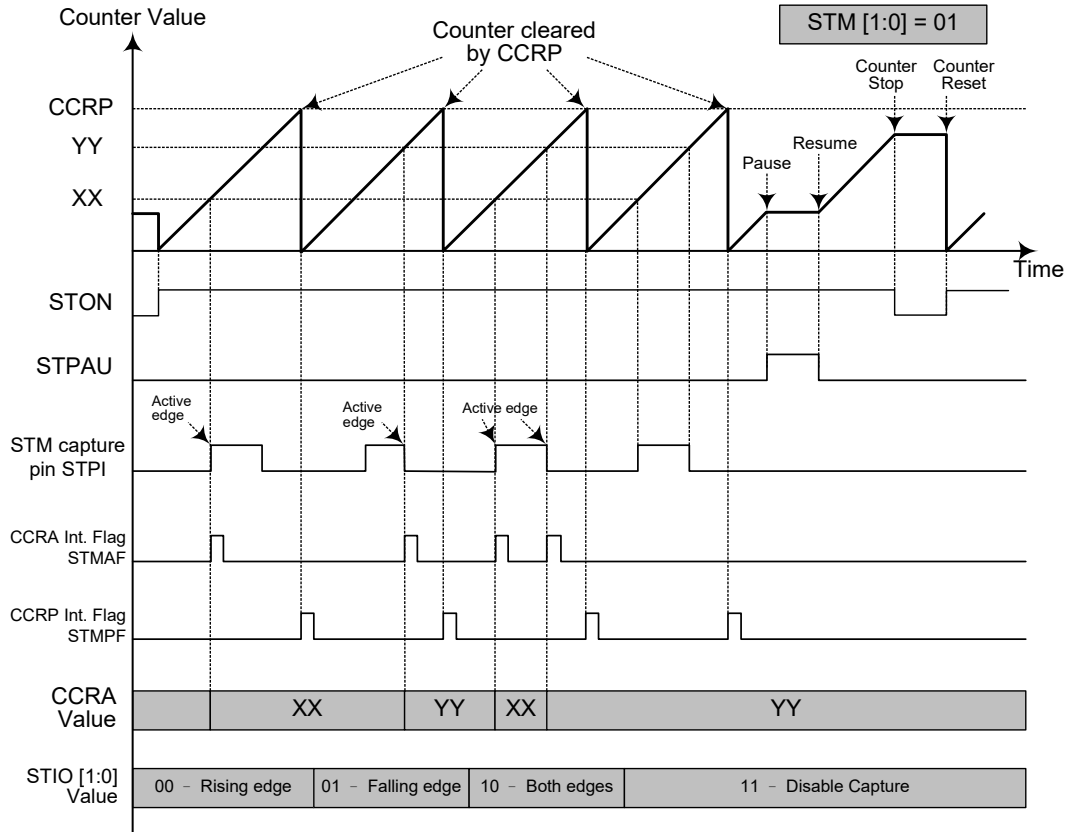
Capture Input Mode

Note: 1. STM [1:0]=01 and active edge set by the STIO [1:0] bits

2. A STM Capture input pin active edge transfers the counter value to CCRA

3. STCCLR bit not used

4. No output function – STOC and STPOL bits are not used

5. CCRP determines the counter value and the counter has a maximum count value when CCRP is equal to zero.

Periodic Type TM – PTM

The Periodic Type TM contains five operating modes, which are Compare Match Output, Timer/Event Counter, Capture Input, Single Pulse Output and PWM Output modes. The Periodic TM can be controlled with two external input pins and can drive some external output pins.
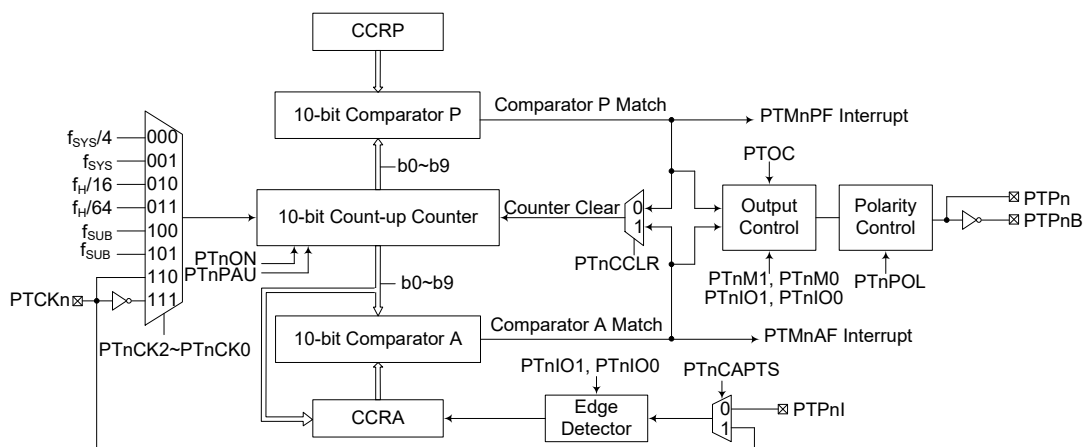
Note: 1. The PTMn external pins are pin-shared with other functions and can input or output on different pins, so before using the PTMn function, the pin-shared function registers must be set properly.

2. For the PTM0, the PTP0I input can be from external pin or the internal OVP output signal selected by PTP0IPS bit.

3. For the PTM1 and PTM2, there is not an external PTPnB pin

Periodic Type TM Block Diagram (n=0, 1 or 2)

Periodic TM Operation

The Periodic Type TM core is a 10-bit count-up counter which is driven by a user selectable internal or external clock source. There are also two internal comparators with the names, Comparator A and Comparator P. These comparators will compare the value in the counter with CCRP and CCRA registers. The CCRP comparator is 10-bit wide.

The only way of changing the value of the 10-bit counter using the application program, is to clear the counter by changing the PTnON bit from low to high. The counter will also be cleared automatically by a counter overflow or a compare match with one of its associated comparators. When these conditions occur, a PTMn interrupt signal will also usually be generated. The Periodic Type TM can operate in a number of different operational modes, can be driven by different clock sources including an input pin and can also control more than one output pin. All operating setup conditions are selected using relevant internal registers.

Periodic Type TM Register Description

Overall operation of the Periodic Type TM is controlled using a series of registers. A read only register pair exists to store the internal counter 10-bit value, while two read/write register pairs exist to store the internal 10-bit CCRA and CCRP value. The remaining two registers are control registers which setup the different operating and control modes.

Register Name	Bit							
	7	6	5	4	3	2	1	0
PTMnC0	PTnPAU	PTnCK2	PTnCK1	PTnCK0	PTnON	—	—	—
PTMnC1	PTnM1	PTnM0	PTnIO1	PTnIO0	PTnOC	PTnPOL	PTnCAPTS	PTnCCLR
PTMnDL	D7	D6	D5	D4	D3	D2	D1	D0
PTMnDH	—	—	—	—	—	—	D9	D8
PTMnAL	D7	D6	D5	D4	D3	D2	D1	D0
PTMnAH	—	—	—	—	—	—	D9	D8
PTMnRPL	D7	D6	D5	D4	D3	D2	D1	D0
PTMnRPH	—	—	—	—	—	—	D9	D8

10-bit Periodic TM Register List (n=0, 1 or 2)

- **PTMnC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	PTnPAU	PTnCK2	PTnCK1	PTnCK0	PTnON	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	—	—	—
POR	0	0	0	0	0	—	—	—

Bit 7 **PTnPAU**: PTMn Counter Pause Control

0: Run

1: Pause

The counter can be paused by setting this bit high. Clearing the bit to zero restores normal counter operation. When in a Pause condition the PTMn will remain powered up and continue to consume power. The counter will retain its residual value when this bit changes from low to high and resume counting from this value when the bit changes to a low value again.

Bit 6~4 **PTnCK2~PTnCK0**: Select PTMn Counter Clock

000: $f_{SYS}/4$

001: f_{SYS}

010: $f_H/16$

011: $f_H/64$

100: f_{SUB}

101: f_{SUB}

110: PTCKn rising edge clock

111: PTCKn falling edge clock

These three bits are used to select the clock source for the PTMn. The external pin clock source can be chosen to be active on the rising or falling edge. The clock source f_{SYS} is the system clock, while f_H and f_{SUB} are other internal clocks, the details of which can be found in the oscillator section.

Bit 3 **PTnON**: PTMn Counter On/Off Control

0: Off

1: On

This bit controls the overall on/off function of the PTMn. Setting the bit high enables the counter to run, clearing the bit disables the PTMn. Clearing this bit to zero will stop the counter from counting and turn off the PTMn which will reduce its power consumption. When the bit changes state from low to high the internal counter value will be reset to zero, however when the bit changes from high to low, the internal counter will retain its residual value until the bit returns high again.

If the PTMn is in the Compare Match Output Mode, PWM output Mode or Single Pulse Output Mode then the PTMn output pin will be reset to its initial condition, as specified by the PTnOC bit, when the PTnON bit changes from low to high.

Bit 2~0 Unimplemented, read as "0"

- **PTMnC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	PTnM1	PTnM0	PTnIO1	PTnIO0	PTnOC	PTnPOL	PTnCAPTS	PTnCCLR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6 **PTnM1~PTnM0**: Select PTMn Operating Mode

00: Compare Match Output Mode
01: Capture Input Mode
10: PWM Output Mode or Single Pulse Output Mode
11: Timer/Counter Mode

These bits setup the required operating mode for the PTMn. To ensure reliable operation the PTMn should be switched off before any changes are made to the PTnM1 and PTnM0 bits. In the Timer/Counter Mode, the PTMn output pin control must be disabled.

Bit 5~4 **PTnIO1~PTnIO0**: Select PTMn External Pin Function

Compare Match Output Mode
00: No change
01: Output low
10: Output high
11: Toggle output

PWM Output Mode/Single Pulse Output Mode
00: PWM Output inactive state
01: PWM Output active state
10: PWM output
11: Single pulse output

Capture Input Mode
00: Input capture at rising edge of PTPnI or PTCKn
01: Input capture at falling edge of PTPnI or PTCKn
10: Input capture at falling/rising edge of PTPnI or PTCKn
11: Input capture disabled

Timer/Counter Mode
Unused

These two bits are used to determine how the PTMn external pin changes state when a certain condition is reached. The function that these bits select depends upon in which mode the PTMn is running.

In the Compare Match Output Mode, the PTnIO1 and PTnIO0 bits determine how the PTMn output pin changes state when a compare match occurs from the Comparator A. The PTMn output pin can be setup to switch high, switch low or to toggle its present state when a compare match occurs from the Comparator A. When the bits are both zero, then no change will take place on the output. The initial value of the PTMn output pin should be setup using the PTnOC bit in the PTMnC1 register. Note that the output level requested by the PTnIO1 and PTnIO0 bits must be different from the initial value setup using the PTnOC bit otherwise no change will occur on the PTMn output pin when a compare match occurs. After the PTMn output pin changes state, it can be reset to its initial level by changing the level of the PTnON bit from low to high.

In the PWM Output Mode, the PTnIO1 and PTnIO0 bits determine how the PTMn output pin changes state when a certain compare match condition occurs. The PWM output function is modified by changing these two bits. It is necessary to only change the values of the PTnIO1 and PTnIO0 bits only after the TM has been switched off. Unpredictable PWM outputs will occur if the PTnIO1 and PTnIO0 bits are changed when the PTMn is running.

Bit 3   **PTnOC**: PTMn PTPn Output Control bit

Compare Match Output Mode
    0: Initial low
    1: Initial high

PWM Output Mode/Single Pulse Output Mode
    0: Active low
    1: Active high

This is the output control bit for the PTMn output pin. Its operation depends upon whether PTMn is being used in the Compare Match Output Mode or in the PWM Output Mode/Single Pulse Output Mode. It has no effect if the PTMn is in the Timer/Counter Mode. In the Compare Match Output Mode it determines the logic level of the PTMn output pin before a compare match occurs. In the PWM Output Mode it determines if the PWM signal is active high or active low.

Bit 2   **PTnPOL**: PTMn PTPn Output Polarity Control
    0: Non-invert
    1: Invert

This bit controls the polarity of the PTPn output pin. When the bit is set high the PTMn output pin will be inverted and not inverted when the bit is zero. It has no effect if the PTMn is in the Timer/Counter Mode.

Bit 1   **PTnCAPTS**: PTMn Capture Trigger Source Selection
    0: From PTPnI pin
    1: From PTCKn pin

Bit 0   **PTnCCLR**: Select PTMn Counter Clear Condition
    0: Comparator P match
    1: Comparator A match

This bit is used to select the method which clears the counter. Remember that the Periodic TM contains two comparators, Comparator A and Comparator P, either of which can be selected to clear the internal counter. With the PTnCCLR bit set high, the counter will be cleared when a compare match occurs from the Comparator A. When the bit is low, the counter will be cleared when a compare match occurs from the Comparator P or with a counter overflow. A counter overflow clearing method can only be implemented if the CCRP bits are all cleared to zero. The PTnCCLR bit is not used in the PWM Output Mode, Single Pulse or Capture Input Mode.

• **PTMnDL Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R	R
POR	0	0	0	0	0	0	0	0

Bit 7~0   **D7~D0**: PTMn Counter Low Byte Register bit 7~bit 0

PTMn 10-bit Counter bit 7~bit 0

• **PTMnDH Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	D9	D8
R/W	—	—	—	—	—	—	R	R
POR	—	—	—	—	—	—	0	0

Bit 7~2   Unimplemented, read as "0"

Bit 1~0   **D9~D8**: PTMn Counter High Byte Register bit 1~bit 0

PTMn 10-bit Counter bit 9~bit 8

- **PTMnAL Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   **D7~D0**: PTMn CCRA Low Byte Register bit 7~bit 0
PTMn 10-bit CCRA bit 7~bit 0

- **PTMnAH Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	D9	D8
R/W	—	—	—	—	—	—	R/W	R/W
POR	—	—	—	—	—	—	0	0

Bit 7~2   Unimplemented, read as "0"

Bit 1~0   **D9~D8**: PTMn CCRA High Byte Register bit 1~bit 0
PTMn 10-bit CCRA bit 9~bit 8

- **PTMnRPL Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   **D7~D0**: PTMn CCRP Low Byte Register bit 7~bit 0
PTMn 10-bit CCRP bit 7~bit 0

- **PTMnRPH Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	D9	D8
R/W	—	—	—	—	—	—	R/W	R/W
POR	—	—	—	—	—	—	0	0

Bit 7~2   Unimplemented, read as "0"

Bit 1~0   **D9~D8**: PTMn CCRP High Byte Register bit 1~bit 0
PTMn 10-bit CCRP bit 9~bit 8

Periodic Type TM Operating Modes

The Periodic Type TM can operate in one of five operating modes, Compare Match Output Mode, PWM Output Mode, Single Pulse Output Mode, Capture Input Mode or Timer/Counter Mode. The operating mode is selected using the PTnM1 and PTnM0 bits in the PTMnC1 register.

Compare Output Mode

To select this mode, bits PTnM1 and PTnM0 in the PTMnC1 register, should be set to 00 respectively. In this mode once the counter is enabled and running it can be cleared by three methods. These are a counter overflow, a compare match from Comparator A and a compare match from Comparator P. When the PTnCCLR bit is low, there are two ways in which the counter can be cleared. One is when a compare match from Comparator P, the other is when the CCRP bits are all zero which allows the counter to overflow. Here both PTMnAF and PTMnPF interrupt request flags for Comparator A and Comparator P respectively, will both be generated.

If the PTnCCLR bit in the PTMnC1 register is high then the counter will be cleared when a compare match occurs from Comparator A. However, here only the PTMnAF interrupt request flag will be generated even if the value of the CCRP bits is less than that of the CCRA registers. Therefore when PTnCCLR is high no PTMnPF interrupt request flag will be generated. In the Compare Match Output Mode, the CCRA can not be cleared to zero.

If the CCRA bits are all zero, the counter will overflow when its reaches its maximum 10-bit, 3FF Hex, value, however here the PTMnAF interrupt request flag will not be generated.

As the name of the mode suggests, after a comparison is made, the PTMn output pin, will change state. The PTMn output pin condition however only changes state when a PTMnAF interrupt request flag is generated after a compare match occurs from Comparator A. The PTMnPF interrupt request flag, generated from a compare match occurs from Comparator P, will have no effect on the PTMn output pin. The way in which the PTMn output pin changes state are determined by the condition of the PTnIO1 and PTnIO0 bits in the PTMnC1 register. The PTMn output pin can be selected using the PTnIO1 and PTnIO0 bits to go high, to go low or to toggle from its present condition when a compare match occurs from Comparator A. The initial condition of the PTMn output pin, which is setup after the PTnON bit changes from low to high, is setup using the PTnOC bit. Note that if the PTnIO1 and PTnIO0 bits are zero then no pin change will take place.
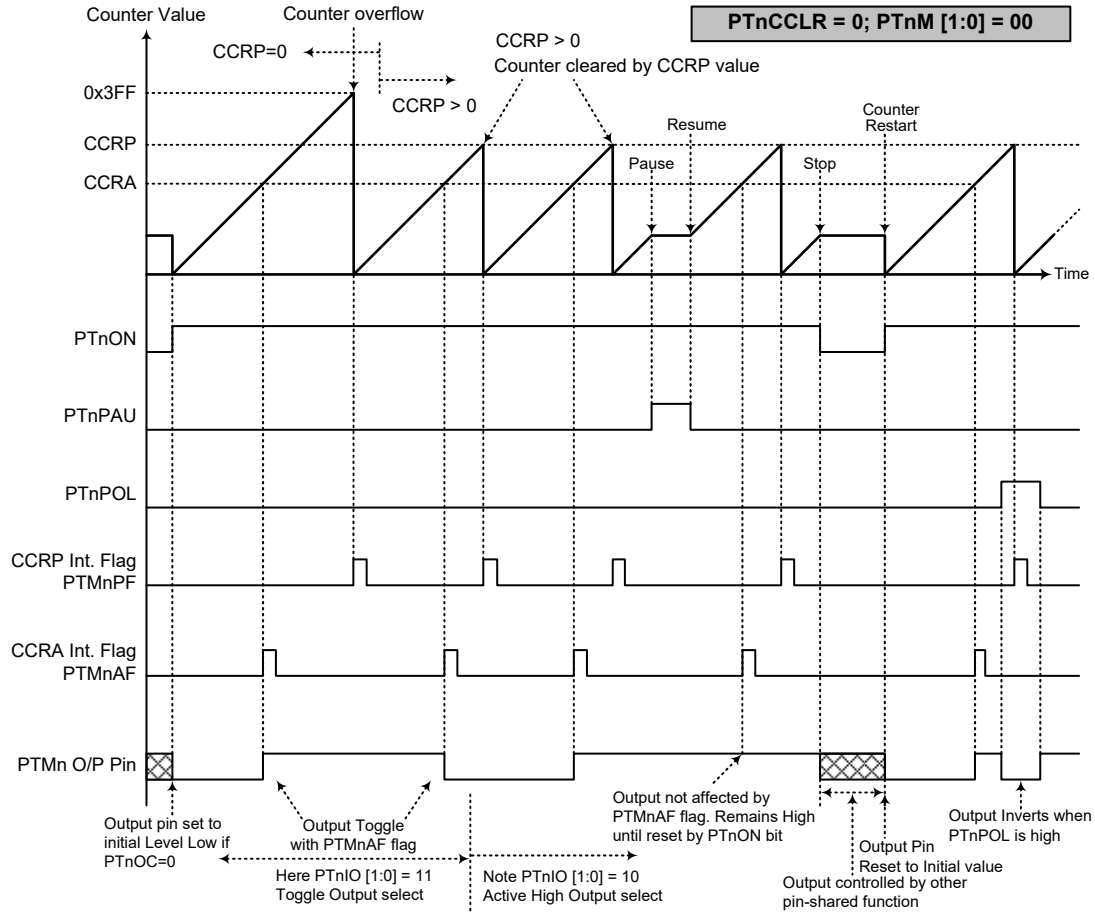
Compare Match Output Mode – PTnCCLR=0 (n=0, 1 or 2)

Note: 1. With PTnCCLR=0 a Comparator P match will clear the counter

2. The PTMn output pin is controlled only by the PTMnAF flag

3. The output pin is reset to its initial state by a PTnON bit rising edge
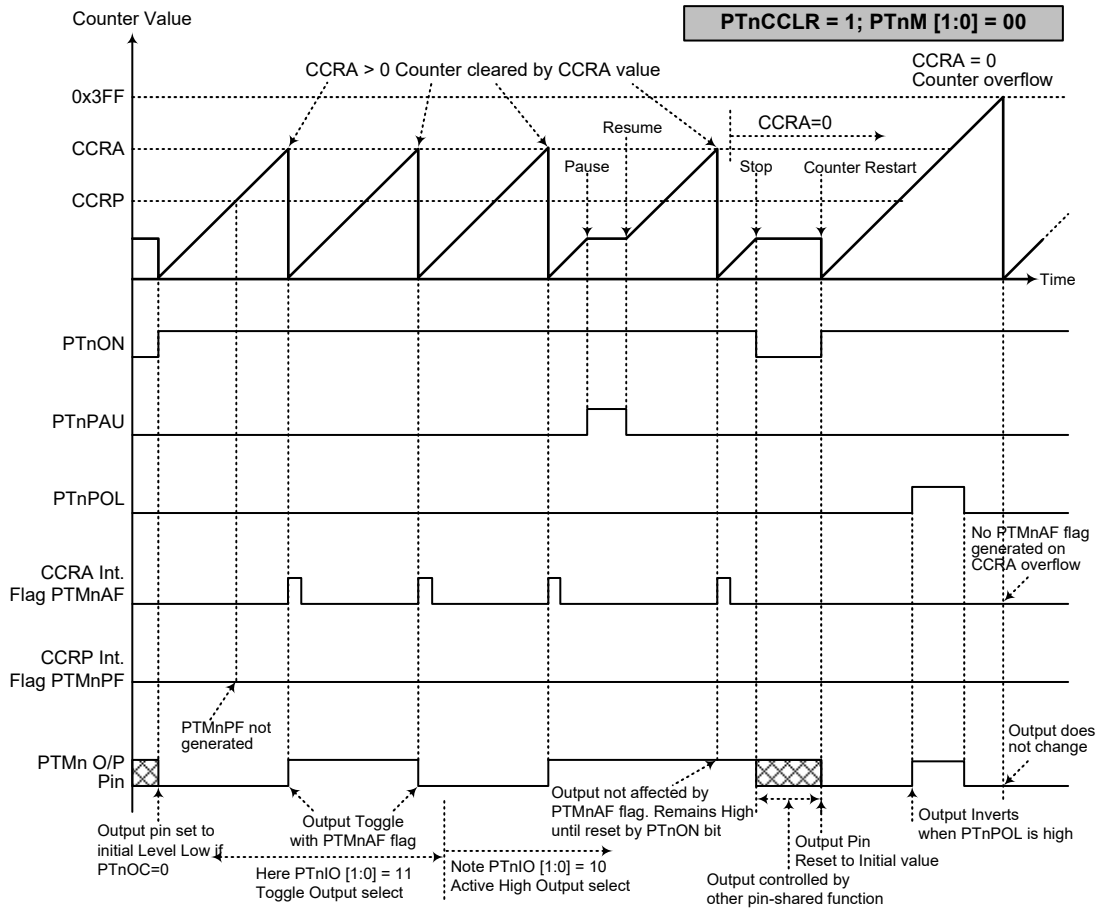
Compare Match Output Mode – PTnCCLR=1 (n=0, 1 or 2)

Note: 1. With PTnCCLR=1 a Comparator A match will clear the counter

2. The PTMn output pin is controlled only by the PTMnAF flag

3. The output pin is reset to its initial state by a PTnON bit rising edge

4. A PTMnPF flag is not generated when PTnCCLR=1

Timer/Counter Mode

To select this mode, bits PTnM1 and PTnM0 in the PTMnC1 register should be set to 11 respectively. The Timer/Counter Mode operates in an identical way to the Compare Match Output Mode generating the same interrupt flags. The exception is that in the Timer/Counter Mode the PTMn output pin is not used. Therefore the above description and Timing Diagrams for the Compare Match Output Mode can be used to understand its function. As the PTMn output pin is not used in this mode, the pin can be used as a normal I/O pin or other pin-shared function.

PWM Output Mode

To select this mode, bits PTnM1 and PTnM0 in the PTMnC1 register should be set to 10 respectively. The PWM function within the PTMn is useful for applications which require functions such as motor control, heating control, illumination control etc. By providing a signal of fixed frequency but of varying duty cycle on the PTMn output pin, a square wave AC waveform can be generated with varying equivalent DC RMS values.

As both the period and duty cycle of the PWM waveform can be controlled, the choice of generated waveform is extremely flexible. In the PWM Output Mode, the PTnCCLR bit has no effect on the PWM operation. Both of the CCRA and CCRP registers are used to generate the PWM waveform, one register is used to clear the internal counter and thus control the PWM waveform frequency, while the other one is used to control the duty cycle. The PWM waveform frequency and duty cycle can therefore be controlled by the values in the CCRA and CCRP registers.

An interrupt flag, one for each of the CCRA and CCRP, will be generated when a compare match occurs from either Comparator A or Comparator P. The PTnOC bit in the PTMnC1 register is used to select the required polarity of the PWM waveform while the two PTnIO1 and PTnIO0 bits are used to enable the PWM output or to force the PTMn output pin to a fixed high or low level. The PTnPOL bit is used to reverse the polarity of the PWM output waveform.

- **10-bit PTMn, PWM Output Mode, Edge-aligned Mode**

CCRP	1~1023	0
Period	1~1023	1024
Duty	CCRA	

If f_{SYS}=12MHz, PTMn clock source select f_{SYS}/4, CCRP=512 and CCRA=128,

The PTMn PWM output frequency=(f_{SYS}/4)/512=f_{SYS}/2048=5.8594kHz, duty=128/512= 25%.

If the Duty value defined by the CCRA register is equal to or greater than the Period value, then the PWM output duty is 100%.
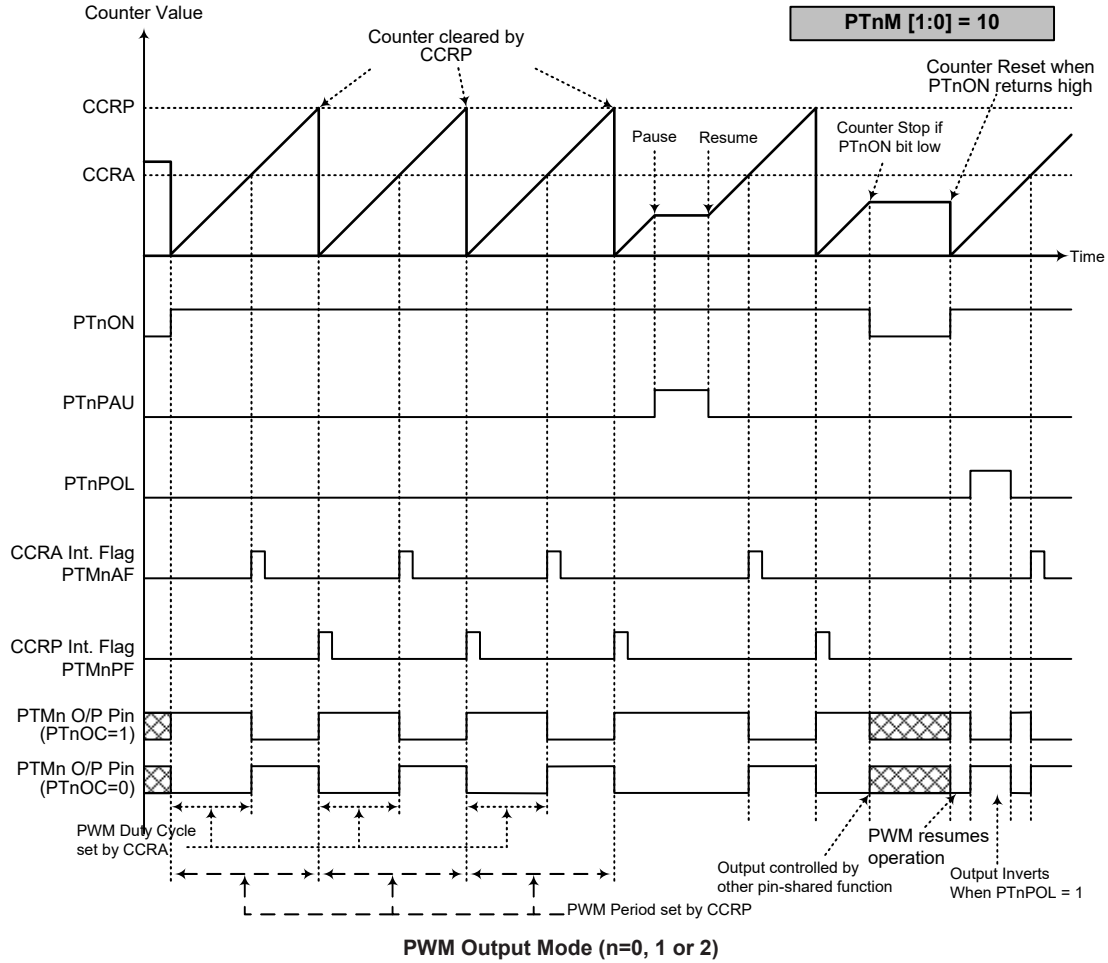
PWM Output Mode (n=0, 1 or 2)

Note: 1. Counter cleared by CCRP

2. A counter clear sets the PWM Period

3. The internal PWM function continues running even when PTnIO[1:0]=00 or 01

4. The PTnCCLR bit has no influence on PWM operation

Single Pulse Mode

To select this mode, bits PTnM1 and PTnM0 in the PTMnC1 register should be set to 10 respectively and also the PTnIO1 and PTnIO0 bits should be set to 11 respectively. The Single Pulse Output Mode, as the name suggests, will generate a single shot pulse on the PTMn output pin.

The trigger for the pulse output leading edge is a low to high transition of the PTnON bit, which can be implemented using the application program. However in the Single Pulse Mode, the PTnON bit can also be made to automatically change from low to high using the external PTCKn pin, which will in turn initiate the Single Pulse output. When the PTnON bit transitions to a high level, the counter will start running and the pulse leading edge will be generated. The PTnON bit should remain high when the pulse is in its active state. The generated pulse trailing edge will be generated when the PTnON bit is cleared to zero, which can be implemented using the application program or when a compare match occurs from Comparator A.

However a compare match from Comparator A will also automatically clear the PTnON bit and thus generate the Single Pulse output trailing edge. In this way the CCRA value can be used to control the pulse width. A compare match from Comparator A will also generate a PTMn interrupt. The counter can only be reset back to zero when the PTnON bit changes from low to high when the counter restarts. In the Single Pulse Mode CCRP is not used. The PTnCCLR bit is not used in this Mode.

Single Pulse Generation (n=0, 1 or 2)
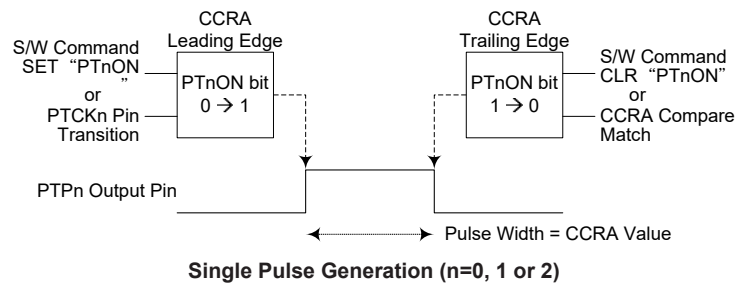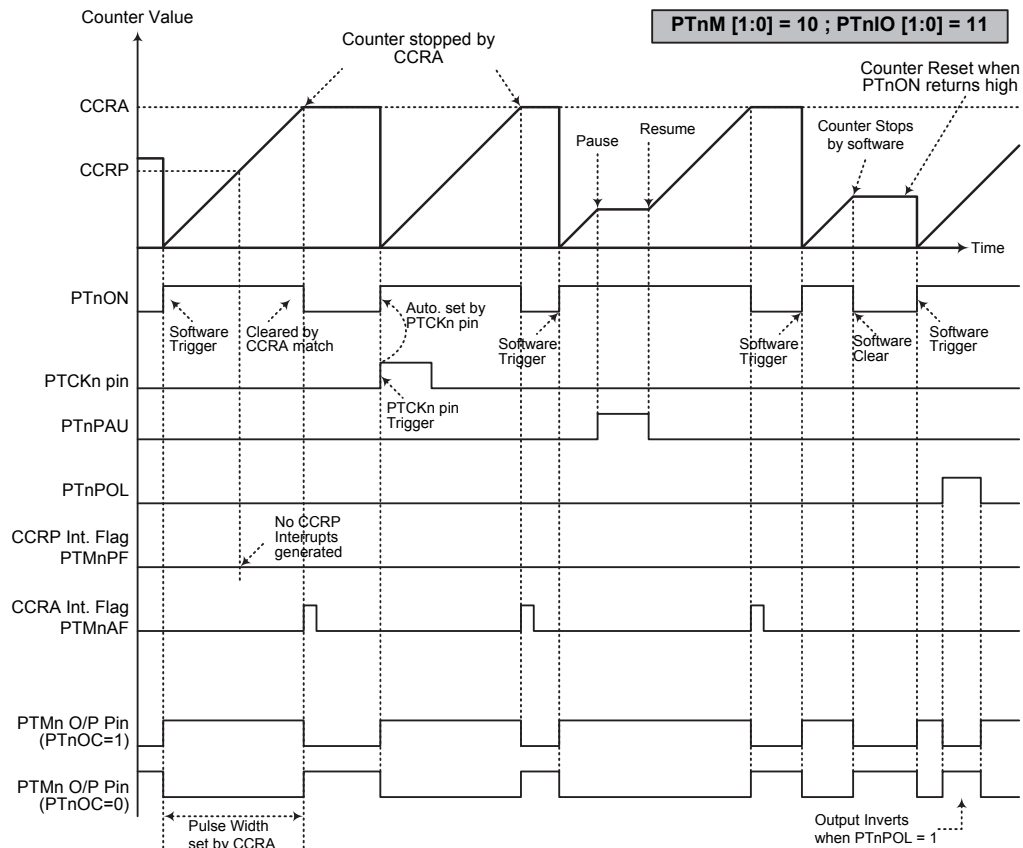
Single Pulse Mode (n=0, 1 or 2)

Note: 1. Counter stopped by CCRA

2. CCRP is not used

3. The pulse is triggered by the PTCKn pin or by setting the PTnON bit high

4. A PTCKn pin active edge will automatically set the PTnON bit high

5. In the Single Pulse Mode, PTnIO[1:0] must be set to "11" and cannot be changed.

Capture Input Mode

To select this mode bits PTnM1 and PTnM0 in the PTMnC1 register should be set to 01 respectively. This mode enables external signals to capture and store the present value of the internal counter and can therefore be used for applications such as pulse width measurements. The external signal is supplied on the PTPnI or PTCKn pin which is selected using the PTnCAPTS bit in the PTMnC1 register. The input pin active edge can be either a rising edge, a falling edge or both rising and falling edges; the active edge transition type is selected using the PTnIO1 and PTnIO0 bits in the PTMnC1 register. The counter is started when the PTnON bit changes from low to high which is initiated using the application program.

When the required edge transition appears on the PTPnI or PTCKn pin the present value in the counter will be latched into the CCRA registers and a PTMn interrupt generated. Irrespective of what events occur on the PTPnI or PTCKn pin, the counter will continue to free run until the PTnON bit changes from high to low. When a CCRP compare match occurs the counter will reset back to zero; in this way the CCRP value can be used to control the maximum counter value. When a CCRP compare match occurs from Comparator P, a PTMn interrupt will also be generated. Counting the number of overflow interrupt signals from the CCRP can be a useful method in measuring long pulse widths. The PTnIO1 and PTnIO0 bits can select the active trigger edge on the PTPnI or PTCKn pin to be a rising edge, falling edge or both edge types. If the PTnIO1 and PTnIO0 bits are both set high, then no capture operation will take place irrespective of what happens on the PTPnI or PTCKn pin, however it must be noted that the counter will continue to run.

As the PTPnI or PTCKn pin is pin shared with other functions, care must be taken if the PTMn is in the Capture Input Mode. This is because if the pin is setup as an output, then any transitions on this pin may cause an input capture operation to be executed. The PTnCCLR, PTnOC and PTnPOL bits are not used in this Mode.
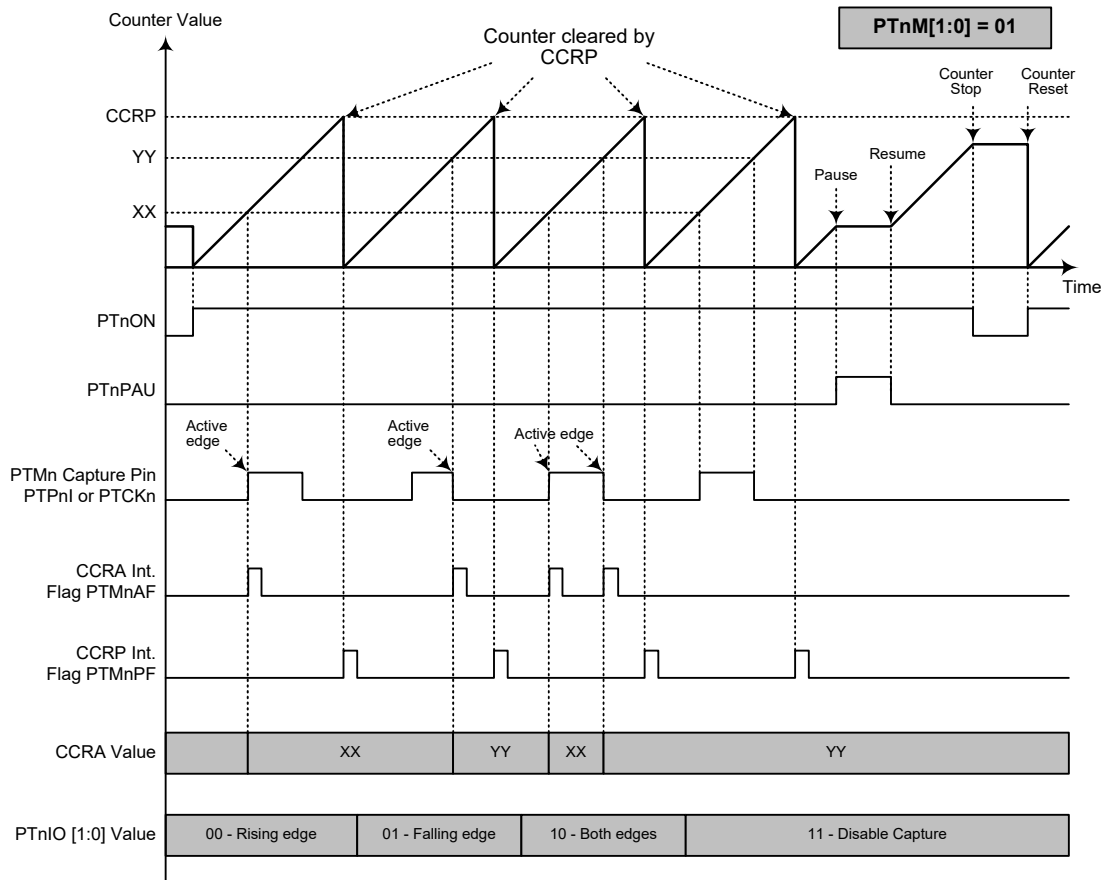
Capture Input Mode (n=0, 1 or 2)

Note: 1. PTnM[1:0]=01 and active edge set by the PTnIO[1:0] bits

    2. A PTMn Capture input pin active edge transfers the counter value to CCRA

    3. PTnCCLR bit not used

    4. No output function – PTnOC and PTnPOL bits are not used

    5. CCRP determines the counter value and the counter has a maximum count value when CCRP is equal to zero.

Internal Reference Voltage Generator

The device includes an internal reference voltage generator to provide an accurate reference voltage V_{IREF} for the A/D converter, 10-bit D/A Converter or other circuits. Refer to the Internal Reference Voltage Characteristics section for more information.
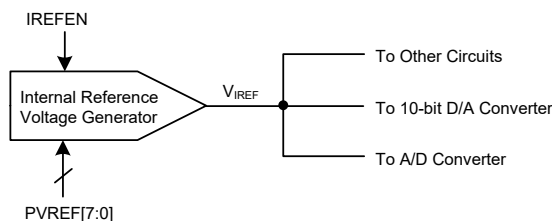
V_{IREF} Voltage Register Description

The internal reference voltage is controlled by two registers. The IREFC register is used for the enable/disabled control while the PVREF register is for fine tuning the internal reference voltage.

Register Name	Bit							
	7	6	5	4	3	2	1	0
IREFC	—	—	—	IREFEN	—	—	DACVRS1	DACVRS0
PVREF	D7	D6	D5	D4	D3	D2	D1	D0

V_{IREF} Register List

- **IREFC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	IREFEN	—	—	DACVRS1	DACVRS0
R/W	—	—	—	R/W	—	—	R/W	R/W
POR	—	—	—	0	—	—	0	0

Bit 7~5   Unimplemented, read as "0"
Bit 4   **IREFEN**: Internal Reference Voltage Generator control
　　　　　0: Disable
　　　　　1: Enable
This bit controls the internal reference voltage generator to provide V_{IREF} voltage for the 10-bit D/A converter or A/D converter. When the bit is set high, the internal reference voltage V_{IREF} can be used as the reference voltage. When this bit is equal to 0, the internal reference voltage generator will enter the power down mode and the output will be in a floating state. If the internal referenc voltage is not used by the other circuits, then the Internal Reference Voltage Generator should be properly configured to conserve power.
Bit 3~2   Unimplemented, read as "0"
Bit 1~0   **DACVRS1~DACVRS0**: 10-bit DAC Reference Voltage selection
　　　　　00/01: V_{IREF}
　　　　　10: V_{DD}
　　　　　11: High impedance (floating)

- **PVREF Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   **D7~D0**: Internal Reference Voltage generator fine tune control
Setting the register can fine tune the internal reference voltage in the range of -60mV~+60mV (base on PVREF=80(Hex)). When the D[7:0] value is increased by one, the internal reference voltage will decrease around 500μV, vice verse.

Digital to Analog Converter – DAC

This device includes a 10-bit D/A Converter which can provide a certain voltage from 0 to $0.5V_{DACVREF}$ to the non-inverting input of the OPA.
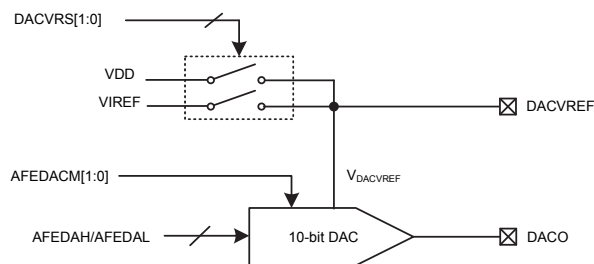
D/A Converter Registers

The DAC function is controlled by four registers. The DACVRS [1:0] bits in the IREFC register are used for selecting its reference voltage, the AFEDAC register is for the DAC function mode control. A 10-bit register pair of AFEDAH and AFEDAL is for the DAC output control.

Register Name	Bit							
	7	6	5	4	3	2	1	0
IREFC	—	—	—	IREFEN	—	—	DACVRS1	DACVRS0
AFEDAC	—	—	—	—	—	—	AFEDACEN1	AFEDACEN0
AFEDAL	D1	D0	—	—	—	—	—	—
AFEDAH	D9	D8	D7	D6	D5	D4	D3	D2

<div align="center">DAC Register List</div>

- **IREFC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	IREFEN	—	—	DACVRS1	DACVRS0
R/W	—	—	—	R/W	—	—	R/W	R/W
POR	—	—	—	0	—	—	0	0

Bit 7~5   Unimplemented, read as "0"

Bit 4   **IREFEN**: Internal Reference Voltage Generator control
    Described elsewhere

Bit 3~2   Unimplemented, read as "0"

Bit 1~0   **DACVRS1~DACVRS0**: 10-bit DAC Reference Voltage $V_{DACVREF}$ selection
      00/01: V_{IREF}
      10: V_{DD}
      11: Floating

- **AFEDAC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	AFEDACEN1	AFEDACEN0
R/W	—	—	—	—	—	—	R/W	R/W
POR	—	—	—	—	—	—	0	0

Bit 7~2   Unimplemented, read as "0"

Bit 1~0   **AFEDACM[1:0]**: 10-bit DAC mode control
    00: DAC disable, output in a high-impendance state
    01: DAC enable
    10: DAC disable, output in a GND state
    11: DAC enable

AFEDAH & AFEDAL Registers

Register	AFEDAH								AFEDAL							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Name	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	—	—	—	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—	—	—	—	—	—
POR	0	0	0	0	0	0	0	0	0	0	—	—	—	—	—	—

D9~D0: 10-bit DAC output control bits

"—": Unimplemented, read as "0"

The bit7~bit0 in the AFEDAH register combines with the bit7~bit6 in the AFEDAL register to form a 10-bit DAC value of 0 ~1023

$$\text{DAC Output Voltage} = V_{DACVREF} \times 0.5 \times (\text{DAC value} / 1024)$$

Note: Firstly write into the AFEDAL and then write into the AFEDAH register.

Operational Amplifier – OPA

This device includes an operational amplifier for measure applications. The 10-bit DAC offers a voltage of $0~0.5V_{DACVREF}$ to the non-inverting input of the OPA. The OPA provides 3 different amplifications by setting the switches SW0~SW2.
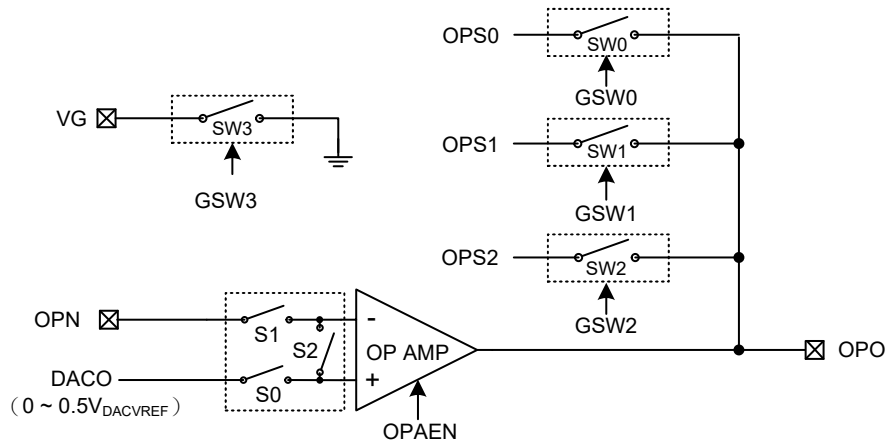
Operational Amplifier Structure

OPA Register Description

The internal Operational Amplifier operation is controlled by two registers. The OPAC register is used for the OPA enable/disabled control and input voltage offset calibration settings while the GSC register is for the OPA output control by setting SW0~SW3 on/off.

Register Name	Bit							
	7	6	5	4	3	2	1	0
OPAC	OPAOFM	OPARS	OPAEN	OPAOF4	OPAOF3	OPAOF2	OPAOF1	OPAOF0
GSC	—	—	—	—	GSW3	GSW2	GSW1	GSW0

OPA Register List

- **OPAC Register**

Bit	7	6	5	4	3	2	1	0
Name	OPAOFM	OPARS	OPAEN	OPAOF4	OPAOF3	OPAOF2	OPAOF1	OPAOF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7   **OPAOFM**: OPA normal operation or input offset voltage cancellation mode selection
       0: Normal operation
       1: Input offset voltage cancellation mode
     When the input offset cancellation mode is selected, the reference voltage input should be derived from the non-inverted input.

Bit 6   **OPARS**: OPA input offset voltage cancellation reference selection
       0: Select OPAIN as the reference input
       1: Select DACO as the reference input
     Note: The OPA input offset voltage cancellation be executed only when OPARS=1.

Bit 5   **OPAEN**: OPA enable/disable control
       0: Disable
       1: Enable

Bit 4~0   **OPAOF4~OPAOF0**: OPA input offset voltage cancellation control bits

- **GSC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	GSW3	GSW2	GSW1	GSW0
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	—	—	—	—	0	0	0	0

Bit 7~4   Unimplemented, read as "0"
Bit 3   **GSW3**: SW3 (Switch 3) control.
       0: Off
       1: On
     When this bit is set high, the VG pin connects to ground.
Bit 2   **GSW2**: SW2 (Switch 2) control.
       0: Off
       1: On
     When this bit is set high, the OPS2 pin connects to OPO.
Bit 1   **GSW1**: SW1 (Switch 1) control.
       0: Off
       1: On
     When this bit is set high, the OPS1 pin connects to OPO.
Bit 0   **GSW0**: SW0 (Switch 0) control.
       0: Off
       1: On
     When this bit is set high, the OPS0 pin connects to OPO.

Offset Calibration Procedure

The input voltage offset calibration can be executed only when setting the OPARS bit high. For operational amplifier input offset calibration, the procedures are summarized as the following.

Step1: Set OPAOFM=1 and OPARS=1, OPAMP is now under offset calibration mode, S0 and S2 on. To make sure V_{OS} as minimize as possible after calibration, the input reference voltage in calibration should be the same as input DC operating voltage in normal mode operation.

Step2: Set OPAOF[4:0]=00000, then read the OPO pin

Step3: Let OPAOF[4:0]=OPAOF[4:0] + 1 then read the OPO pin. If the OPO pin state is changed, record the data as V_{OS1}

Step4: Set OPAOF[4:0]=11111, then read OPO pin.

Step5: Let OPAOF[4:0]=OPAOF[4:0] - 1 then read OPO pin, if the OPO pin state is changed, record the data as V_{OS2}

Step6: Restore $V_{OS}=(V_{OS1} + V_{OS2})/2$ to OPAOF[4:0] bits, the calibration is finished.
If $(V_{OS1} + V_{OS2})/2$ is not integral, discard the decimal.

Analog to Digital Converter – ADC

The need to interface to real world analog signals is a common requirement for many electronic systems. However, to properly process these signals by a microcontroller, they must first be converted into digital signals by A/D converters. By integrating the A/D conversion electronic circuitry into the microcontroller, the need for external components is reduced significantly with the corresponding follow-on benefits of lower costs and reduced component space requirements.

A/D Converter Overview

This device contains a multi-channel analog to digital converter which can directly interface to external analog signals, such as that from sensors or other control signals and convert these signals directly into a 12-bit digital value. It also can convert the internal signals, the OPA output signal (OPS0, OPS1 or OPS2) and the DAC output signal DACO, into a 12-bit digital value. The external or internal analog signal to be converted is determined by the SAINS2~SAINS0 bits together with the SACS3~SACS0 bits. When the external analog signal is to be converted, the corresponding pin-shared control bits should first be properly configured and then the desired external channel input should be selected using the SAINS2~SAINS0 and SACS3~SACS0 bits. Note that when the internal analog signal is to be converted, the pin-shared control bits should also be properly configured except the SAINS and SACS bit fields. More detailed information about the A/D input signal is described in the "A/D Converter Control Registers" and "A/D Converter Input Signals" sections respectively.

External Input Channels	Internal Signals	Input signal Selection Bits
4: AN0~AN3	OPA output: OPS0, OPS1, OPS2 DAC output: DACO	SAINS2~SAINS0, SACS3~SACS0

The accompanying block diagram shows the overall internal structure of the A/D converter, together with its associated registers.
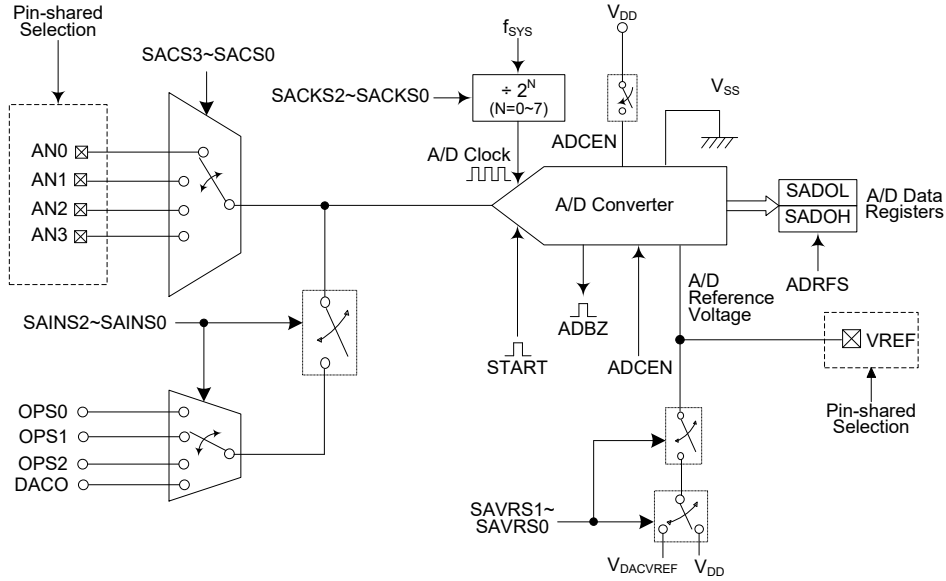
A/D Converter Structure

A/D Converter Register Description

Overall operation of the A/D converter is controlled using several registers. A read only register pair exists to store the A/D converter data 12-bit value. The remaining two registers are control registers which setup the operating and control function of the A/D converter.

Register Name	Bit							
	7	6	5	4	3	2	1	0
SADOL(ADRFS=0)	D3	D2	D1	D0	—	—	—	—
SADOL(ADRFS=1)	D7	D6	D5	D4	D3	D2	D1	D0
SADOH(ADRFS=0)	D11	D10	D9	D8	D7	D6	D5	D4
SADOH(ADRFS=1)	—	—	—	—	D11	D10	D9	D8
SADC0	START	ADBZ	ADCEN	ADRFS	SACS3	SACS2	SACS1	SACS0
SADC1	SAINS2	SAINS1	SAINS0	SAVRS1	SAVRS0	SACKS2	SACKS1	SACKS0

A/D Converter Register List

A/D Converter Data Registers – SADOL, SADOH

As this device contains an internal 12-bit A/D converter, it requires two data registers to store the converted value. These are a high byte register, known as SADOH, and a low byte register, known as SADOL. After the conversion process takes place, these registers can be directly read by the microcontroller to obtain the digitised conversion value. As only 12 bits of the 16-bit register space is utilised, the format in which the data is stored is controlled by the ADRFS bit in the SADC0 register as shown in the accompanying table. D0~D11 are the A/D conversion result data bits. Any unused bits will be read as zero. Note that A/D data registers contents will be unchanged if the A/D converter is disabled.

ADRFS	SADOH								SADOL							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0
1	0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

A/D Data Registers

A/D Converter Control Registers – SADC0, SADC1

To control the function and operation of the A/D converter, two control registers known as SADC0 and SADC1 are provided. These 8-bit registers define functions such as the selection of which analog channel is connected to the internal A/D converter, the digitised data format, the A/D clock source as well as controlling the start function and monitoring the A/D converter busy status. As the device contains only one actual analog to digital converter hardware circuit, each of the external or internal analog signal inputs must be routed to the converter. The SACS3~SACS0 bits in the SADC0 register are used to determine which external channel input is selected to be converted. The SAINS2~SAINS0 bits in the SADC1 register are used to determine that the analog signal to be converted comes from the internal analog signal or external analog channel input.

The relevant pin-shared function selection bits determine which pins on I/O Ports are used as analog inputs for the A/D converter input and which pins are not to be used as the A/D converter input. When the pin is selected to be an A/D input, its original function whether it is an I/O or other pin-shared function will be removed. In addition, any internal pull-high resistor connected to the pin will be automatically removed if the pin is selected to be an A/D converter input.

- **SADC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	START	ADBZ	ADCEN	ADRFS	SACS3	SACS2	SACS1	SACS0
R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7   **START**: Start the A/D conversion
        $0{\rightarrow}1{\rightarrow}0$: Start
    This bit is used to initiate an A/D conversion process. The bit is normally low but if set high and then cleared low again, the A/D converter will initiate a conversion process. When the bit is set high the A/D converter will be reset.

Bit 6   **ADBZ**: A/D converter busy flag
        0: No A/D conversion is in progress
        1: A/D conversion is in progress
    This read only flag is used to indicate whether the A/D conversion is in progress or not. When the START bit is set from low to high and then to low again, the ADBZ flag will be set to 1 to indicate that the A/D conversion is initiated. The ADBZ flag will be cleared to 0 after the A/D conversion is complete.

Bit 5   **ADCEN**: A/D converter function enable control
        0: Disable
        1: Enable
    This bit controls the A/D internal function. This bit should be set to one to enable the A/D converter. If the bit is set low, then the A/D converter will be switched off reducing the device power consumption. When the A/D converter function is disabled, the contents of the A/D data register pair known as ADRH and ADRL will be unchanged.

Bit 4   **ADRFS**: A/D converter data format select
        0: A/D converter data format $\rightarrow$ SADOH=D[11:4]; SADOL=D[3:0]
        1: A/D converter data format $\rightarrow$ SADOH=D[11:8]; SADOL=D[7:0]
    This bit controls the format of the 12-bit converted A/D value in the two A/D data registers. Details are provided in the A/D data register section.

Bit 3~0   **SACS3~SACS0**: A/D converter external analog channel input select
        0000: AN0
        0001: AN1
        0010: AN2
        0011: AN3
        0100~1111: Floating

- **SADC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	SAINS2	SAINS1	SAINS0	SAVRS1	SAVRS0	SACKS2	SACKS1	SACKS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~5   **SAINS2~SAINS0**: A/D converter input signal select
     000: External input – External analog channel input
     001: OPS0
     010: OPS1
     011: OPS2
     100: DACO
     101~111: External input – External analog channel input

     Care must be taken if the SAINS2~SAINS0 bits are set from "001" to "100" to select the internal analog signal to be converted. When the internal analog signal is selected to be converted, the external input pin must never be selected as the A/D input signal by properly setting the SACS3~SACS0 bits with a value from 0100 to 1111. Otherwise, the external channel input will be connected together with the internal analog signal. This will result in unpredictable situations such as an irreversible damage.

Bit 4~3   **SAVRS1~SAVRS0**: A/D converter reference voltage select
     00/11: From VREF pin
     01: Internal A/D converter power, V_{DD}
     10: Internal DAC reference voltage, $V_{DACVREF}$

     These bits are used to select the A/D converter reference voltage. Care must be taken if the SAVRS1~SAVRS0 bits are set to "01" or "10" to select the internal V_{DD} or DAC reference voltage as the A/D Converter reference voltage source. When the internal A/D converter power or DAC reference voltage is selected as the reference voltage, the VREF pin cannot be configured as the reference voltage input by properly configuring the corresponding pin-shared function control bits. Otherwise, the external input voltage on VREF pin will be connected to the internal A/D converter power or the DAC reference voltage. This will result in unpredictable situations

Bit 2~0   **SACKS2~SACKS0**: A/D conversion clock source select
     000: f_{SYS}
     001: $f_{SYS}/2$
     010: $f_{SYS}/4$
     011: $f_{SYS}/8$
     100: $f_{SYS}/16$
     101: $f_{SYS}/32$
     110: $f_{SYS}/64$
     111: $f_{SYS}/128$

     These three bits are used to select the clock source for the A/D converter.

A/D Converter Operation

The START bit in the SADC0 register is used to start the A/D conversion. When the microcontroller sets this bit from low to high and then low again, an analog to digital conversion cycle will be initiated.

The ADBZ bit in the SADC0 register is used to indicate whether the analog to digital conversion process is in progress or not. This bit will be automatically set to 1 by the microcontroller after an A/D conversion is successfully initiated. When the A/D conversion is complete, the ADBZ will be cleared to 0. In addition, the corresponding A/D interrupt request flag will be set in the interrupt control register, and if the interrupts are enabled, an appropriate internal interrupt signal will be generated. This A/D internal interrupt signal will direct the program flow to the associated A/D internal interrupt address for processing. If the A/D internal interrupt is disabled, the microcontroller can poll the ADBZ bit in the SADC0 register to check whether it has been cleared as an alternative method of detecting the end of an A/D conversion cycle.

The clock source for the A/D converter, which originates from the system clock f_{SYS}, can be chosen to be either f_{SYS} or a subdivided version of f_{SYS}. The division ratio value is determined by the SACKS2~SACKS0 bits in the SADC1 register. Although the A/D clock source is determined by the system clock f_{SYS} and by bits SACKS2~SACKS0, there are some limitations on the maximum A/D clock source speed that can be selected. As the recommended range of permissible A/D clock period, t_{ADCK}, is from 0.5μs to 10μs, care must be taken for system clock frequencies. For example, as the system clock operates at a frequency of 8MHz, the SACKS2~SACKS0 bits should not be set to 000, 001 or 111. Doing so will give A/D clock periods that are less   or larger than the minimum or maximum A/D clock period which may result in inaccurate A/D conversion values. Refer to the following table for examples, where values marked with an asterisk * show where, depending upon the device, special care must be taken, as the values may be less or larger than the specified minimum A/D Clock Period range.

f_{SYS}	A/D Clock Period (t_{ADCK})							
	SACKS [2:0]= 000 (f_{SYS})	SACKS [2:0]= 001 (f_{SYS}/2)	SACKS [2:0]= 010 (f_{SYS}/4)	SACKS [2:0]= 011 (f_{SYS}/8)	SACKS [2:0]= 100 (f_{SYS}/16)	SACKS [2:0]= 101 (f_{SYS}/32)	SACKS [2:0]= 110 (f_{SYS}/64)	SACKS [2:0]= 111 (f_{SYS}/128)
1MHz	1μs	2μs	4μs	8μs	16μs *	32μs *	64μs *	128μs *
2MHz	500ns	1μs	2μs	4μs	8μs	16μs *	32μs *	64μs *
4MHz	250ns *	500ns	1μs	2μs	4μs	8μs	16μs *	32μs *
8MHz	125ns *	250ns *	500ns	1μs	2μs	4μs	8μs	16μs *
12MHz	83ns *	167ns *	333ns *	667ns	1.33μs	2.67μs	5.33μs	10.67μs *
16MHz	62.5ns *	125ns *	250ns *	500ns	1μs	2μs	4μs	8μs

A/D Clock Period Examples

Controlling the power on/off function of the A/D converter circuitry is implemented using the ADCEN bit in the SADC0 register. This bit must be set high to power on the A/D converter. When the ADCEN bit is set high to power on the A/D converter internal circuitry a certain delay, as indicated in the timing diagram, must be allowed before an A/D conversion is initiated. Even if no pins are selected for use as A/D inputs, if the ADCEN bit is high, then some power will still be consumed. In power conscious applications it is therefore recommended that the ADCEN is set low to reduce power consumption when the A/D converter function is not being used.

A/D Converter Reference Voltage

The reference voltage supply to the A/D converter can be supplied from the power supply V_{DD}, the DAC reference voltage $V_{DACVREF}$ or from an external reference source supplied on pin VREF. The desired selection is made using the SAVRS1 and SAVRS0 bits. When the SAVRS bit field is set to "01", the A/D converter reference voltage will come from the internal power V_{DD}. When the SAVRS bit field is set to "10", the A/D converter reference voltage will come from the DAC reference voltage $V_{DACVREF}$. When the SAVRS bit field is set to "00" or "11", the A/D converter reference voltage will come from the external VREF pin. However, if the internal A/D converter power or the DAC reference voltage is selected as the reference voltage, the VREF pin must not be configured as the reference voltage input function for the A/D converter to avoid the unpredictable situations. The analog input values must not be allowed to exceed the value of the selected reference voltage.

A/D Converter Input Signals

All the external A/D analog channel input pins are pin-shared with the I/O pins as well as other functions. The corresponding control bits for each A/D external input pin in the PCS0 register determine whether the input pins are setup as A/D converter analog inputs or whether they have other functions. If the pin is setup to be as an A/D analog channel input, the original pin functions will be disabled. In this way, pins can be changed under program control to change their function

between A/D inputs and other functions. All pull high resistors, which are setup through register programming, will be automatically disconnected if the pins are setup as A/D inputs. Note that it is not necessary to first setup the A/D pin as an input in the port control register to enable the A/D input as when the pin-shared function control bits enable an A/D input, the status of the port control register will be overridden.

There are four internal analog signals derived from the OPA output voltage or DAC output signal, which can be connected to the A/D converter as the analog input signal by configuring the SAINS2~SAINS0 bits. If the external channel input is selected to be converted, the SAINS2~SAINS0 bits should be set to "000" or "101~111" and the SACS3~SACS0 bits can determine which external channel is selected. If the internal analog signal is selected to be converted, the SACS3~SACS0 bits must be configured with a value from 0100 to 1111 to switch off the external analog channel input. Otherwise, the internal analog signal will be connected together with the external channel input. This will result in unpredictable situations.

SAINS[2:0]	SACS[3:0]	Input Signals	Description
000, 101~111	0000~0011	AN0~AN3	External pin analog input
	0100~1111	—	Non-existed channel, input is floating.
001	0100~1111	OPS0	OPA output
010	0100~1111	OPS1	OPA output
011	0100~1111	OPS2	OPA output
100	0100~1111	DACO	DAC output

A/D Converter Input Signal Selection

Conversion Rate and Timing Diagram

A complete A/D conversion contains two parts, data sampling and data conversion. The data sampling which is defined as t_{ADS} takes 4 A/D clock cycles and the data conversion takes 12 A/D clock cycles. Therefore a total of 16 A/D clock cycles for an external input A/D conversion which is defined as t_{ADC} are necessary.

Maximum single A/D conversion rate=A/D clock period / 16

The accompanying diagram shows graphically the various stages involved in an analog to digital conversion process and its associated timing. After an A/D conversion process has been initiated by the application program, the microcontroller internal hardware will begin to carry out the conversion, during which time the program can continue with other functions. The time taken for the A/D conversion is 16 t_{ADCK} clock cycles where t_{ADCK} is equal to the A/D clock period.

A/D Conversion Timing – External Channel Input
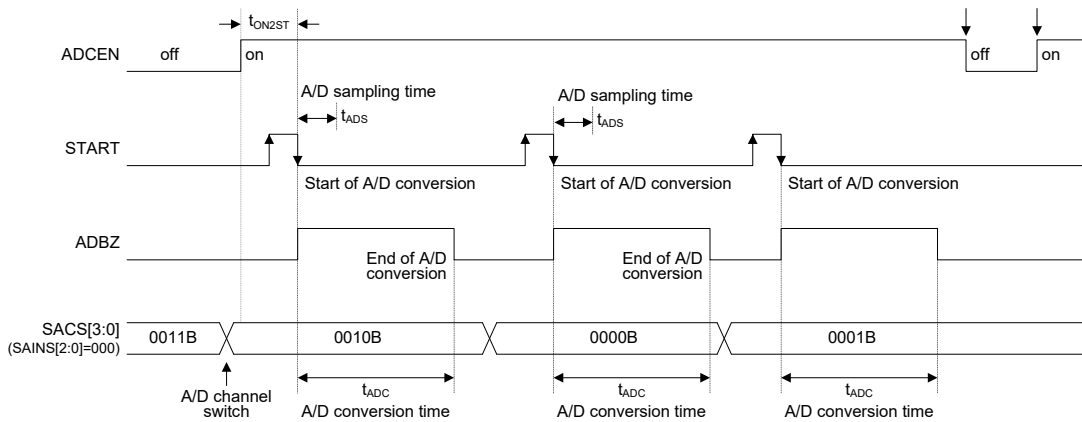
Summary of A/D Conversion Steps

The following summarises the individual steps that should be executed in order to implement an A/D conversion process.

- Step 1

  Select the required A/D conversion clock by correctly programming bits SACKS2~SACKS0 in the SADC1 register.

- Step 2

  Enable the A/D by setting the ADCEN bit in the SADC0 register to 1.

- Step 3

  Select which signal is to be connected to the internal A/D converter by correctly configuring the SAINS2~SAINS0 bits

  Select the external channel input to be converted, go to Step 4.

  Select the internal analog signal to be converted, go to Step 5.

- Step 4

  If the A/D input signal comes from the external channel input selecting by configuring the SAINS bit field, the corresponding pins should be configured as A/D input function by configuring the relevant pin-shared function control bits. The desired analog channel then should be selected by configuring the SACS bit field. After this step, go to Step 6.

- Step 5

  Before the A/D input signal is selected to come from the internal analog signal by configuring the SAINS bit field, the corresponding external input pin must be switched to a non-existed channel input by setting the SACS3~SACS0 bits with a value from 0100 to 1111. The desired internal analog signal then can be selected by configuring the SAINS bit field. After this step, go to Step 6.

- Step 6

  Select the reference voltage source by configuring the SAVRS1~SAVRS0 bits in the SADC1 register.

- Step 7

  Select A/D converter output data format by setting the ADRFS bit in the SADC0 register.

- Step 8

  If A/D conversion interrupt is used, the interrupt control registers must be correctly configured to ensure the A/D interrupt function is active. The master interrupt control bit, EMI, and the A/D conversion interrupt control bit, ADE, must both be set high in advance.

- Step 9

  The A/D conversion procedure can now be initialized by setting the START bit from low to high and then low again.

- Step 10

  If A/D conversion is in progress, the ADBZ flag will be set high. After the A/D conversion process is complete, the ADBZ flag will go low and then the output data can be read from SADOH and SADOL registers.

Note: When checking for the end of the conversion process, if the method of polling the ADBZ bit in the SADC0 register is used, the interrupt enable step above can be omitted.

Programming Considerations

During microcontroller operations where the A/D converter is not being used, the A/D internal circuitry can be switched off to reduce power consumption, by clearing bit ADCEN to 0 in the SADC0 register. When this happens, the internal A/D converter circuits will not consume power irrespective of what analog voltage is applied to their input lines. If the A/D converter input lines are used as normal I/Os, then care must be taken as if the input voltage is not at a valid logic level, then this may lead to some increase in power consumption.

A/D Conversion Function

As the device contains a 12-bit A/D converter, its full-scale converted digitised value is equal to FFFH. Since the full-scale analog input value is equal to the actual A/D converter reference voltage, V_{REF}, this gives a single bit analog input value of V_{REF} divided by 4096.

$$1 \text{ LSB} = V_{REF} \div 4096$$

The A/D Converter input voltage value can be calculated using the following equation:

$$\text{A/D input voltage} = \text{A/D output digital value} \times V_{REF} \div 4096$$

The diagram shows the ideal transfer function between the analog input value and the digitised output value for the A/D converter. Except for the digitised zero value, the subsequent digitised values will change at a point 0.5 LSB below where they would change without the offset, and the last full scale digitised value will change at a point 1.5 LSB below the V_{REF} level. Note that here the V_{REF} voltage is the actual A/D converter reference voltage determined by the SAVRS field.
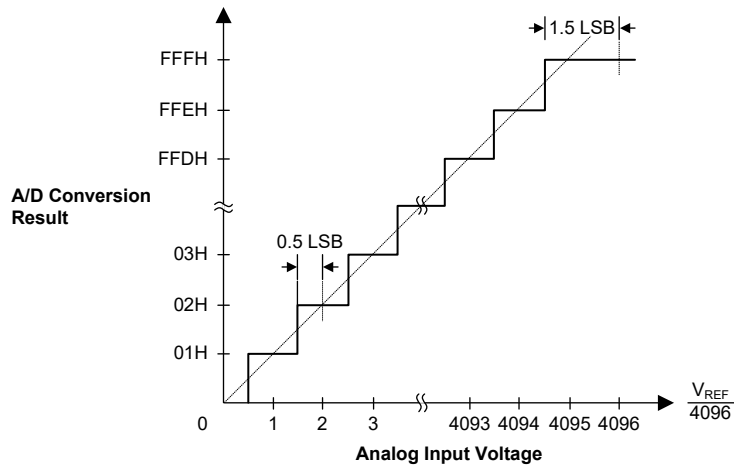
Ideal A/D Transfer Function

A/D Conversion Programming Examples

The following two programming examples illustrate how to setup and implement an A/D conversion. In the first example, the method of polling the ADBZ bit in the SADC0 register is used to detect when the conversion cycle is complete, whereas in the second example, the A/D interrupt is used to determine when the conversion is complete.

Example: using an ADBZ polling method to detect the end of conversion

```
clr   ADE              ; disable ADC interrupt
mov   a,03H
mov   SADC1,a          ; select fSYS/8 as A/D clock
set   ADCEN
mov   a, 30h           ; setup PCS0 to configure pin AN0
```

```
        mov  PCS0,a
        mov  a,20h
        mov  SADC0,a              ; enable and connect AN0 channel to A/D converter
        :
start_conversion:
        clr  START                ; high pulse on start bit to initiate conversion
        set  START                ; reset A/D
        clr  START                ; start A/D
polling_EOC:
        sz   ADBZ                 ; poll the SADC0 register ADBZ bit to detect end of A/D conversion
        jmp  polling_EOC          ; continue polling
        mov  a,SADOL              ; read low byte conversion result value
        mov  SADOL_buffer,a       ; save result to user defined register
        mov  a,SADOH              ; read high byte conversion result value
        mov  SADOH_buffer,a       ; save result to user defined register
        :
        :
        jmp  start_conversion     ; start next A/D conversion
```

Example: using the interrupt method to detect the end of conversion

```
        clr  ADE                  ; disable ADC interrupt
        mov  a,03H
        mov  SADC1,a              ; select f_SYS/8 as A/D clock
        set  ADCEN
        mov  a, 30h               ; setup PCS0 to configure pin AN0
        mov  PCS0,a
        mov  a,20h
        mov  SADC0,a              ; enable and connect AN0 channel to A/D converter
Start_conversion:
        clr  START                ; high pulse on START bit to initiate conversion
        set  START                ; reset A/D
        clr  START                ; start A/D
        clr  ADF                  ; clear ADC interrupt request flag
        set  ADE                  ; enable ADC interrupt
        set  EMI                  ; enable global interrupt
        :
        :
        ; ADC interrupt service routine
ADC_ISR:
        mov  acc_stack,a          ; save ACC to user defined memory
        mov  a,STATUS
        mov  status_stack,a       ; save STATUS to user defined memory
        :
        :
        mov  a,SADOL              ; read low byte conversion result value
        mov  SADOL_buffer,a       ; save result to user defined register
        mov  a,SADOH              ; read high byte conversion result value
        mov  SADOH_buffer,a       ; save result to user defined register
        :
        :
EXIT_INT_ISR:
        mov  a,status_stack
        mov  STATUS,a             ; restore STATUS from user defined memory
        mov  a,acc_stack          ; restore ACC from user defined memory
        reti
```

16-bit Multiplication Division Unit – MDU

The device has a 16-bit Multiplication Division Unit, MDU, which integrates a 16-bit unsigned multiplier and a 32-bit/16-bit divider. The MDU, in replacing the software multiplication and division operations, can therefore save large amounts of computing time as well as the Program and Data Memory space. It also reduces the overall microcontroller loading and results in the overall system performance improvements.

16-Bit MDU Block Diagram
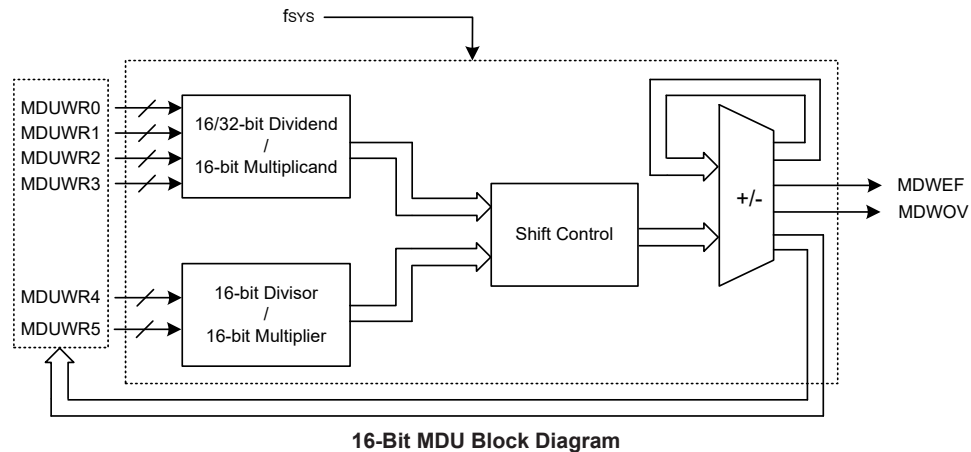
MDU Registers

The multiplication and division operations are implemented in a specific way, a specific write access sequence of a series of MDU data registers. The status register, MDUWCTRL, provides the indications for the MDU operation. The data register each is used to store the data regarded as the different operand corresponding to different MDU operations.

Register Name	Bit							
	7	6	5	4	3	2	1	0
MDUWR0	D7	D6	D5	D4	D3	D2	D1	D0
MDUWR1	D7	D6	D5	D4	D3	D2	D1	D0
MDUWR2	D7	D6	D5	D4	D3	D2	D1	D0
MDUWR3	D7	D6	D5	D4	D3	D2	D1	D0
MDUWR4	D7	D6	D5	D4	D3	D2	D1	D0
MDUWR5	D7	D6	D5	D4	D3	D2	D1	D0
MDUWCTRL	MDWEF	MDWOV	—	—	—	—	—	—

MDU Register List

- **MDUWRn Register (n=0~5)**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x": unknown

Bit 7~0   **D7~D0**: 16-bit MDU data register n
Using the register depends on the current MDU operation

- **MDUWCTRL Register**

Bit	7	6	5	4	3	2	1	0
Name	MDWEF	MDWOV	—	—	—	—	—	—
R/W	R	R	—	—	—	—	—	—
POR	0	0	—	—	—	—	—	—

Bit 7   **MDWEF**: 16-bit MDU error flag
　　　　　0: Normal
　　　　　1: Abnormal
　　　　This bit will be set to 1 if the data register MDUWRn is written or read as the MDU operation is executing. This bit should be cleared to 0 by reading the MDUWCTRL register if it is equal to 1 and the MDU operation is completed.

Bit 6   **MDWOV**: 16-bit MDU overflow flag
　　　　　0: No overflow occurs
　　　　　1: Multiplication product > FFFFH or Divisor=0
　　　　When an operation is completed, this bit will be updated by hardware to a new value corresponding to the current operation situation.

Bit 5~0   Unimplemented, read as "0"

MDU Operation

For this MDU the multiplication or division operation is carried out in a specific way and is determined by the write access sequence of the six MDU data registers, MDUWR0~MDUWR5. The low byte data, regardless of the dividend, multiplicand, divisor or multiplier, must first be written into the corresponding MDU data register followed by the high byte data. All MDU operations will be executed after the MDUWR5 register is write-accessed together with the correct specific write access sequence of the MDUWRn. Note that it is not necessary to consecutively write data into the MDU data registers but must be in a correct write access sequence. Therefore, a non-write MDUWRn instruction or an interrupt, etc., can be inserted into the correct write access sequence without destroying the write operation. The relationship between the write access sequence and the MDU operation is shown in the following.

- 32-bit/16-bit division operation: Write data sequentially into the six MDU data registers from MDUWR0 to MDUWR5.

- 16-bit/16-bit division operation: Write data sequentially into the specific four MDU data registers in a sequence of MDUWR0, MDUWR1, MDUWR4 and MDUWR5 with no write access to MDUWR2 and MDUWR3.

- 16-bit×16-bit multiplication operation: Write data sequentially into the specific four MDU data register in a sequence of MDUWR0, MDUWR4, MDUWR1 and MDUWR5 with no write access to MDUWR2 and MDUWR3.

After the specific write access sequence is determined, the MDU will start to perform the corresponding operation. The calculation time necessary for these MDU operations are different. During the calculation time any read/write access to the six MDU data registers is forbidden. After the completion of each operation, it is necessary to check the operation status in the MDUWCTRL register to make sure that whether the operation is correct or not. Then the operation result can be read out from the corresponding MDU data registers in a specific read access sequence if the operation is correctly finished. The necessary calculation time for different MDU operations is listed in the following.

- 32-bit/16-bit division operation: $17 \times t_{SYS}$.

- 16-bit/16-bit division operation: $9 \times t_{SYS}$.

- 16-bit×16-bit multiplication operation: $11 \times t_{SYS}$.

The operation results will be stored in the corresponding MDU data registers and should be read out from the MDU data registers in a specific read access sequence after the operation is completed. Noe that it is not necessary to consecutively read data out from the MDU data registers but must be in a correct read access sequence. Therefore, a non-read MDUWRn instruction or an interrupt, etc., can be inserted into the correct read access sequence without destroying the read operation. The relationship between the operation result read access sequence and the MDU operation is shown in the following.

- 32-bit/16-bit division operation: Read the quotient from MDUWR0 to MDUWR3 and remainder from MDUWR4 and MDUWR5 sequentially.

- 16-bit/16-bit division operation: Read the quotient from MDUWR0 and MDUWR1 and remainder from MDUWR4 and MDUWR5 sequentially.

- 16-bit×16-bit multiplication operation: Read the product sequentially from MDUWR0 to MDUWR3.

The overall important points for the MDU read/write access sequence and calculation time are summarized in the following table.

Operations \ Items	32-bit / 16-bit Division	16-bit / 16-bit Division	16-bit×16-bit Multiplication
Write Sequence First write ↓↓↓↓ Last write	Dividend Byte 0 written to MDUWR0 Dividend Byte 1 written to MDUWR1 Dividend Byte 2 written to MDUWR2 Dividend Byte 3 written to MDUWR3 Divisor Byte 0 written to MDUWR4 Divisor Byte 1 written to MDUWR5	Dividend Byte 0 written to MDUWR0 Dividend Byte 1 written to MDUWR1 Divisor Byte 0 written to MDUWR4 Divisor Byte 1 written to MDUWR5	Multiplicand Byte 0 written to MDUWR0 Multiplier Byte 0 written to MDUWR4 Multiplicand Byte 1 written to MDUWR1 Multiplier Byte 1 written to MDUWR5
Calculation Time	$17 \times t_{SYS}$	$9 \times t_{SYS}$	$11 \times t_{SYS}$
Read Sequence First read ↓↓↓↓ Last read	Quotient Byte 0 read from MDUWR0 Quotient Byte 1 read from MDUWR1 Quotient Byte 2 read from MDUWR2 Quotient Byte 3 read from MDUWR3 Remainder Byte 0 read from MDUWR4 Remainder Byte 1 read from MDUWR5	Quotient Byte 0 read from MDUWR0 Quotient Byte 1 read from MDUWR1 Remainder Byte 0 read from MDUWR4 Remainder Byte 1 read from MDUWR5	Product Byte 0 written to MDUWR0 Product Byte 1 written to MDUWR1 Product Byte 2 written to MDUWR2 Product Byte 3 written to MDUWR3

MDU Operations Summary

Over Voltage Protection – OVP

The device includes an over voltage protection function which provides a protection mechanism for applications. To prevent the operating voltage from exceeding a specific level, the voltage on the OVPI pin is compared with a reference voltage generated by an 8-bit DAC. When an over voltage event occurs, an OVP interrupt will be generated if the corresponding interrupt control is enabled.
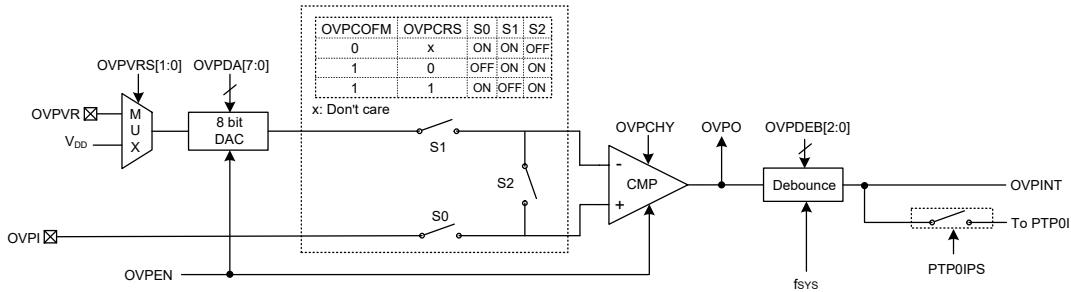
Over Voltage Protection Circuit

Over Voltage Protection Operation

The source voltage is supplied on the OVPI pin and then connected to one input of the comparator. A DAC is used to generate a reference voltage. The comparator compares the reference voltage with the input voltage to produce the OVPO signal.

Over Voltage Protection Control Registers

Overall operation of the over voltage protection is controlled using several registers. One register is used to provide the reference voltages for the over voltage protection circuit. The remaining two registers are control registers which are used to control the OVP function, DAC reference voltage selection, comparator de-bounce time, comparator hysteresis function together with the comparator input offset calibration.

Register Name	Bit							
	7	6	5	4	3	2	1	0
OVPC0	—	—	OVPEN	OVPCHY	—	OVPVRS	OVPDEB1	OVPDEB0
OVPC1	OVPO	OVPCOFM	OVPCRS	OVPCOF4	OVPCOF3	OVPCOF2	OVPCOF1	OVPCOF0
OVPDA	D7	D6	D5	D4	D3	D2	D1	D0

OVP Register List

- **OVPC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	OVPEN	OVPCHY	—	OVPVRS	OVPDEB1	OVPDEB0
R/W	—	—	R/W	R/W	—	R/W	R/W	R/W
POR	—	—	0	0	—	0	0	0

Bit 7~6   Unimplemented, read as "0"

Bit 5   **OVPEN**: OVP function control bit
      0: Disable
      1: Enable

      If the OVPEN bit is cleared to 0, the over voltage protection function is disabled and no power will be consumed. This results in the comparator and D/A converter of OVP both being switched off.

Bit 4   **OVPCHY**: OVP comparator hysteresis function control bit
      0: Disable
      1: Enable

Bit 3   Unimplemented, read as "0"

Bit 2   **OVPVRS**: OVP DAC reference voltage selection bit
      0: DAC reference voltage comes from V_{DD}
      1: DAC reference voltage comes from OVPVR pin

Bit 1~0   **OVPDEB1~OVPDEB0**: OVP comparator debounce time control bits
      00: No debounce
      01: $(7\sim8) \times 1/f_{SYS}$
      10: $(15\sim16) \times 1/f_{SYS}$
      11: $(31\sim32) \times 1/f_{SYS}$

- **OVPC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	OVPO	OVPCOFM	OVPCRS	OVPCOF4	OVPCOF3	OVPCOF2	OVPCOF1	OVPCOF0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	1	0	0	0	0

Bit 7   **OVPO**: OVP comparator ouptut bit
        0: Positive input voltage < negative input voltage
        1: Positive input voltage > negative input voltage

Bit 6   **OVPCOFM**: OVP comparator normal operation or input offset voltage calibration mode selection
        0: Normal operation
        1: Input offset voltage calibration mode

Bit 5   **OVPCRS**: OVP comparator input offset voltage calibration reference selection bit
        0: Input reference voltage comes from negative input
        1: Input reference voltage comes from positive input

Bit 4~0   **OVPCOF4~OVPCOF0**: OVP comparator input offset voltage calibration control bits

- **OVPDA Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   OVP DAC output voltage control bits
        DAC Output: DAC V_{OUT}=(DAC reference voltage / 256) × OVPDA[7:0]

Offset Calibration

The OVPCOFM bit in the OVPC1 register is used to select the OVP comparator operating mode, normal operation or offset calibration mode. If set the bit high, the comparator will enter the offset voltage calibration mode. It is need to note that before offset calibration, the hysteresis voltage should be zero by set OVPCHY=0 and because the OVP pin are pin-shared with I/O, it should be configured as comparator input first.

Comparator Calibration Procedure:

Step1: Set OVPCOFM=1, OVPCRS=1, the OVP is now in the comparator calibration mode, S0 and S2 on. To make sure V_{OS} as minimize as possible after calibration, the input reference voltage in calibration should be the same as input DC operating voltage in normal mode operation.

Step2: Set OVPCOF[4:0]=00000 then read OVPO bit

Step3: Let OVPCOF[4:0]=OVPCOF[4:0]+1 then read the OVPO bit status; if OVPO is changed, record the OVPCOF[4:0] data as V_{OS1}

Step4: Set OVPCOF[4:0]=11111 then read the OVPO bit status

Step5: Let OVPCOF[4:0]=OVPCOF[4:0]-1 then read the OVPO bit status; if OVPO data is changed, record the OVPCOF[4:0] data as V_{OS2}.

Step6: Restore V_{OS}=(V_{OS1} + V_{OS2})/2 to the OVPCOF[4:0] bits. The calibration is finished.
        If (V_{OS1} + V_{OS2})/2 is not integral, discard the decimal. Residue V_{OS}=V_{OUT} - V_{IN}

Serial Interface Module – SIM

The device contains a Serial Interface Module, which includes both the four line SPI interface and the two line I²C interface types, to allow an easy method of communication with external peripheral hardware. Having relatively simple communication protocols, these serial interface types allow the microcontroller to interface to external SPI or I²C based hardware such as sensors, Flash memory, etc. As both interface types share the same pins and registers, the choice of whether the SPI or I²C type is used is made using the SIM operating mode control bits, named SIM2~SIM0, in the SIMC0 register. These pull-high resistors of the SIM pin-shared I/O pins are selected using pull-high control registers when the SIM function is enabled and the corresponding pins are used as SIM input pins.

SPI Interface

The SPI interface is often used to communicate with external peripheral devices such as sensors, Flash memory devices etc. Originally developed by Motorola, the four line SPI interface is a synchronous serial data interface that has a relatively simple communication protocol simplifying the programming requirements when communicating with external hardware devices.

The communication is full duplex and operates as a slave/master type, where the device can be either master or slave. Although the SPI interface specification can control multiple slave devices from a single master, but this device is provided only one $\overline{\text{SCS}}$ pin. If the master needs to control multiple slave devices from a single master, the master can use I/O pin to select the slave devices.
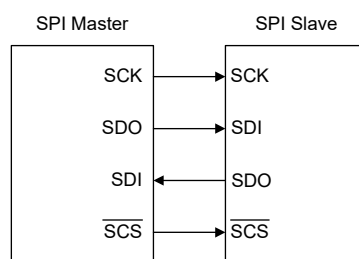
SPI Master/Slave Connection

SPI Interface Operation

The SPI interface is a full duplex synchronous serial data link. It is a four line interface with pin names SDI, SDO, SCK and $\overline{\text{SCS}}$. Pins SDI and SDO are the Serial Data Input and Serial Data Output lines; SCK is the Serial Clock line and $\overline{\text{SCS}}$ is the Slave Select line. As the SPI interface pins are pin-shared with normal I/O pins and with the I²C function pins, the SPI interface must first be enabled by setting the correct bits in the SIMC0 and SIMC2 registers. The SPI can be disabled or enabled using the SIMEN bit in the SIMC0 register. Communication between devices connected to the SPI interface is carried out in a slave/master mode with all data transfer initiations being implemented by the master. The Master also controls the clock signal. As the device only contains a single $\overline{\text{SCS}}$ pin only one slave device can be utilized. The $\overline{\text{SCS}}$ pin is controlled by software, set CSEN bit to "1" to enable $\overline{\text{SCS}}$ pin function, set CSEN bit to "0" the $\overline{\text{SCS}}$ pin will be floating state.
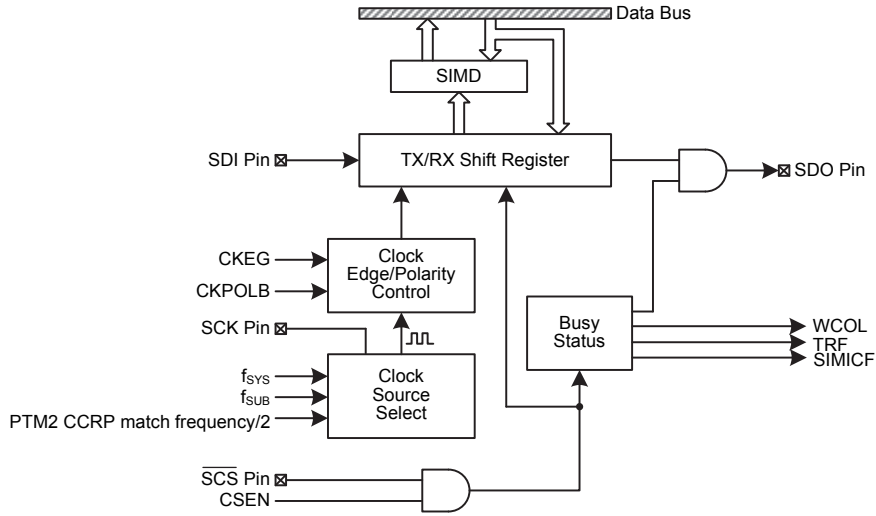
SPI Block Diagram

The SPI function in the device offers the following features:

- Full duplex synchronous data transfer

- Both Master and Slave modes

- LSB first or MSB first data transmission modes

- Transmission complete flag

- Rising or falling active clock edge

The status of the SPI interface pins is determined by a number of factors such as whether the device is in the master or slave mode and upon the condition of certain control bits such as CSEN and SIMEN.

SPI Registers

There are three internal registers which control the overall operation of the SPI interface. These are the SIMD data register and two registers SIMC0 and SIMC2. Note that the SIMC1 register is only used by the I^2C interface.

Register Name	Bit							
	7	6	5	4	3	2	1	0
SIMC0	SIM2	SIM1	SIM0	—	SIMDEB1	SIMDEB0	SIMEN	SIMICF
SIMD	D7	D6	D5	D4	D3	D2	D1	D0
SIMC2	D7	D6	CKPOLB	CKEG	MLS	CSEN	WCOL	TRF

SIM Register List

The SIMD register is used to store the data being transmitted and received. The same register is used by both the SPI and I^2C functions. Before the device writes data to the SPI bus, the actual data to be transmitted must be placed in the SIMD register. After the data is received from the SPI bus, the device can read it from the SIMD register. Any transmission or reception of data from the SPI bus must be made via the SIMD register.

- **SIMD Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x" unknown

There are two control registers for the SPI interface, SIMC0 and SIMC2. Note that the SIMC2 register also has the name SIMA which is used by the I²C function. The SIMC1 register is not used by the SPI function, only by the I²C function. Register SIMC0 is used to control the enable/disable function and to set the data transmission clock frequency. Although not connected with the SPI function, the SIMC0 register is also used to control the Peripheral Clock Prescaler. Register SIMC2 is used for other control functions such as LSB/MSB selection, write collision flag etc.

- **SIMC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	SIM2	SIM1	SIM0	—	SIMDEB1	SIMDEB0	SIMEN	SIMICF
R/W	R/W	R/W	R/W	—	R/W	R/W	R/W	R/W
POR	1	1	1	—	0	0	0	0

Bit 7~5   **SIM2~SIM0**: SIM Operating Mode Control
   000: SPI master mode; SPI clock is $f_{SYS}/4$
   001: SPI master mode; SPI clock is $f_{SYS}/16$
   010: SPI master mode; SPI clock is $f_{SYS}/64$
   011: SPI master mode; SPI clock is f_{SUB}
   100: SPI master mode; SPI clock is PTM2 CCRP match frequency/2
   101: SPI slave mode
   110: I²C slave mode
   111: Unused

These bits setup the overall operating mode of the SIM function. As well as selecting if the I²C or SPI function, they are used to control the SPI Master/Slave selection and the SPI Master clock frequency. The SPI clock is a function of the system clock but can also be chosen to be sourced from the PTM2. If the SPI Slave Mode is selected then the clock will be supplied by an external Master device.

Bit 4   Unimplemented, read as "0"

Bit 3~2   **SIMDEB[1:0]**: I²C Debounce Time Selection
The SIMDEB[1:0] bits are of no use in SPI mode of SIM, please ignore these selection bits when operateing in SPI mode.

Bit 1   **SIMEN**: SIM Control
   0: Disable
   1: Enable

The bit is the overall on/off control for the SIM interface. When the SIMEN bit is cleared to zero to disable the SIM interface, the SDI, SDO, SCK and $\overline{SCS}$, or SDA and SCL lines will be in a floating condition and the SIM operating current will be reduced to a minimum value. When the bit is high the SIM interface is enabled. The SIM configuration option must have first enabled the SIM interface for this bit to be effective. If the SIM is configured to operate as an SPI interface via the SIM2~SIM0 bits, the contents of the SPI control registers will remain at the previous settings when the SIMEN bit changes from low to high and should therefore be first initialised by the application program. If the SIM is configured to operate as an I²C interface via the SIM2~SIM0 bits and the SIMEN bit changes from low to high, the contents of the I²C control bits such as HTX and TXAK will remain at the previous settings and should therefore be first initialised by the application program while the relevant I²C flags such as HCF, HAAS, HBB, SRW and RXAK will be set to their default states.

Bit 0   **SIMICF**: SIM SPI Incomplete Flag
   0: SIM SPI incompleted is not occurred
   1: SIM SPI incompleted is occurred

The SIMICF bit is determined by $\overline{SCS}$ pin. When $\overline{SCS}$ pin is set high, it will clear the SPI counter. Meanwhile, the interrupt is occurred and the incomplete flag, SIMICF, is set high.

- **SIMC2 Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	CKPOLB	CKEG	MLS	CSEN	WCOL	TRF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **D7~D6**: Undefined bit

This bit can be read or written by user software program.

Bit 5   **CKPOLB**: Determines the Base Condition of the Clock Line

     0: The SCK line will be high when the clock is inactive
     1: The SCK line will be low when the clock is inactive

The CKPOLB bit determines the base condition of the clock line, if the bit is high, then the SCK line will be low when the clock is inactive. When the CKPOLB bit is low, then the SCK line will be high when the clock is inactive.

Bit 4   **CKEG**: Determines SPI SCK Active Clock Edge Type

CKPOLB=0
     0: SCK is high base level and data capture at SCK rising edge
     1: SCK is high base level and data capture at SCK falling edge
CKPOLB=1
     0: SCK is low base level and data capture at SCK falling edge
     1: SCK is low base level and data capture at SCK rising edge

The CKEG and CKPOLB bits are used to setup the way that the clock signal outputs and inputs data on the SPI bus. These two bits must be configured before data transfer is executed otherwise an erroneous clock edge may be generated. The CKPOLB bit determines the base condition of the clock line, if the bit is high, then the SCK line will be low when the clock is inactive. When the CKPOLB bit is low, then the SCK line will be high when the clock is inactive. The CKEG bit determines active clock edge type which depends upon the condition of CKPOLB bit.

Bit 3   **MLS**: SPI Data Shift Order

     0: LSB
     1: MSB

This is the data shift select bit and is used to select how the data is transferred, either MSB or LSB first. Setting the bit high will select MSB first and low for LSB first.

Bit 2   **CSEN**: SPI $\overline{SCS}$ Pin Control

     0: Disable
     1: Enable

The CSEN bit is used as an enable/disable for the $\overline{SCS}$ pin. If this bit is low, then the $\overline{SCS}$ pin will be disabled and placed into a floating condition. If the bit is high the $\overline{SCS}$ pin will be enabled and used as a select pin.

Bit 1   **WCOL**: SPI Write Collision Flag

     0: No collision
     1: Collision

The WCOL flag is used to detect if a data collision has occurred. If this bit is high it means that data has been attempted to be written to the SIMD register during a data transfer operation. This writing operation will be ignored if data is being transferred. The bit can be cleared by the application program.

Bit 0   **TRF**: SPI Transmit/Receive Complete Flag

     0: Data is being transferred
     1: SPI data transmission is completed

The TRF bit is the Transmit/Receive Complete flag and is set high automatically when an SPI data transmission is completed, but must cleared to zero by the application program. It can be used to generate an interrupt.

SPI Communication

After the SPI interface is enabled by setting the SIMEN bit high, then in the Master Mode, when data is written to the SIMD register, transmission/reception will begin simultaneously. When the data transfer is complete, the TRF flag will be set automatically, but must be cleared using the application program. In the Slave Mode, when the clock signal from the master has been received, any data in the SIMD register will be transmitted and any data on the SDI pin will be shifted into the SIMD register. The master should output an $\overline{SCS}$ signal to enable the slave device before a clock signal is provided. The slave data to be transferred should be well prepared at the appropriate moment relative to the $\overline{SCS}$ signal depending upon the configurations of the CKPOLB bit and CKEG bit. The accompanying timing diagram shows the relationship between the slave data and $\overline{SCS}$ signal for various configurations of the CKPOLB and CKEG bits.

The SPI will continue to function in certain IDLE Modes in which the clock source used by the SPI interface is still active.
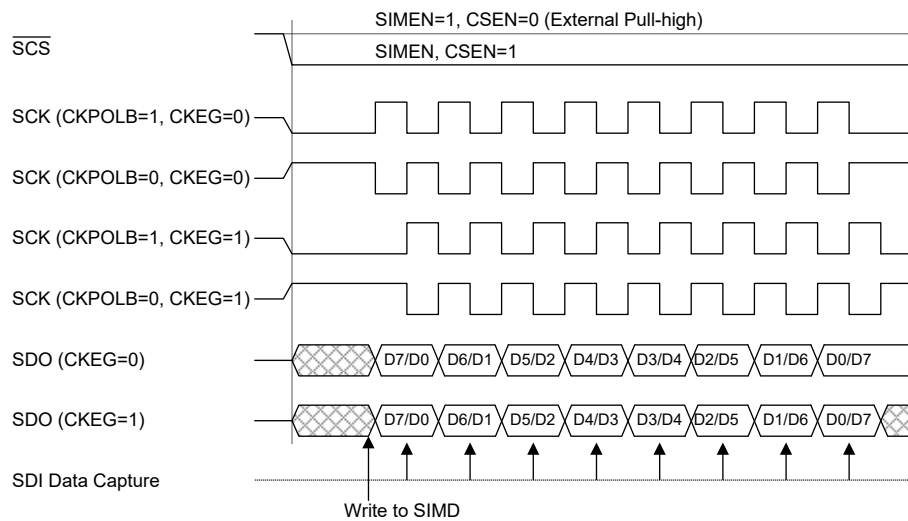
SPI Master Mode Timing

SPI Slave Mode Timing – CKEG=0

SCS

SCK (CKPOLB=1)

SCK (CKPOLB=0)

SDO   D7/D0 D6/D1 D5/D2 D4/D3 D3/D4 D2/D5 D1/D6 D0/D7

SDI Data Capture
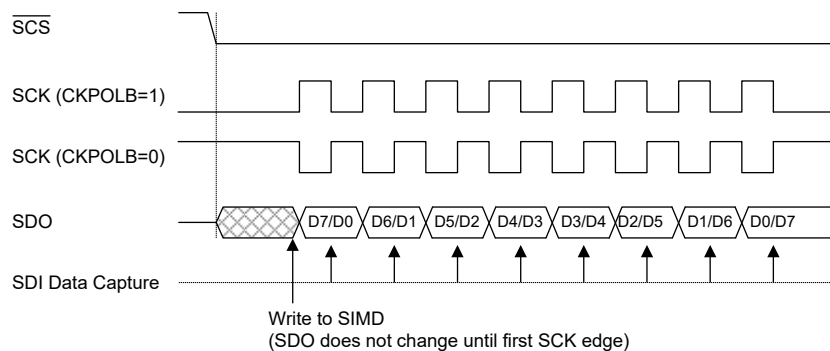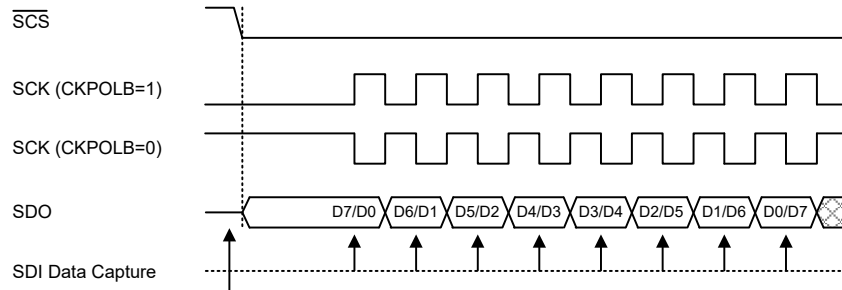
Write to SIMD
(SDO changes as soon as writing occurs; SDO is floating if SCS=1)

Note: For SPI slave mode, if SIMEN=1 and CSEN=0, SPI is always
enabled and ignores the SCS level.

SPI Slave Mode Timing – CKEG=1
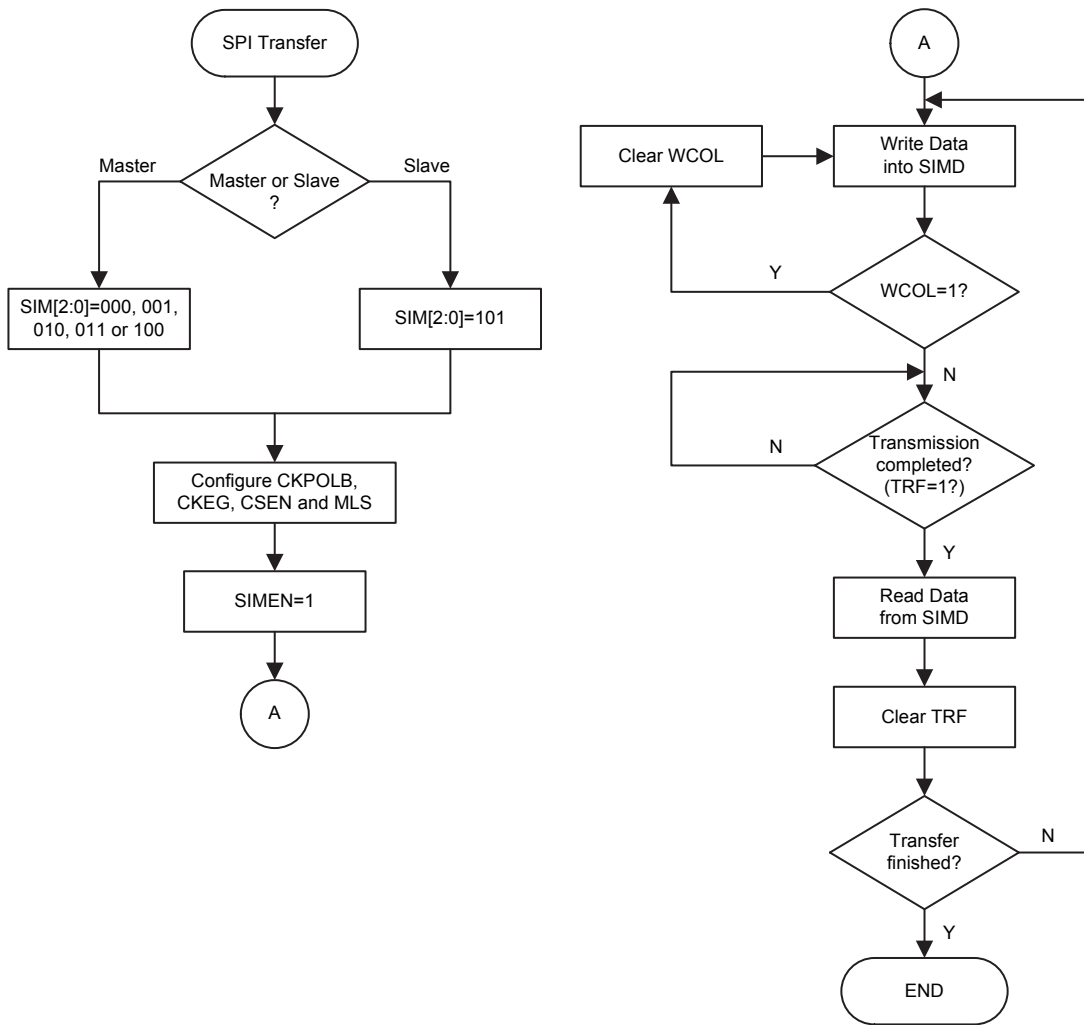
SPI Transfer Control Flowchart

I²C Interface

The I²C interface is used to communicate with external peripheral devices such as sensors etc. Originally developed by Philips, it is a two line low speed serial interface for synchronous serial data transfer. The advantage of only two lines for communication, relatively simple communication protocol and the ability to accommodate multiple devices on the same bus has made it an extremely popular interface type for many applications.

I²C Master/Slave Bus Connection
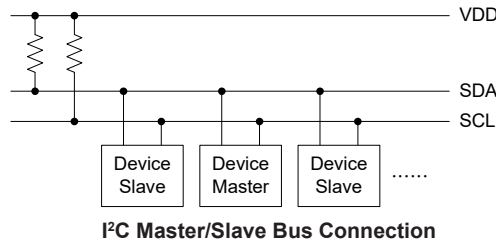
I²C Interface Operation

The I²C serial interface is a two line interface, a serial data line, SDA, and serial clock line, SCL. As many devices may be connected together on the same bus, their outputs are both open drain types. For this reason it is necessary that external pull-high resistors are connected to these outputs. Note that no chip select line exists, as each device on the I²C bus is identified by a unique address which will be transmitted and received on the I²C bus.

When two devices communicate with each other on the bidirectional I²C bus, one is known as the master device and one as the slave device. Both master and slave can transmit and receive data; however, it is the master device that has overall control of the bus. For the device, which only operate in slave mode, there are two methods of transferring data on the I²C bus, the slave transmit mode and the slave receive mode. The pull-up control function pin-shared with SCL/SDA pin is still applicable even if I²C device is activated and the related internal pull-up register could be controlled by its corresponding pull-up control register.

I²C Block Diagram
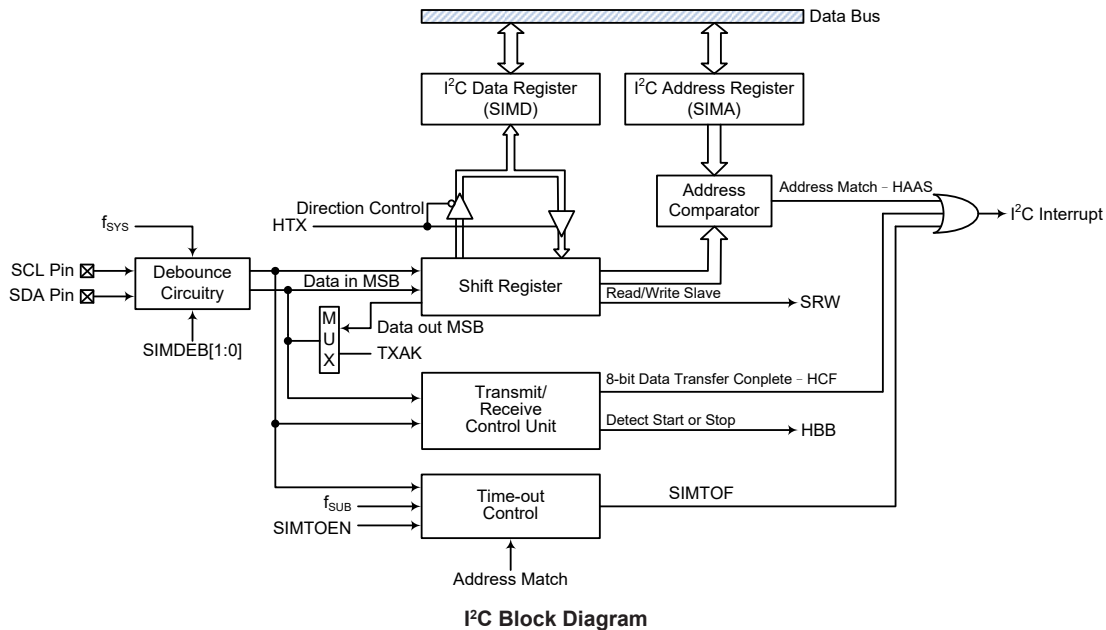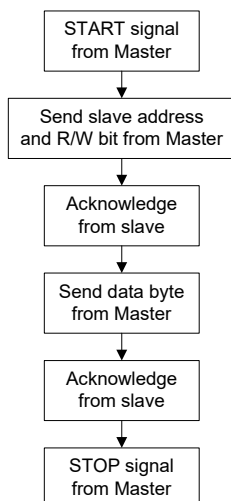
I²C Registers

There are three control registers associated with the I²C bus, SIMC0, SIMC1 and SIMTOC, one address register, SIMA and one data register, SIMD. The SIMD register, which is shown in the above SPI section, is used to store the data being transmitted and received on the I²C bus. Note that the SIMA register also has the name SIMC2 when the register is used for the SPI function. Bit SIMEN and bits SIM2~SIM0 in register SIMC0 are used by the I²C interface. The SIMTOC register is used for I²C time-out control.

Register Name	Bit							
	7	6	5	4	3	2	1	0
SIMC0	SIM2	SIM1	SIM0	—	SIMDEB1	SIMDEB0	SIMEN	SIMICF
SIMC1	HCF	HAAS	HBB	HTX	TXAK	SRW	IAMWU	RXAK
SIMD	D7	D6	D5	D4	D3	D2	D1	D0
SIMA	A6	A5	A4	A3	A2	A1	A0	D0
SIMTOC	SIMTOEN	SIMTOF	SIMTOS5	SIMTOS4	SIMTOS3	SIMTOS2	SIMTOS1	SIMTOS0

I²C Register List

- **SIMC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	SIM2	SIM1	SIM0	—	SIMDEB1	SIMDEB0	SIMEN	SIMICF
R/W	R/W	R/W	R/W	—	R/W	R/W	R/W	R/W
POR	1	1	1	—	0	0	0	0

Bit 7~5   **SIM2~SIM0**: SIM Operating Mode Control
           000: SPI master mode; SPI clock is $f_{SYS}/4$
           001: SPI master mode; SPI clock is $f_{SYS}/16$
           010: SPI master mode; SPI clock is $f_{SYS}/64$
           011: SPI master mode; SPI clock is f_{SUB}
           100: SPI master mode; SPI clock is PTM2 CCRP match frequency/2
           101: SPI slave mode
           110: I²C slave mode
           111: Unused

These bits setup the overall operating mode of the SIM function. As well as selecting if the I²C or SPI function, they are used to control the SPI Master/Slave selection and the SPI Master clock frequency. The SPI clock is a function of the system clock but can also be chosen to be sourced from the PTM2. If the SPI Slave Mode is selected then the clock will be supplied by an external Master device.

Bit 4   Unimplemented, read as "0"

Bit 3~2   **SIMDEB1~SIMDEB0**: I²C Debounce Time Selection
               00: No debounce
               01: 2 system clock debounce
               1x: 4 system clock debounce

Bit 1   **SIMEN**: SIM Control
               0: Disable
               1: Enable

               The bit is the overall on/off control for the SIM interface. When the SIMEN bit is
               cleared to zero to disable the SIM interface, the SDI, SDO, SCK and $\overline{SCS}$, or SDA
               and SCL lines will be in a floating condition and the SIM operating current will be
               reduced to a minimum value. When the bit is high the SIM interface is enabled. The
               SIM configuration option must have first enabled the SIM interface for this bit to be
               effective. If the SIM is configured to operate as an SPI interface via the SIM2~SIM0
               bits, the contents of the SPI control registers will remain at the previous settings when
               the SIMEN bit changes from low to high and should therefore be first initialised by
               the application program. If the SIM is configured to operate as an I²C interface via the
               SIM2~SIM0 bits and the SIMEN bit changes from low to high, the contents of the I²C
               control bits such as HTX and TXAK will remain at the previous settings and should
               therefore be first initialised by the application program while the relevant I²C flags
               such as HCF, HAAS, HBB, SRW and RXAK will be set to their default states.

Bit 0   **SIMICF**: SIM SPI Incomplete Flag

               SIMICF is of no use in I²C mode of SIM, please ignore this flag when operate in I²C
               mode.

- **SIMC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	HCF	HAAS	HBB	HTX	TXAK	SRW	IAMWU	RXAK
R/W	R	R	R	R/W	R/W	R	R/W	R
POR	1	0	0	0	0	0	0	1

Bit 7   **HCF**: I²C Bus Data Transfer Completion Flag
               0: Data is being transferred
               1: Completion of an 8-bit data transfer

               The HCF flag is the data transfer flag. This flag will be zero when data is being
               transferred. Upon completion of an 8-bit data transfer the flag will go high and an
               interrupt will be generated.

Bit 6   **HAAS**: I²C Bus Address Match Flag
               0: Not address match
               1: Address match

               The HAAS flag is the address match flag. This flag is used to determine if the slave
               device address is the same as the master transmit address. If the addresses match then
               this bit will be high, if there is no match then the flag will be low.

Bit 5   **HBB**: I²C Bus Busy Flag
               0: I²C Bus is not busy
               1: I²C Bus is busy

               The HBB flag is the I²C busy flag. This flag will be "1" when the I²C bus is busy which
               will occur when a START signal is detected. The flag will be cleared to zero when the
               bus is free which will occur when a STOP signal is detected.

Bit 4   **HTX**: Select I²C Slave Device is Transmitter or Receiver
               0: Slave device is the receiver
               1: Slave device is the transmitter

Bit 3　　　**TXAK**: I²C Bus Transmit Acknowledge Flag

　　　　0: Slave send acknowledge flag

　　　　1: Slave do not send acknowledge flag

The TXAK bit is the transmit acknowledge flag. After the slave device receipt of 8-bit of data, this bit will be transmitted to the bus on the 9th clock from the slave device. The slave device must always set TXAK bit to "0" before further data is received.

Bit 2　　　**SRW**: I²C Slave Read/Write Flag

　　　　0: Slave device should be in receive mode

　　　　1: Slave device should be in transmit mode

The SRW flag is the I²C Slave Read/Write flag. This flag determines whether the master device wishes to transmit or receive data from the I²C bus. When the transmitted address and slave address is match, that is when the HAAS flag is set high, the slave device will check the SRW flag to determine whether it should be in transmit mode or receive mode. If the SRW flag is high, the master is requesting to read data from the bus, so the slave device should be in transmit mode. When the SRW flag is zero, the master will write data to the bus, therefore the slave device should be in receive mode to read this data.

Bit 1　　　**IAMWU**: I²C Address Match Wake Up Function Control

　　　　0: Disable

　　　　1: Enable.

This bit should be set to 1 to enable the I²C address match wake up from the SLEEP or IDLE Mode. If the IAMWU bit has been set before entering either the SLEEP or IDLE mode to enable the I²C address match wake up, then this bit must be cleared by the application program after wake-up to ensure correct device operation.

Bit 0　　　**RXAK**: I²C Bus Receive Acknowledge Flag

　　　　0: Slave receives acknowledge flag

　　　　1: Slave does not receive acknowledge flag

The RXAK flag is the receiver acknowledge flag. When the RXAK flag is "0", it means that a acknowledge signal has been received at the 9th clock, after 8 bits of data have been transmitted. When the slave device in the transmit mode, the slave device checks the RXAK flag to determine if the master receive wishes to receive the next byte. The slave transmitter will therefore continue sending out data until the RXAK flag is "1". When this occurs, the slave transmitter will release the SDA line to allow the master to send a STOP signal to release the I²C bus.

The SIMD register is used to store the data being transmitted and received. The same register is used by both the SPI and I²C functions. Before the device write data to the I²C bus, the actual data to be transmitted must be placed in the SIMD register. After the data is received from the I²C bus, the device can read it from the SIMD register. Any transmission or reception of data from the I²C bus must be made via the SIMD register.

- **SIMD Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x" unknown

- **SIMA Register**

Bit	7	6	5	4	3	2	1	0
Name	A6	A5	A4	A3	A2	A1	A0	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~1　　**A6~A0**: I²C Slave address

A6~A0 is the I²C slave address bit 6~bit 0.

The SIMA register is also used by the SPI interface but has the name SIMC2. The SIMA register is the location where the 7-bit slave address of the slave device is stored. Bit 7~Bit 1 of the SIMA register define the device slave address. Bit 0 is not defined.

When a master device, which is connected to the I²C bus, sends out an address, which matches the slave address in the SIMA register, the slave device will be selected. Note that the SIMA register is the same register address as SIMC2 which is used by the SPI interface.

Bit 0   Undefined bit

This bit can be read or written by user software program.

- **SIMTOC Register**

Bit	7	6	5	4	3	2	1	0
Name	SIMTOEN	SIMTOF	SIMTOS5	SIMTOS4	SIMTOS3	SIMTOS2	SIMTOS1	SIMTOS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7   **SIMTOEN**: I²C interface Time-out control
         0: Disable
         1: Enable

Bit 6   **SIMTOF**: I²C interface Time-out flag
         0: No occurred
         1: Occurred
         The SIMTOF flag is set by the time-out circuitry when the time-out event occurs and cleared by software program.

Bit 5~0   **SIMTOS5~SIMTOS0**: I²C interface Time-out period selection
         The I²C Time-Out clock source is $f_{SUB}/32$.
         The I²C Time-Out time is $([SIMTOS5:SIMTOS0] + 1) \times (32/f_{SUB})$

I²C Bus Communication

Communication on the I²C bus requires four separate steps, a START signal, a slave device address transmission, a data transmission and finally a STOP signal. When a START signal is placed on the I²C bus, all devices on the bus will receive this signal and be notified of the imminent arrival of data on the bus. The first seven bits of the data will be the slave address with the first bit being the MSB. If the address of the slave device matches that of the transmitted address, the HAAS bit in the SIMC1 register will be set and an I²C interrupt will be generated. After entering the interrupt service routine, the slave device must first check the condition of the HAAS bit and SIMTOF bit to determine whether the interrupt source originates from an address match or from the completion of an 8-bit data transfer or from the I²C communication time-out. During a data transfer, note that after the 7-bit slave address has been transmitted, the following bit, which is the 8th bit, is the read/write bit whose value will be placed in the SRW bit. This bit will be checked by the slave device to determine whether to go into transmit or receive mode. Before any transfer of data to or from the I²C bus, the microcontroller must initialise the bus, the following are steps to achieve this:

- Step 1
 Set the SIM2~SIM0 bits to "110" and the SIMEN bits to "1" in the SIMC0 register to enable the I²C bus.

- Step 2
 Write the slave address to the I²C bus address register SIMA.

- Step 3
 Set the interrupt enable bit SIME to enable the SIM interrupt.
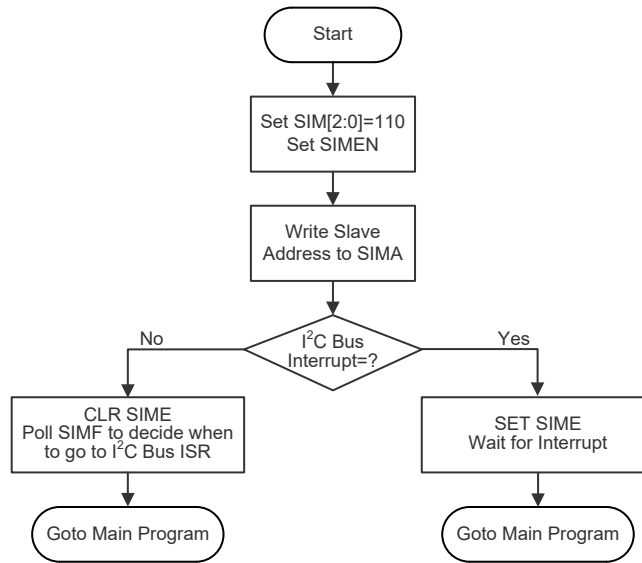
I²C Bus Initialisation Flow Chart

I²C Bus Start Signal

The START signal can only be generated by the master device connected to the I²C bus and not by the slave device. This START signal will be detected by all devices connected to the I²C bus. When detected, this indicates that the I²C bus is busy and therefore the HBB bit will be set. A START condition occurs when a high to low transition on the SDA line takes place when the SCL line remains high.

Slave Address

The transmission of a START signal by the master will be detected by all devices on the I²C bus. To determine which slave device the master wishes to communicate with, the address of the slave device will be sent out immediately following the START signal. All slave devices, after receiving this 7-bit address data, will compare it with their own 7-bit slave address. If the address sent out by the master matches the internal address of the microcontroller slave device, then an internal I²C bus interrupt signal will be generated. The next bit following the address, which is the 8th bit, defines the read/write status and will be saved to the SRW bit of the SIMC1 register. The slave device will then transmit an acknowledge bit, which is a low level, as the 9th bit. The slave device will also set the status flag HAAS when the addresses match.

As an I²C bus interrupt can come from three sources, when the program enters the interrupt subroutine, the HAAS bit and SIMTOF bit should be examined to see whether the interrupt source has come from a matching slave address or from the completion of a data byte transfer or from the I²C communication time-out. When a slave address is matched, the device must be placed in either the transmit mode and then write data to the SIMD register, or in the receive mode where it must implement a dummy read from the SIMD register to release the SCL line.

I²C Bus Read/Write Signal

The SRW bit in the SIMC1 register defines whether the slave device wishes to read data from the I²C bus or write data to the I²C bus. The slave device should examine this bit to determine if it is to be a transmitter or a receiver. If the SRW flag is "1" then this indicates that the master device wishes to read data from the I²C bus, therefore the slave device must be setup to send data to the I²C bus as a transmitter. If the SRW flag is "0" then this indicates that the master wishes to send data to the I²C bus, therefore the slave device must be setup to read data from the I²C bus as a receiver.

I²C Bus Slave Address Acknowledge Signal

After the master has transmitted a calling address, any slave device on the I²C bus, whose own internal address matches the calling address, must generate an acknowledge signal. The acknowledge signal will inform the master that a slave device has accepted its calling address. If no acknowledge signal is received by the master then a STOP signal must be transmitted by the master to end the communication. When the HAAS flag is high, the addresses have matched and the slave device must check the SRW flag to determine if it is to be a transmitter or a receiver. If the SRW flag is high, the slave device should be setup to be a transmitter so the HTX bit in the SIMC1 register should be set high. If the SRW flag is low, then the microcontroller slave device should be setup as a receiver and the HTX bit in the SIMC1 register should be cleared to zero.

I²C Bus Data and Acknowledge Signal

The transmitted data is 8-bit wide and is transmitted after the slave device has acknowledged receipt of its slave address. The order of serial bit transmission is the MSB first and the LSB last. After receipt of 8-bit of data, the receiver must transmit an acknowledge signal, level "0", before it can receive the next data byte. If the slave transmitter does not receive an acknowledge bit signal from the master receiver, then the slave transmitter will release the SDA line to allow the master to send a STOP signal to release the I²C Bus. The corresponding data will be stored in the SIMD register. If setup as a transmitter, the slave device must first write the data to be transmitted into the SIMD register. If setup as a receiver, the slave device must read the transmitted data from the SIMD register.

When the slave receiver receives the data byte, it must generate an acknowledge bit, known as TXAK, on the 9th clock. The slave device, which is setup as a transmitter will check the RXAK bit in the SIMC1 register to determine if it is to send another data byte, if not then it will release the SDA line and await the receipt of a STOP signal from the master.

S=Start (1 bit)
SA=Slave Address (7 bits)
SR=SRW bit (1 bit)
M=Slave device send acknowledge bit (1 bit)
D=Data (8 bits)
A=ACK (RXAK bit for transmitter, TXAK bit for receiver, 1 bit)
P=Stop (1 bit)

S	SA	SR	M	D	A	D	A	······	S	SA	SR	M	D	A	D	A	······	P
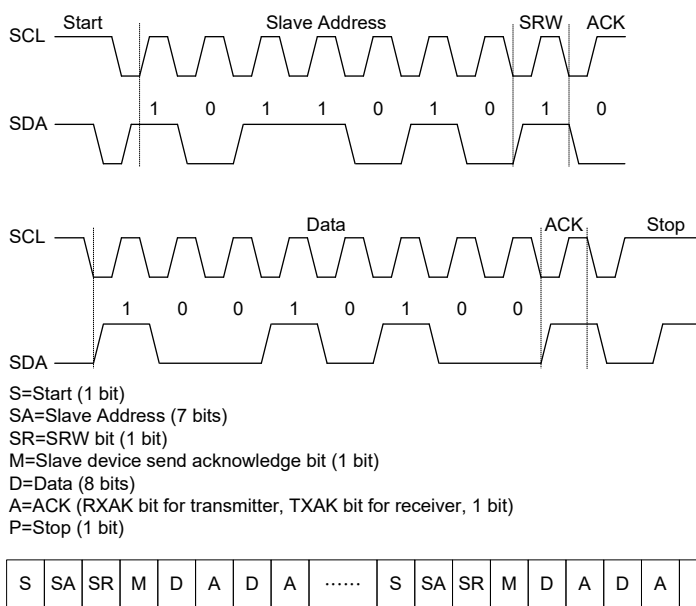
I²C Communication Timing Diagram

Note: *When a slave address is matched, the device must be placed in either the transmit mode and then write data to the SIMD register, or in the receive mode where it must implement a dummy read from the SIMD register to release the SCL line.
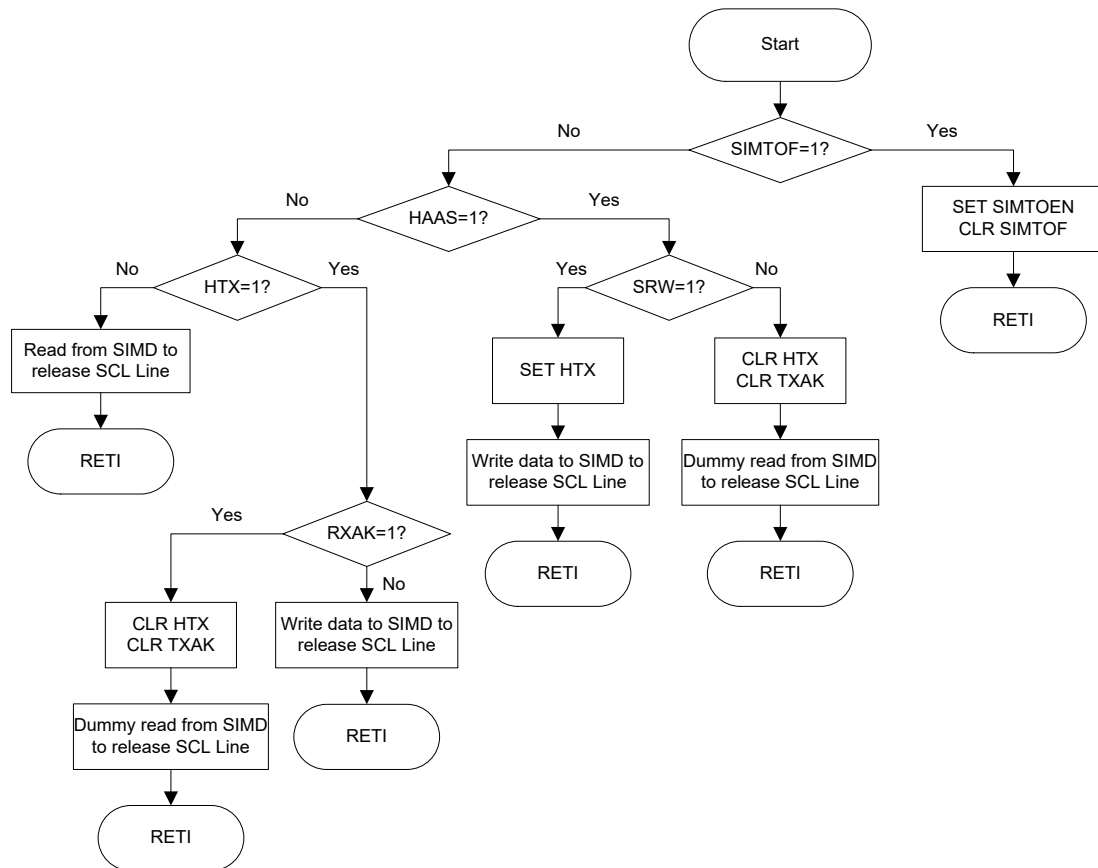
I²C Bus ISR Flow Chart

I²C Time Out function

In order to reduce the I²C lockup problem due to reception of erroneous clock sources, a time-out function is provided. If the clock source connected to the I²C bus is not received for a while, then the I²C circuitry and the SIMC1 register will be reset, the SIMTOF bit in the SIMTOC register will be set high after a certain time-out period. The Time Out function enable/disable and the time-out period are managed by the SIMTOC register.

I²C Time Out operation

The time-out counter starts to count on an I²C bus "START" & "address match" condition, and is cleared by an SCL falling edge. Before the next SCL falling edge arrives, if the time elapsed is greater than the time-out period specified by the SIMTOC register, then a time-out condition will occur. The time-out function will stop when an I²C "STOP" condition occurs. There are 64 time-out period selections which can be selected using the SIMTOS0~SIMTOS5 bits in the SIMTOC register.
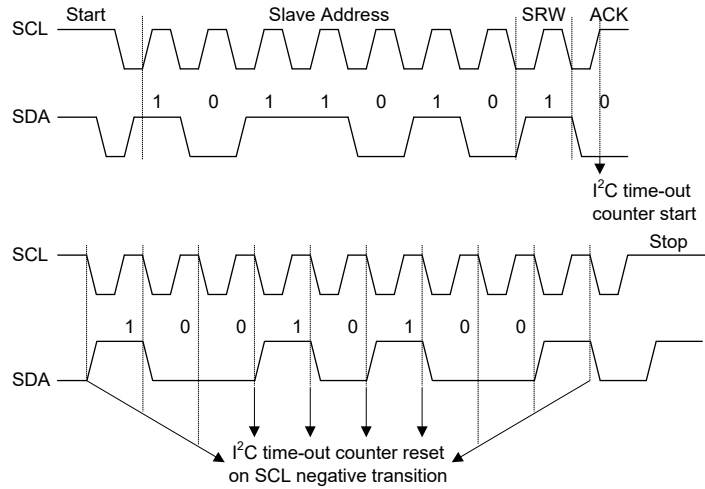
I²C Time-out Diagram

When an I²C time-out counter overflow occurs, the counter will stop and the SIMTOEN bit will be cleared to zero and the SIMTOF bit will be set high to indicate that a time-out condition has occurred. When an I²C time-out occurs, the I²C internal circuitry will be reset and the registers will be reset into the following condition:

Register	After I²C Time-out
SIMD, SIMA, SIMC0	No change
SIMC1	Reset to POR condition

I²C Registers after Time-out

Serial Peripheral Interface – SPIA

The device contains an independent SPI function. It is important not to confuse this independent SPI function with the additional one contained within the combined SIM function, which is described in another section of this datasheet. This independent SPI function will carry the name SPIA to distinguish it from the other one in the SIM.

The SPIA interface is often used to communicate with external peripheral devices such as sensors, Flash or EEPROM memory devices etc. Originally developed by Motorola, the four line SPIA interface is a synchronous serial data interface that has a relatively simple communication protocol simplifying the programming requirements when communicating with external hardware devices.

The communication is full duplex and operates as a slave/master type, where the device can be either master or slave. Although the SPIA interface specification can control multiple slave devices from a single master, however the device is provided with only one $\overline{SCSA}$ pin. If the master needs to control multiple slave devices from a single master, the master can use I/O pins to select the slave devices.

SPIA Interface Operation

The SPIA interface is a full duplex synchronous serial data link. It is a four line interface with pin names SDIA, SDOA, SCKA and $\overline{SCSA}$. Pins SDIA and SDOA are the Serial Data Input and Serial Data Output lines, the SCKA pin is the Serial Clock line and $\overline{SCSA}$ is the Slave Select line. As the SPIA interface pins are pin-shared with normal I/O pins, the SPIA interface must first be enabled by configuring the corresponding selection bits in the pin-shared function selection registers. The SPIA can be disabled or enabled using the SPIAEN bit in the SPIAC0 register. Communication between devices connected to the SPIA interface is carried out in a slave/master mode with all data transfer initiations being implemented by the master. The Master also controls the clock signal. As the device only contains a single $\overline{SCSA}$ pin only one slave device can be utilized.

The $\overline{SCSA}$ pin is controlled by the application program, set the SACSEN bit to "1" to enable the $\overline{SCSA}$ pin function and clear the SACSEN bit to "0" to place the $\overline{SCSA}$ pin into a floating state.
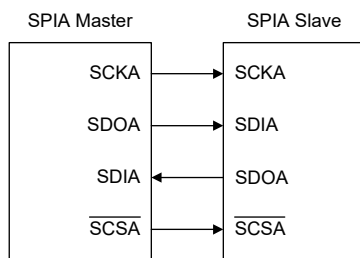
SPIA Master/Slave Connection

The SPIA function in the device offers the following features:

- Full duplex synchronous data transfer
- Both Master and Slave modes
- LSB first or MSB first data transmission modes
- Transmission complete flag
- Rising or falling active clock edge

The status of the SPIA interface pins is determined by a number of factors such as whether the device is in the master or slave mode and upon the condition of certain control bits such as SACSEN and SPIAEN.

SPIA Block Diagram
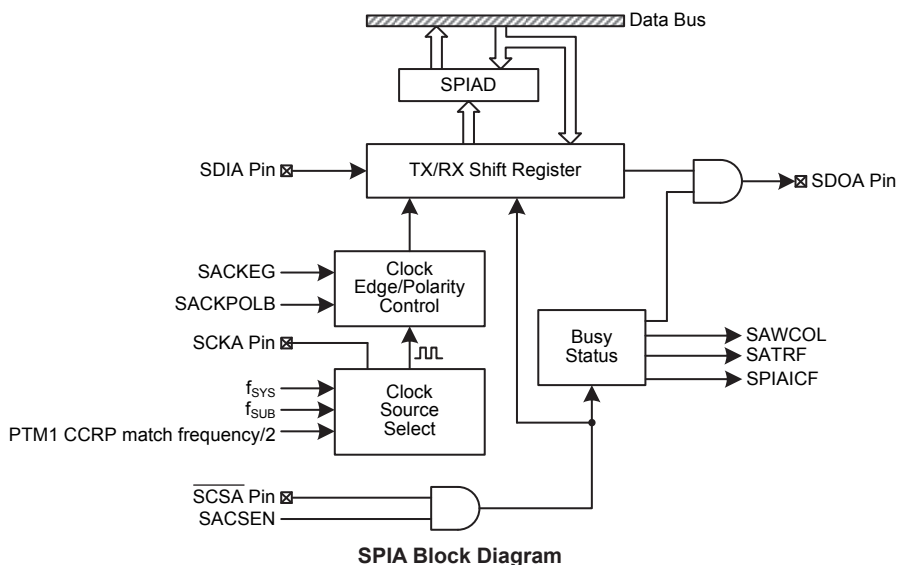
SPIA Registers

There are three internal registers which control the overall operation of the SPIA interface. These are the SPIAD data register and two control registers, SPIAC0 and SPIAC1.

Register Name	Bit							
	7	6	5	4	3	2	1	0
SPIAC0	SASPI2	SASPI1	SASPI0	—	—	—	SPIAEN	SPIAICF
SPIAC1	—	—	SACKPOLB	SACKEG	SAMLS	SACSEN	SAWCOL	SATRF
SPIAD	D7	D6	D5	D4	D3	D2	D1	D0

SPIA Register List

SPIA Data Register

The SPIAD register is used to store the data being transmitted and received. Before the device writes data to the SPIA bus, the actual data to be transmitted must be placed in the SPIAD register. After the data is received from the SPIA bus, the device can read it from the SPIAD register. Any transmission or reception of data from the SPIA bus must be made via the SPIAD register.

- **SPIAD Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x": unknown

Bit 7~0 **D7~D0**: SPIA Data Register bit 7~bit 0

SPIA Control Registers

There are also two control registers for the SPIA interface, SPIAC0 and SPIAC1. The SPIAC0 register is used to control the enable/disable function and to set the data transmission clock frequency. The SPIAC1 register is used for other control functions such as LSB/MSB selection, write collision flag etc.

- **SPIAC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	SASPI2	SASPI1	SASPI0	—	—	—	SPIAEN	SPIAICF
R/W	R/W	R/W	R/W	R/W	—	—	R/W	R/W
POR	1	1	1	—	—	—	0	0

Bit 7~5　　**SASPI2~SASPI0**: SPIA Operating Mode Control
　　　　　000: SPIA master mode; SPIA clock is fSYS/4
　　　　　001: SPIA master mode; SPIA clock is fSYS/16
　　　　　010: SPIA master mode; SPIA clock is fSYS/64
　　　　　011: SPIA master mode; SPIA clock is fSUB
　　　　　100: SPIA master mode; SPIA clock is PTM1 CCRP match frequency/2
　　　　　101: SPIA slave mode
　　　　　110: Undefined
　　　　　111: Undefined

These bits are used to control the SPIA Master/Slave selection and the SPIA Master clock frequency. The SPIA clock is a function of the system clock but can also be chosen to be sourced from PTM1 and f_{SUB}. If the SPIA Slave Mode is selected then the clock will be supplied by an external Master device.

Bit 4~2　　Unimplemented, read as "0"

Bit 1　　**SPIAEN**: SPIA Enable Control
　　　　　0: Disable
　　　　　1: Enable

The bit is the overall on/off control for the SPIA interface. When the SPIAEN bit is cleared to zero to disable the SPIA interface, the SDIA, SDOA, SCKA and $\overline{SCSA}$ lines will lose their SPIA function and the SPIA operating current will be reduced to a minimum value. When the bit is high the SPIA interface is enabled.

Bit 0　　**SPIAICF**: SPIA Incomplete Flag
　　　　　0: SPIA incomplete condition is not occurred
　　　　　1: SPIA incomplete condition is occured

This bit is only available when the SPIA is configured to operate in an SPIA slave mode. If the SPIA operates in the slave mode with the SPIAEN and SACSEN bits both being set to 1 but the $\overline{SCSA}$ line is pulled high by the external master device before the SPIA data transfer is completely finished, the SPIAICF bit will be set to 1 together with the SATRF bit. When this condition occurs, the corresponding interrupt will occur if the interrupt function is enabled. However, the SATRF bit will not be set to 1 if the SPIAICF bit is set to 1 by software application program.

- **SPIAC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	SACKPOLB	SACKEG	SAMLS	SACSEN	SAWCOL	SATRF
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

Bit 7~6　　Unimplemented, read as "0".

Bit 5　　**SACKPOLB**: SPIA Clock Line Base Condition Selection
　　　　　0: The SCKA line will be high when the clock is inactive
　　　　　1: The SCKA line will be low when the clock is inactive

The SACKPOLB bit determines the base condition of the clock line, if the bit is high, then the SCKA line will be low when the clock is inactive. When the SACKPOLB bit is low, then the SCKA line will be high when the clock is inactive.

Bit 4 **SACKEG**: SPIA SCKA Clock Active Edge Type Selection

    SACKPOLB=0

     0: SCKA has high base level with data capture on SCKA rising edge

     1: SCKA has high base level with data capture on SCKA falling edge

    SACKPOLB=1

     0: SCKA has low base level with data capture on SCKA falling edge

     1: SCKA has low base level with data capture on SCKA rising edge

    The SACKEG and SACKPOLB bits are used to setup the way that the clock signal outputs and inputs data on the SPIA bus. These two bits must be configured before a data transfer is executed otherwise an erroneous clock edge may be generated. The SACKPOLB bit determines the base condition of the clock line, if the bit is high, then the SCKA line will be low when the clock is inactive. When the SACKPOLB bit is low, then the SCKA line will be high when the clock is inactive. The SACKEG bit determines active clock edge type which depends upon the condition of the SACKPOLB bit.

Bit 3 **SAMLS**: SPIA Data Shift Order

    0: LSB first

    1: MSB first

    This is the data shift select bit and is used to select how the data is transferred, either MSB or LSB first. Setting the bit high will select MSB first and low for LSB first.

Bit 2 **SACSEN**: SPIA $\overline{SCSA}$ Pin Control

    0: Disable

    1: Enable

    The SACSEN bit is used as an enable/disable for the $\overline{SCSA}$ pin. If this bit is low, then the $\overline{SCSA}$ pin will be disabled and placed into a floating state. If the bit is high the $\overline{SCSA}$ pin will be enabled and used as a select pin.

Bit 1 **SAWCOL**: SPIA Write Collision Flag

    0: No collision

    1: Collision

    The SAWCOL flag is used to detect if a data collision has occurred. If this bit is high it means that data has been attempted to be written to the SPIAD register during a data transfer operation. This writing operation will be ignored if data is being transferred. The bit can be cleared by the application program.

Bit 0 **SATRF**: SPIA Transmit/Receive Complete Flag

    0: SPIA data is being transferred

    1: SPIA data transmission is completed

    The SATRF bit is the Transmit/Receive Complete flag and is set "1" automatically when an SPIA data transmission is completed, but must set to zero by the application program. It can be used to generate an interrupt.

SPIA Communication

After the SPIA interface is enabled by setting the SPIAEN bit high, then in the Master Mode, when data is written to the SPIAD register, transmission/reception will begin simultaneously. When the data transfer is complete, the SATRF flag will be set automatically, but must be cleared using the application program. In the Slave Mode, when the clock signal from the master has been received, any data in the SPIAD register will be transmitted and any data on the SDIA pin will be shifted into the SPIAD register.

The master should output an $\overline{SCSA}$ signal to enable the slave device before a clock signal is provided. The slave data to be transferred should be well prepared at the appropriate moment relative to the $\overline{SCSA}$ signal depending upon the configurations of the SACKPOLB bit and SACKEG bit. The accompanying timing diagram shows the relationship between the slave data and $\overline{SCSA}$ signal for various configurations of the SACKPOLB and SACKEG bits.
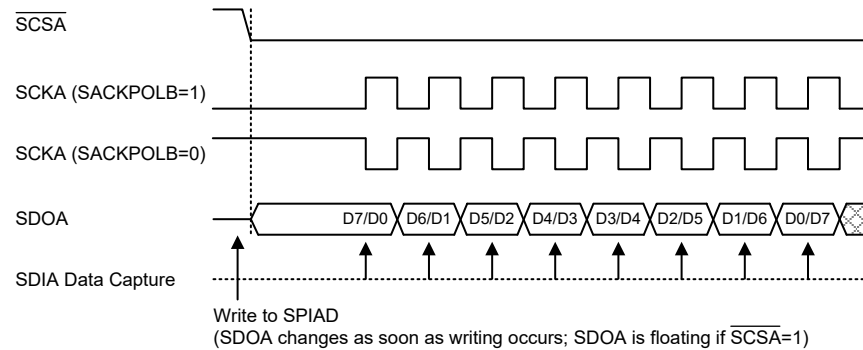
The SPIA will continue to function in special IDLE Modes if the clock source used by the SPIA interface is still active.
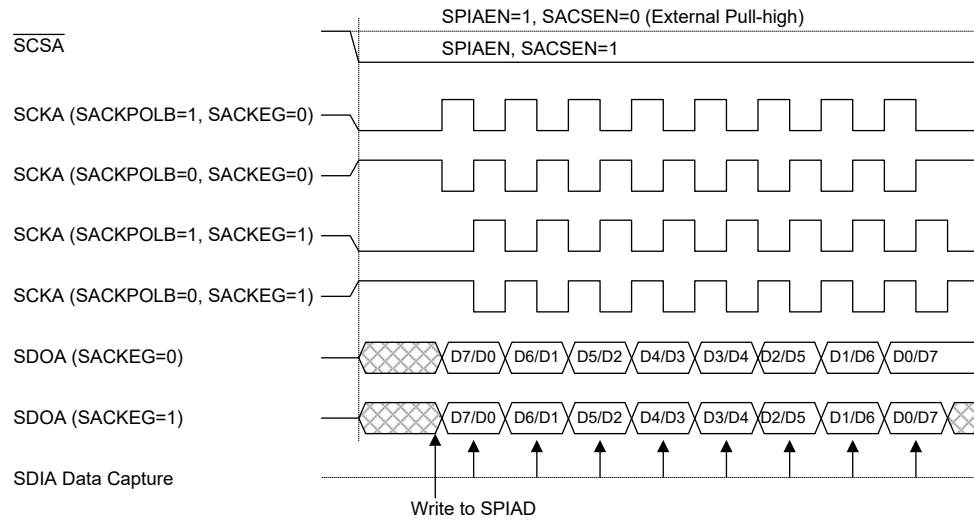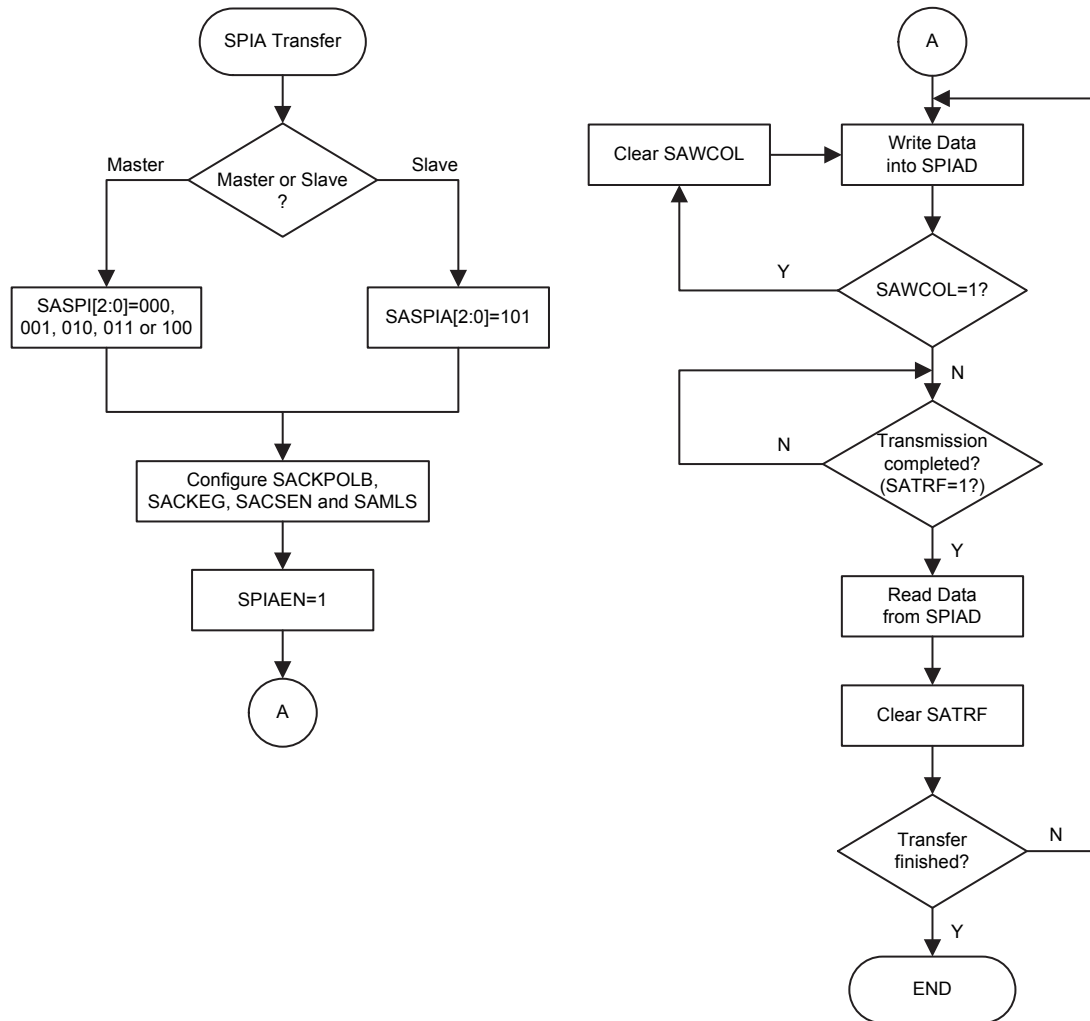

SPIA Master Mode Timing
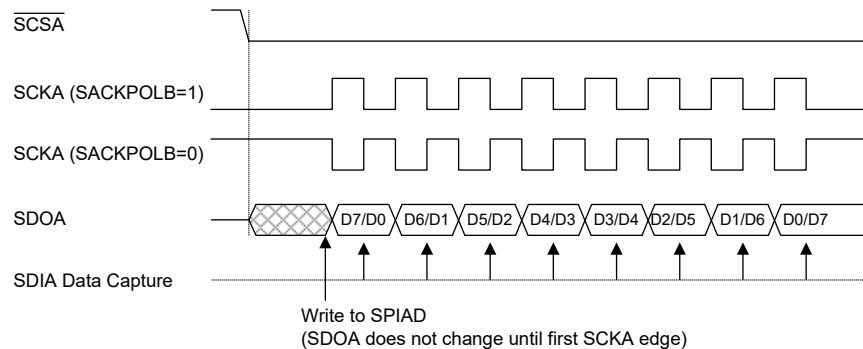
SPIA Slave Mode Timing – SACKEG=0

Note: For SPIA slave mode, if SPIAEN=1 and SACSEN=0, SPIA is always enabled and ignores the $\overline{SCSA}$ level.

SPIA Slave Mode Timing – SACKEG=1

SPIA Transfer Control Flowchart

SPIA Bus Enable/Disable

To enable the SPIA bus, set SACSEN=1 and $\overline{SCSA}$=0, then wait for data to be written into the SPIAD (TXRX buffer) register. For the Master Mode, after data has been written to the SPIAD (TXRX buffer) register, then transmission or reception will start automatically. When all the data has been transferred the SATRF bit should be set. For the Slave Mode, when clock pulses are received on SCKA, data in the TXRX buffer will be shifted out or data on SDIA will be shifted in.

If the SPIA bus is not used, the external lines SCKA, SDIA, SDOA, $\overline{SCSA}$ can be selected as general I/O pins or other pin-shared functions.

SPIA Operation

All communication is carried out using the 4-line interface for either Master or Slave Mode.

The SACSEN bit in the SPIAC1 register controls the overall function of the SPIA interface. Setting this bit high will enable the SPIA interface by allowing the $\overline{SCSA}$ line to be active, which can then be used to control the SPIA interface. If the SACSEN bit is low, the SPIA interface will be disabled and the $\overline{SCSA}$ line will be an I/O pin or the other functions and can therefore not be used for control of the SPIA interface. If the SACSEN bit and the SPIAEN bit in the SPIAC0 register are set high,

this will place the SDIA line in a floating condition and the SDOA line high. If in Master Mode the SCKA line will be either high or low depending upon the clock polarity selection bit SACKPOLB in the SPIAC1 register. If in Slave Mode the SCKA line will be in a floating condition. If SPIAEN is low then the bus will be disabled and $\overline{\text{SCSA}}$, SDIA, SDOA and SCKA will all become I/O pins or the other functions. In the Master Mode the Master will always generate the clock signal. The clock and data transmission will be initiated after data has been written into the SPIAD register. In the Slave Mode, the clock signal will be received from an external master device for both data transmission and reception. The following sequences show the order to be followed for data transfer in both Master and Slave Mode.

Master Mode

- Step 1

  Select the clock source and Master mode using the SASPI2~SASPI0 bits in the SPIAC0 control register.

- Step 2

  Setup the SACSEN bit and setup the SAMLS bit to choose if the data is MSB or LSB first, this must be same as the Slave device.

- Step 3

  Setup the SPIAEN bit in the SPIAC0 control register to enable the SPIA interface.

- Step 4

  For write operations: write the data to the SPIAD register, which will actually place the data into the TXRX buffer. Then use the SCKA and $\overline{\text{SCSA}}$ lines to output the data. After this go to step 5.

  For read operations: the data transferred in on the SDIA line will be stored in the TXRX buffer until all the data has been received at which point it will be latched into the SPIAD register.

- Step 5

  Check the SAWCOL bit if set high then a collision error has occurred so return to step 4. If equal to zero then go to the following step.

- Step 6

  Check the SATRF bit or wait for a SPIA serial bus interrupt.

- Step 7

  Read data from the SPIAD register.

- Step 8

  Clear SATRF.

- Step 9

  Go to step 4.

Slave Mode

- Step 1

  Select the SPIA Slave mode using the SASPI2~SASPI0 bits in the SPIAC0 control register.

- Step 2

  Setup the SACSEN bit and setup the SAMLS bit to choose if the data is MSB or LSB first, this setting must be the same with the Master device.

- Step 3

  Setup the SPIAEN bit in the SPIAC0 control register to enable the SPIA interface.

- Step 4

  For write operations: write the data to the SPIAD register, which will actually place the data into the TXRX buffer. Then wait for the master clock SCKA and $\overline{SCSA}$ signal. After this, go to step 5. For read operations: the data transferred in on the SDIA line will be stored in the TXRX buffer until all the data has been received at which point it will be latched into the SPIAD register.

- Step 5

  Check the SAWCOL bit if set high then a collision error has occurred so return to step 4. If equal to zero then go to the following step.

- Step 6

  Check the SATRF bit or wait for a SPIA serial bus interrupt.

- Step 7

  Read data from the SPIAD register.

- Step 8

  Clear SATRF.

- Step 9

  Go to step 4.

Error Detection

The SAWCOL bit in the SPIAC1 register is provided to indicate errors during data transfer. The bit is set by the SPIA serial Interface but must be cleared by the application program. This bit indicates a data collision has occurred which happens if a write to the SPIAD register takes place during a data transfer operation and will prevent the write operation from continuing.

UART Interfaces

The device contains up to two integrated full-duplex asynchronous serial communications UART interfaces that enable communication with external devices that contain a serial interface. Each UART function has many features and can transmit and receive data serially by transferring a frame of data with eight or nine data bits per transmission as well as being able to detect errors when the data is overwritten or incorrectly framed. Each UART function possesses its own internal interrupt which can be used to indicate when a reception occurs or when a transmission terminates.

The integrated UART functions contain the following features:

- Full-duplex, asynchronous communication
- 8 or 9 bits character length
- Even, odd or no parity options
- One or two stop bits
- Baud rate generator with 8-bit prescaler
- Parity, framing, noise and overrun error detection
- Support for interrupt on address detect (last character bit=1)
- Separately enabled transmitter and receiver
- 2-byte Deep FIFO Receive Data Buffer
- RXn pin wake-up function
- Transmit and receive interrupts

- Interrupts can be initialized by the following conditions:
  - Transmitter Empty
  - Transmitter Idle
  - Receiver Full
  - Receiver Overrun
  - Address Mode Detect
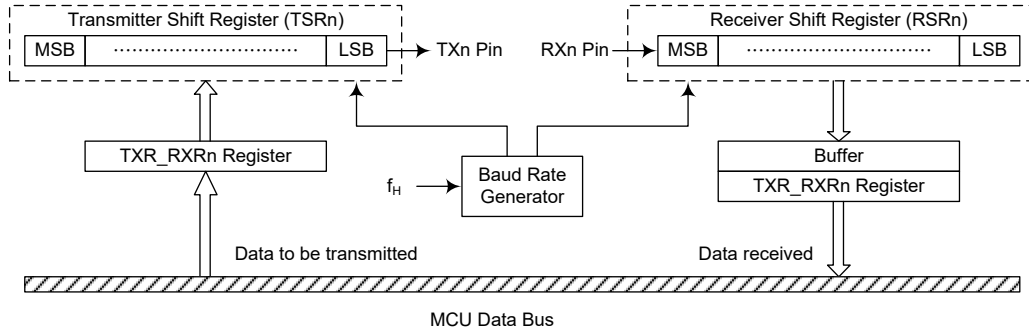
UARTn Data Transfer Block Diagram (n=0 ~ 1)

UARTn External Pins

To communicate with an external serial interface, the internal UARTn has two external pins known as TXn and RXn. The TXn and RXn pins are the UART transmitter and receiver pins respectively. The TXn and RXn pin function should first be selected by the corresponding pin-shared function selection register before the UARTn function is used. Along with the UARTENn bit, the TXENn and RXENn bits, if set, will setup these pins to their respective TXn output and RXn input conditions and disable any pull-high resistor option which may exist on the TXn and RXn pins. When the TXn or RXn pin function is disabled by clearing the UARTENn, TXENn or RXENn bit, the TXn or RXn pin will be placed into a floating state. At this time whether the internal pull-high resistor is connected to the TXn or RXn pin or not is determined by the corresponding I/O pull-high function control bit.

UARTn Data Transfer Scheme

The UARTn data transfer block diagram shows the overall data transfer structure arrangement for the UARTn. The actual data to be transmitted from the MCU is first transferred to the TXR_RXRn register by the application program. The data will then be transferred to the Transmit Shift Register from where it will be shifted out, LSB first, onto the TXn pin at a rate controlled by the Baud Rate Generator. Only the TXR_RXRn register is mapped onto the MCU Data Memory, the Transmit Shift Register is not mapped and is therefore inaccessible to the application program.

Data to be received by the UARTn is accepted on the external RXn pin, from where it is shifted in, LSB first, to the Receiver Shift Register at a rate controlled by the Baud Rate Generator. When the shift register is full, the data will then be transferred from the shift register to the internal TXR_RXRn register, where it is buffered and can be manipulated by the application program. Only the TXR_RXRn register is mapped onto the MCU Data Memory, the Receiver Shift Register is not mapped and is therefore inaccessible to the application program.

It should be noted that the actual register for data transmission and reception only exists as a single shared register in the Data Memory. This shared register known as the TXR_RXRn register is used for both data transmission and data reception.

UARTn Status and Control Registers

There are five control registers associated with the UARTn function. The UnSR, UnCR1 and UnCR2 registers control the overall function of the UARTn, while the BRGn register controls the Baud rate. The actual data to be transmitted and received on the serial interface is managed through the TXR_RXRn data register.

Register Name	Bit							
	7	6	5	4	3	2	1	0
UnSR	PERRn	NFn	FERRn	OERRn	RIDLEn	RXIFn	TIDLEn	TXIFn
UnCR1	UARTENn	BNOn	PRENn	PRTn	STOPSn	TXBRKn	RX8n	TX8n
UnCR2	TXENn	RXENn	BRGHn	ADDENn	WAKEn	RIEn	TIIEn	TEIEn
TXR_RXRn	TXRXn7	TXRXn6	TXRXn5	TXRXn4	TXRXn3	TXRXn2	TXRXn1	TXRXn0
BRGn	BRGn7	BRGn6	BRGn5	BRGn4	BRGn3	BRGn2	BRGn1	BRGn0

UARTn Register List (n=0 ~ 1)

- **UnSR Register**

The UnSR register is the status register for the UARTn, which can be read by the program to determine the present status of the UARTn. All flags within the UnSR register are read only. Further explanation on each of the flags is given below:

Bit	7	6	5	4	3	2	1	0
Name	PERRn	NFn	FERRn	OERRn	RIDLEn	RXIFn	TIDLEn	TXIFn
R/W	R	R	R	R	R	R	R	R
POR	0	0	0	0	1	0	1	1

Bit 7 **PERRn**: Parity error flag
0: No parity error is detected
1: Parity error is detected
The PERRn flag is the parity error flag. When this read only flag is "0", it indicates a parity error has not been detected. When the flag is "1", it indicates that the parity of the received word is incorrect. This error flag is applicable only if Parity mode (odd or even) is selected. The flag can also be cleared by a software sequence which involves a read to the status register UnSR followed by an access to the TXR_RXRn data register.

Bit 6 **NFn**: Noise flag
0: No noise is detected
1: Noise is detected
The NFn flag is the noise flag. When this read only flag is "0", it indicates no noise condition. When the flag is "1", it indicates that the UARTn has detected noise on the receiver input. The NFn flag is set during the same cycle as the RXIFn flag but will not be set in the case of as overrun. The NFn flag can be cleared by a software sequence which will involve a read to the status register UnSR followed by an access to the TXR_RXRn data register.

Bit 5 **FERRn**: Framing error flag
0: No framing error is detected
1: Framing error is detected
The FERRn flag is the framing error flag. When this read only flag is "0", it indicates that there is no framing error. When the flag is "1", it indicates that a framing error has been detected for the current character. The flag can also be cleared by a software sequence which will involve a read to the status register UnSR followed by an access to the TXR_RXRn data register.

Bit 4 **OERRn**: Overrun error flag

0: No overrun error is detected

1: Overrun error is detected

The OERRn flag is the overrun error flag which indicates when the receiver buffer has overflowed. When this read only flag is "0", it indicates that there is no overrun error. When the flag is "1", it indicates that an overrun error occurs which will inhibit further transfers to the TXR_RXRn receive data register. The flag is cleared by a software sequence, which is a read to the status register UnSR followed by an access to the TXR_RXRn data register.

Bit 3 **RIDLEn**: Receiver status

0: Data reception is in progress (Data being received)

1: No data reception is in progress (Receiver is idle)

The RIDLEn flag is the receiver status flag. When this read only flag is "0", it indicates that the receiver is between the initial detection of the start bit and the completion of the stop bit. When the flag is "1", it indicates that the receiver is idle. Between the completion of the stop bit and the detection of the next start bit, the RIDLEn bit is "1" indicating that the UARTn receiver is idle and the RXn pin stays in logic high condition.

Bit 2 **RXIFn**: Receive TXR_RXRn data register status

0: TXR_RXRn data register is empty

1: TXR_RXRn data register has available data

The RXIFn flag is the receive data register status flag. When this read only flag is "0", it indicates that the TXR_RXRn read data register is empty. When the flag is "1", it indicates that the TXR_RXRn read data register contains new data. When the contents of the shift register are transferred to the TXR_RXRn register, an interrupt is generated if RIEn=1 in the UnCR2 register. If one or more errors are detected in the received word, the appropriate receive-related flags NFn, FERRn, and/or PERRn are set within the same clock cycle. The RXIFn flag is cleared when the UnSR register is read with RXIFn set, followed by a read from the TXR_RXRn register, and if the TXR_RXRn register has no data available.

Bit 1 **TIDLEn**: Transmission idle

0: Data transmission is in progress (Data being transmitted)

1: No data transmission is in progress (Transmitter is idle)

The TIDLEn flag is known as the transmission complete flag. When this read only flag is "0", it indicates that a transmission is in progress. This flag will be set high when the TXIFn flag is "1" and when there is no transmit data or break character being transmitted. When TIDLEn is equal to "1", the TXn pin becomes idle with the pin state in logic high condition. The TIDLEn flag is cleared by reading the UnSR register with TIDLEn set and then writing to the TXR_RXRn register. The flag is not generated when a data character or a break is queued and ready to be sent.

Bit 0 **TXIFn**: Transmit TXR_RXRn data register status

0: Character is not transferred to the transmit shift register

1: Character has transferred to the transmit shift register (TXR_RXRn data register is empty)

The TXIFn flag is the transmit data register empty flag. When this read only flag is "0", it indicates that the character is not transferred to the transmitter shift register. When the flag is "1", it indicates that the transmitter shift register has received a character from the TXR_RXRn data register. The TXIFn flag is cleared by reading the UARTn status register (UnSR) with TXIFn set and then writing to the TXR_RXRn data register. Note that when the TXENn bit is set, the TXIFn flag bit will also be set since the transmit data register is not yet full.

- **UnCR1 Register**

    The UnCR1 register together with the UnCR2 register are the two UARTn control registers that are used to set the various options for the UARTn function, such as overall on/off control, parity control, data transfer bit length etc. Further explanation on each of the bits is given below:

Bit	7	6	5	4	3	2	1	0
Name	UARTENn	BNOn	PRENn	PRTn	STOPSn	TXBRKn	RX8n	TX8n
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	W
POR	0	0	0	0	0	0	x	0

"x" unknown

Bit 7　　**UARTENn**: UARTn function enable control
　　　　　0: Disable UARTn. TXn and RXn pins are in a floating state
　　　　　1: Enable UARTn. TXn and RXn pins function as UARTn pins

　　　　The UARTENn bit is the UARTn enable bit. When this bit is equal to "0", the UARTn will be disabled and the RXn pin as well as the TXn pin will be in a floating state. When the bit is equal to "1", the UARTn will be enabled and the TXn and RXn pins will function as defined by the TXENn and RXENn enable control bits.

　　　　When the UARTn is disabled, it will empty the buffer so any character remaining in the buffer will be discarded. In addition, the value of the baud rate counter will be reset. If the UARTn is disabled, all error and status flags will be reset. Also the TXENn, RXENn, TXBRKn, RXIFn, OERRn, FERRn, PERRn and NFn bits will be cleared, while the TIDLEn, TXIFn and RIDLEn bits will be set. Other control bits in UnCR1, UnCR2 and BRGn registers will remain unaffected. If the UARTn is active and the UARTENn bit is cleared, all pending transmissions and receptions will be terminated and the module will be reset as defined above. When the UARTn is re-enabled, it will restart in the same configuration.

Bit 6　　**BNOn**: Number of data transfer bits selection
　　　　　0: 8-bit data transfer
　　　　　1: 9-bit data transfer

　　　　This bit is used to select the data length format, which can have a choice of either 8-bit or 9-bit format. When this bit is equal to "1", a 9-bit data length format will be selected. If the bit is equal to "0", then an 8-bit data length format will be selected. If 9-bit data length format is selected, then bits RX8n and TX8n will be used to store the 9th bit of the received and transmitted data respectively.

Bit 5　　**PRENn**: Parity function enable control
　　　　　0: Parity function is disabled
　　　　　1: Parity function is enabled

　　　　This is the parity enable bit. When this bit is equal to "1", the parity function will be enabled. If the bit is equal to "0", then the parity function will be disabled.

Bit 4　　**PRTn**: Parity type selection bit
　　　　　0: Even parity for parity generator
　　　　　1: Odd parity for parity generator

　　　　This bit is the parity type selection bit. When this bit is equal to "1", odd parity type will be selected. If the bit is equal to "0", then even parity type will be selected.

Bit 3　　**STOPSn**: Number of Stop bits selection
　　　　　0: One stop bit format is used
　　　　　1: Two stop bits format is used

　　　　This bit determines if one or two stop bits are to be used. When this bit is equal to "1", two stop bits are used. If this bit is equal to "0", then only one stop bit is used.

Bit 2   **TXBRKn**: Transmit break character
        0: No break character is transmitted
        1: Break characters transmit

        The TXBRKn bit is the Transmit Break Character bit. When this bit is "0", there are no break characters and the TXn pin operates normally. When the bit is "1", there are transmit break characters and the transmitter will send logic zeros. When this bit is equal to "1", after the buffered data has been transmitted, the transmitter output is held low for a minimum of a 13-bit length and until the TXBRKn bit is reset.

Bit 1   **RX8n**: Receive data bit 8 for 9-bit data transfer format (read only)

        This bit is only used if 9-bit data transfers are used, in which case this bit location will store the 9th bit of the received data known as RX8n. The BNOn bit is used to determine whether data transfers are in 8-bit or 9-bit format.

Bit 0   **TX8n**: Transmit data bit 8 for 9-bit data transfer format (write only)

        This bit is only used if 9-bit data transfers are used, in which case this bit location will store the 9th bit of the transmitted data known as TX8n. The BNOn bit is used to determine whether data transfers are in 8-bit or 9-bit format.

- **UnCR2 Register**

The UnCR2 register is another UARTn control registers and serves several purposes. One of its main functions is to control the basic enable/disable operation of the UARTn Transmitter and Receiver as well as enabling the various UARTn interrupt sources. The register also serves to control the baud rate speed, receiver wake-up enable and the address detect enable. Further explanation on each of the bits is given below:

Bit	7	6	5	4	3	2	1	0
Name	TXENn	RXENn	BRGHn	ADDENn	WAKEn	RIEn	TIIEn	TEIEn
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7   **TXENn**: UARTn Transmitter enabled control
        0: UARTn transmitter is disabled
        1: UARTn transmitter is enabled

        The bit named TXENn is the Transmitter Enable Bit. When this bit is equal to "0", the transmitter will be disabled with any pending data transmissions being aborted. In addition the buffers will be reset. In this situation the TXn pin will be in a floating state.

        If the TXENn bit is equal to "1" and the UARTENn bit is also equal to "1", the transmitter will be enabled and the TXn pin will be controlled by the UARTn. Clearing the TXENn bit during a transmission will cause the data transmission to be aborted and will reset the transmitter. If this situation occurs, the TXn pin will be in a floating state.

Bit 6   **RXENn**: UARTn Receiver enabled control
        0: UARTn receiver is disabled
        1: UARTn receiver is enabled

        The bit named RXENn is the Receiver Enable Bit. When this bit is equal to "0", the receiver will be disabled with any pending data receptions being aborted. In addition the receive buffers will be reset. In this situation the RXn pin will be in a floating state. If the RXENn bit is equal to "1" and the UARTENn bit is also equal to "1", the receiver will be enabled and the RXn pin will be controlled by the UARTn. Clearing the RXENn bit during a reception will cause the data reception to be aborted and will reset the receiver. If this situation occurs, the RXn pin will be in a floating state.

Bit 5 **BRGHn**: Baud Rate speed selection

0: Low speed baud rate

1: High speed baud rate

The bit named BRGHn selects the high or low speed mode of the Baud Rate Generator. This bit, together with the value placed in the baud rate register BRGn, controls the Baud Rate of the UARTn. If this bit is equal to "1", the high speed mode is selected. If the bit is equal to "0", the low speed mode is selected.

Bit 4 **ADDENn**: Address detect function enable control

0: Address detect function is disabled

1: Address detect function is enabled

The bit named ADDENn is the address detect function enable control bit. When this bit is equal to "1", the address detect function is enabled. When it occurs, if the 8th bit, which corresponds to RX7n if BNOn=0 or the 9th bit, which corresponds to RX8n if BNOn=1, has a value of "1", then the received word will be identified as an address, rather than data. If the corresponding interrupt is enabled, an interrupt request will be generated each time the received word has the address bit set, which is the 8th or 9th bit depending on the value of BNOn. If the address bit known as the 8th or 9th bit of the received word is "0" with the address detect function being enabled, an interrupt will not be generated and the received data will be discarded.

Bit 3 **WAKEn**: RXn pin wake-up UARTn function enable control

0: RXn pin wake-up UARTn function is disabled

1: RXn pin wake-up UARTn function is enabled

This bit is used to control the wake-up UARTn function when a falling edge on the RXn pin occurs. Note that this bit is only available when the UARTn clock (f_H) is switched off. There will be no RXn pin wake-up UARTn function if the UARTn clock (f_H) exists. If the WAKEn bit is set to 1 as the UARTn clock (f_H) is switched off, a UARTn wake-up request will be initiated when a falling edge on the RXn pin occurs. When this request happens and the corresponding interrupt is enabled, an RXn pin wake-up UARTn interrupt will be generated to inform the MCU to wake up the UARTn function by switching on the UARTn clock (f_H) via the application program. Otherwise, the UARTn function can not resume even if there is a falling edge on the RXn pin when the WAKEn bit is cleared to 0.

Bit 2 **RIEn**: Receiver interrupt enable control

0: Receiver related interrupt is disabled

1: Receiver related interrupt is enabled

This bit enables or disables the receiver interrupt. If this bit is equal to "1" and when the receiver overrun flag OERRn or receive data available flag RXIFn is set, the UARTn interrupt request flag will be set. If this bit is equal to "0", the UARTn interrupt request flag will not be influenced by the condition of the OERRn or RXIFn flags.

Bit 1 **TIIEn**: Transmitter Idle interrupt enable control

0: Transmitter idle interrupt is disabled

1: Transmitter idle interrupt is enabled

This bit enables or disables the transmitter idle interrupt. If this bit is equal to "1" and when the transmitter idle flag TIDLEn is set, due to a transmitter idle condition, the UARTn interrupt request flag will be set. If this bit is equal to "0", the UARTn interrupt request flag will not be influenced by the condition of the TIDLEn flag.

Bit 0 **TEIEn**: Transmitter Empty interrupt enable control

0: Transmitter empty interrupt is disabled

1: Transmitter empty interrupt is enabled

This bit enables or disables the transmitter empty interrupt. If this bit is equal to "1" and when the transmitter empty flag TXIFn is set, due to a transmitter empty condition, the UARTn interrupt request flag will be set. If this bit is equal to "0", the UARTn interrupt request flag will not be influenced by the condition of the TXIFn flag.

- **TXR_RXRn Register**

Bit	7	6	5	4	3	2	1	0
Name	TXRXn7	TXRXn6	TXRXn5	TXRXn4	TXRXn3	TXRXn2	TXRXn1	TXRXn0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x" unknown

Bit 7~0   **TXRXn7~TXRXn0**: UARTn Transmit/Receive Data bit 7 ~ bit 0

- **BRGn Register**

Bit	7	6	5	4	3	2	1	0
Name	BRGn7	BRGn6	BRGn5	BRGn4	BRGn3	BRGn2	BRGn1	BRGn0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x" unknown

Bit 7~0   **BRGn7~ BRGn0**: Baud Rate values

By programming the BRGHn bit in UnCR2 Register which allows selection of the related formula described above and programming the required value in the BRGn register, the required baud rate can be setup.

Note: Baud rate= f_H / [64 × (N+1)] if BRGHn=0.

Baud rate= f_H / [16 × (N+1)] if BRGHn=1.

Baud Rate Generator

To setup the speed of the serial data communication, the UARTn function contains its own dedicated baud rate generator. The baud rate is controlled by its own internal free running 8-bit timer, the period of which is determined by two factors. The first of these is the value placed in the baud rate register BRGn and the second is the value of the BRGHn bit with the control register UnCR2. The BRGHn bit decides if the baud rate generator is to be used in a high speed mode or low speed mode, which in turn determines the formula that is used to calculate the baud rate. The value N in the BRGn register which is used in the following baud rate calculation formula determines the division factor. Note that N is the decimal value placed in the BRGn register and has a range of between 0 and 255.

UnCR2 BRGHn Bit	0	1
Baud Rate (BR)	f_H / [64 (N+1)]	f_H / [16 (N+1)]

By programming the BRGHn bit which allows selection of the related formula and programming the required value in the BRGn register, the required baud rate can be setup. Note that because the actual baud rate is determined using a discrete value, N, placed in the BRGn register, there will be an error associated between the actual and requested value. The following example shows how the BRGn register value N and the error value can be calculated.

Calculating the Baud Rate and Error Values

For a clock frequency of 4MHz, and with BRGHn cleared to zero determine the BRGn register value N, the actual baud rate and the error value for a desired baud rate of 4800.

From the above table the desired baud rate BR = f_H / [64 (N+1)]

Re-arranging this equation gives N = [f_H / (BR×64)] - 1

Giving a value for N = [4000000 / (4800×64)] - 1 = 12.0208

To obtain the closest value, a decimal value of 12 should be placed into the BRGn register. This gives an actual or calculated baud rate value of BR = 4000000 / [64 × (12+1)] = 4808

Therefore the error is equal to (4808 - 4800) / 4800 = 0.16%

UARTn Setup and Control

For data transfer, the UARTn function utilizes a non-return-to-zero, more commonly known as NRZ, format. This is composed of one start bit, eight or nine data bits, and one or two stop bits. Parity is supported by the UARTn hardware, and can be setup to be even, odd or no parity. For the most common data format, 8 data bits along with no parity and one stop bit, denoted as 8, N, 1, is used as the default setting, which is the setting at power-on. The number of data bits and stop bits, along with the parity, are setup by programming the corresponding BNOn, PRTn, PRENn, and STOPSn bits in the UnCR1 register. The baud rate used to transmit and receive data is setup using the internal 8-bit baud rate generator, while the data is transmitted and received LSB first. Although the UARTn transmitter and receiver are functionally independent, they both use the same data format and baud rate. In all cases stop bits will be used for data transmission.

Enabling/Disabling the UARTn Interface

The basic on/off function of the internal UARTn function is controlled using the UARTENn bit in the UnCR1 register. If the UARTENn, TXENn and RXENn bits are set, then these two UARTn pins will act as normal TXn output pin and RXn input pin respectively. If no data is being transmitted on the TXn pin, then it will default to a logic high value.

Clearing the UARTENn bit will disable the TXn and RXn pins and allow these two pins to be used as normal I/O or other pin-shared functional pins by configuring the corresponding pin-shared control bits. When the UARTn function is disabled the buffer will be reset to an empty condition, at the same time discarding any remaining residual data. Disabling the UARTn will also reset the error and status flags with bits TXENn, RXENn, TXBRKn, RXIFn, OERRn, FERRn, PERRn and NFn being cleared while bits TIDLEn, TXIFn and RIDLEn will be set. The remaining control bits in the UnCR1, UnCR2 and BRGn registers will remain unaffected. If the UARTENn bit in the UnCR1 register is cleared while the UARTn is active, then all pending transmissions and receptions will be immediately suspended and the UARTn will be reset to a condition as defined above. If the UARTn is then subsequently re-enabled, it will restart again in the same configuration.

Data, Parity and Stop Bit Selection

The format of the data to be transferred is composed of various factors such as data bit length, parity on/off, parity type, address bits and the number of stop bits. These factors are determined by the setup of various bits within the UnCR1 register. The BNOn bit controls the number of data bits which can be set to either 8 or 9, the PRTn bit controls the choice of odd or even parity, the PRENn bit controls the parity on/off function and the STOPSn bit decides whether one or two stop bits are to be used. The following table shows various formats for data transmission. The address bit, which is the MSB of the data byte, identifies the frame as an address character or data if the address detect function is enabled. The number of stop bits, which can be either one or two, is independent of the data length and is only used for the transmitter. There is only one stop bit for the receiver.

Start Bit	Data Bits	Address Bit	Parity Bit	Stop Bit
Example of 8-bit Data Formats				
1	8	0	0	1
1	7	0	1	1
1	7	1	0	1
Example of 9-bit Data Formats				
1	9	0	0	1
1	8	0	1	1
1	8	1	0	1

Transmitter Receiver Data Format

The following diagram shows the transmit and receive waveforms for both 8-bit and 9-bit data formats.

8-bit Data Format

9-bit Data Format
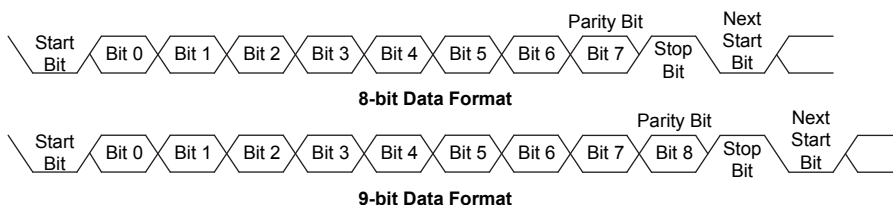
UARTn Transmitter

Data word lengths of either 8 or 9 bits can be selected by programming the BNOn bit in the UnCR1 register. When BNOn bit is set, the word length will be set to 9 bits. In this case the 9th bit, which is the MSB, needs to be stored in the TX8n bit in the UnCR1 register. At the transmitter core lies the Transmitter Shift Register, more commonly known as the TSRn, whose data is obtained from the transmit data register, which is known as the TXR_RXRn register. The data to be transmitted is loaded into this TXR_RXRn register by the application program. The TSRn register is not written to with new data until the stop bit from the previous transmission has been sent out. As soon as this stop bit has been transmitted, the TSRn can then be loaded with new data from the TXR_RXRn register, if it is available. It should be noted that the TSRn register, unlike many other registers, is not directly mapped into the Data Memory area and as such is not available to the application program for direct read/write operations. An actual transmission of data will normally be enabled when the TXENn bit is set, but the data will not be transmitted until the TXR_RXRn register has been loaded with data and the baud rate generator has defined a shift clock source. However, the transmission can also be initiated by first loading data into the TXR_RXRn register, after which the TXENn bit can be set. When a transmission of data begins, the TSRn is normally empty, in which case a transfer to the TXR_RXRn register will result in an immediate transfer to the TSRn. If during a transmission the TXENn bit is cleared, the transmission will immediately cease and the transmitter will be reset. The TXn output pin can then be configured as the I/O or other pin-shared function by configuring the corresponding pin-shared control bits.

Transmitting Data

When the UARTn is transmitting data, the data is shifted on the TXn pin from the shift register, with the least significant bit first. In the transmit mode, the TXR_RXRn register forms a buffer between the internal bus and the transmitter shift register. It should be noted that if 9-bit data format has been selected, then the MSB will be taken from the TX8n bit in the UnCR1 register. The steps to initiate a data transfer can be summarized as follows:

- Make the correct selection of the BNOn, PRTn, PRENn and STOPSn bits to define the required word length, parity type and number of stop bits.

- Setup the BRGn register to select the desired baud rate.

- Set the TXENn bit to ensure that the TXn pin is used as a UARTn transmitter pin.

- Access the UnSR register and write the data that is to be transmitted into the TXR_RXRn register.

Note that this step will clear the TXIFn bit.

This sequence of events can now be repeated to send additional data.

It should be noted that when TXIFn=0, data will be inhibited from being written to the TXR_RXRn register. Clearing the TXIFn flag is always achieved using the following software sequence:

1. A UnSR register access

2. A TXR_RXRn register write execution

The read-only TXIFn flag is set by the UARTn hardware and if set indicates that the TXR_RXRn register is empty and that other data can now be written into the TXR_RXRn register without overwriting the previous data. If the TEIEn bit is set then the TXIFn flag will generate an interrupt.

During a data transmission, a write instruction to the TXR_RXRn register will place the data into the TXR_RXRn register, which will be copied to the shift register at the end of the present transmission. When there is no data transmission in progress, a write instruction to the TXR_RXRn register will place the data directly into the shift register, resulting in the commencement of data transmission, and the TXIFn bit being immediately set. When a frame transmission is complete, which happens after stop bits are sent or after the break frame, the TIDLEn bit will be set. To clear the TIDLEn bit the following software sequence is used:

1. A UnSR register access

2. A TXR_RXRn register write execution

Note that both the TXIFn and TIDLEn bits are cleared by the same software sequence.

Transmit Break

If the TXBRKn bit is set then break characters will be sent on the next transmission. Break character transmission consists of a start bit, followed by $13 \times N$ "0" bits and stop bits, where N=1, 2, etc. If a break character is to be transmitted then the TXBRKn bit must be first set by the application program, and then cleared to generate the stop bits. Transmitting a break character will not generate a transmit interrupt. Note that a break condition length is at least 13 bits long. If the TXBRKn bit is continually kept at a logic high level then the transmitter circuitry will transmit continuous break characters. After the application program has cleared the TXBRKn bit, the transmitter will finish transmitting the last break character and subsequently send out one or two stop bits. The automatic logic highs at the end of the last break character will ensure that the start bit of the next frame is recognized.

UARTn Receiver

The UARTn is capable of receiving word lengths of either 8 or 9 bits. If the BNOn bit is set, the word length will be set to 9 bits with the MSB being stored in the RX8n bit of the UnCR1 register. At the receiver core lies the Receive Serial Shift Register, commonly known as the RSRn. The data which is received on the RXn external input pin is sent to the data recovery block. The data recovery block operating speed is 16 times that of the baud rate, while the main receive serial shifter operates at the baud rate. After the RXn pin is sampled for the stop bit, the received data in RSRn is transferred to the receive data register, if the register is empty. The data which is received on the external RXn input pin is sampled three times by a majority detect circuit to determine the logic level that has been placed onto the RXn pin. It should be noted that the RSRn register, unlike many other registers, is not directly mapped into the Data Memory area and as such is not available to the application program for direct read/write operations.

Receiving Data

When the UARTn receiver is receiving data, the data is serially shifted in on the external RXn input pin, LSB first. In the read mode, the TXR_RXRn register forms a buffer between the internal bus and the receiver shift register. The TXR_RXRn register is a two byte deep FIFO data buffer, where two bytes can be held in the FIFO while a third byte can continue to be received. Note that the application program must ensure that the data is read from TXR_RXRn before the third byte has been completely shifted in, otherwise this third byte will be discarded and an overrun error OERRn will be subsequently indicated. The steps to initiate a data transfer can be summarized as follows:

• Make the correct selection of BNOn, PRTn and PRENn bits to define the word length, parity type.

- Setup the BRGn register to select the desired baud rate.

- Set the RXENn bit to ensure that the RXn pin is used as a UARTn receiver pin.

At this point the receiver will be enabled which will begin to look for a start bit.

When a character is received the following sequence of events will occur:

- The RXIFn bit in the UnSR register will be set when the TXR_RXRn register has data available. There will be at most one more character available before an overrun error occurs.

- When the contents of the shift register have been transferred to the TXR_RXRn register, then if the RIEn bit is set, an interrupt will be generated.

- If during reception, a frame error, noise error, parity error, or an overrun error has been detected, then the error flags can be set.

The RXIFn bit can be cleared using the following software sequence:

1. A UnSR register access

2. A TXR_RXRn register read execution

Receive Break

Any break character received by the UARTn will be managed as a framing error. The receiver will count and expect a certain number of bit times as specified by the values programmed into the BNOn bit plus one stop bit. If the break is much longer than 13 bit times, the reception will be considered as complete after the number of bit times specified by BNOn plus one stop bit. The RXIFn bit is set, FERRn is set, zeros are loaded into the receive data register, interrupts are generated if appropriate and the RIDLEn bit is set. A break is regarded as a character that contains only zeros with the FERRn flag set. If a long break signal has been detected, the receiver will regard it as a data frame including a start bit, data bits and the invalid stop bit and the FERRn flag will be set. The receiver must wait for a valid stop bit before looking for the next start bit. The receiver will not make the assumption that the break condition on the line is the next start bit. The break character will be loaded into the buffer and no further data will be received until stop bits are received. It should be noted that the RIDLEn read only flag will go high when the stop bits have not yet been received.

The reception of a break character on the UARTn registers will result in the following:

- The framing error flag, FERRn, will be set.

- The receive data register, TXR_RXRn, will be cleared.

- The OERRn, NFn, PERRn, RIDLEn or RXIFn flags will possibly be set.

Idle Status

When the receiver is reading data, which means it will be in between the detection of a start bit and the reading of a stop bit, the receiver status flag in the UnSR register, otherwise known as the RIDLEn flag, will have a zero value. In between the reception of a stop bit and the detection of the next start bit, the RIDLEn flag will have a high value, which indicates the receiver is in an idle condition.

Receiver Interrupt

The read only receive interrupt flag RXIFn in the UnSR register is set by an edge generated by the receiver. An interrupt is generated if RIEn=1, when a word is transferred from the Receive Shift Register, RSRn, to the Receive Data Register, TXR_RXRn. An overrun error can also generate an interrupt if RIEn=1.

Managing Receiver Errors

Several types of reception errors can occur within the UARTn module, the following section describes the various types and how they are managed by the UARTn.

Overrun Error – OERRn

The TXR_RXRn register is composed of a two byte deep FIFO data buffer, where two bytes can be held in the FIFO register, while a third byte can continue to be received. Before this third byte has been entirely shifted in, the data should be read from the TXR_RXRn register. If this is not done, the overrun error flag OERRn will be consequently indicated.

In the event of an overrun error occurring, the following will happen:

- The OERRn flag in the UnSR register will be set.
- The TXR_RXRn contents will not be lost.
- The shift register will be overwritten.
- An interrupt will be generated if the RIEn bit is set.

The OERRn flag can be cleared by an access to the UnSR register followed by a read to the TXR_RXRn register.

Noise Error – NFn

Over-sampling is used for data recovery to identify valid incoming data and noise. If noise is detected within a frame the following will occur:

- The read only noise flag, NFn, in the UnSR register will be set on the rising edge of the RXIFn bit.
- Data will be transferred from the Shift register to the TXR_RXRn register.
- No interrupt will be generated. However this bit rises at the same time as the RXIFn bit which itself generates an interrupt.

Note that the NFn flag is reset by an UnSR register read operation followed by a TXR_RXRn register read operation.

Framing Error – FERRn

The read only framing error flag, FERRn, in the UnSR register, is set if a zero is detected instead of stop bits. If two stop bits are selected, both stop bits must be high; otherwise the FERRn flag will be set. The FERRn flag and the received data will be recorded in the UnSR and TXR_RXRn registers respectively, and the flag is cleared in any reset.

Parity Error – PERRn

The read only parity error flag, PERRn, in the UnSR register, is set if the parity of the received word is incorrect. This error flag is only applicable if the parity is enabled, PRENn = 1, and if the parity type, odd or even is selected. The read only PERRn flag and the received data will be recorded in the UnSR and TXR_RXRn registers respectively. It is cleared on any reset, it should be noted that the flags, FERRn and PERRn, in the UnSR register should first be read by the application program before reading the data word.

UARTn Interrupt Structure

Several individual UARTn conditions can generate a UARTn interrupt. When these conditions exist, a low pulse will be generated to get the attention of the microcontroller. These conditions are a transmitter data register empty, transmitter idle, receiver data available, receiver overrun, address detect and an RXn pin wake-up. When any of these conditions are created, if the global interrupt enable bit, multi-function interrupt enable bit and its corresponding interrupt control bit are enabled and the stack is not full, the program will jump to its corresponding interrupt vector where it can be serviced before returning to the main program. Four of these conditions have the corresponding UnSR register flags which will generate a UARTn interrupt if its associated interrupt enable control bit in the UnCR2 register is set. The two transmitter interrupt conditions have their own corresponding enable control bits, while the two receiver interrupt conditions have a shared enable control bit. These enable bits can be used to mask out individual UARTn interrupt sources.

The address detect condition, which is also a UARTn interrupt source, does not have an associated flag, but will generate a UARTn interrupt when an address detect condition occurs if its function is enabled by setting the ADDENn bit in the UnCR2 register. An RXn pin wake-up, which is also a UARTn interrupt source, does not have an associated flag, but will generate a UARTn interrupt if the UARTn clock (f_H) source is switched off and the WAKEn and RIEn bits in the UnCR2 register are set when a falling edge on the RXn pin occurs.

Note that the UnSR register flags are read only and cannot be cleared or set by the application program, neither will they be cleared when the program jumps to the corresponding interrupt servicing routine, as is the case for some of the other interrupts. The flags will be cleared automatically when certain actions are taken by the UARTn, the details of which are given in the UARTn register section. The overall UARTn interrupt can be disabled or enabled by the related interrupt enable control bits in the interrupt control registers of the microcontroller to decide whether the interrupt requested by the UARTn module is masked out or allowed.
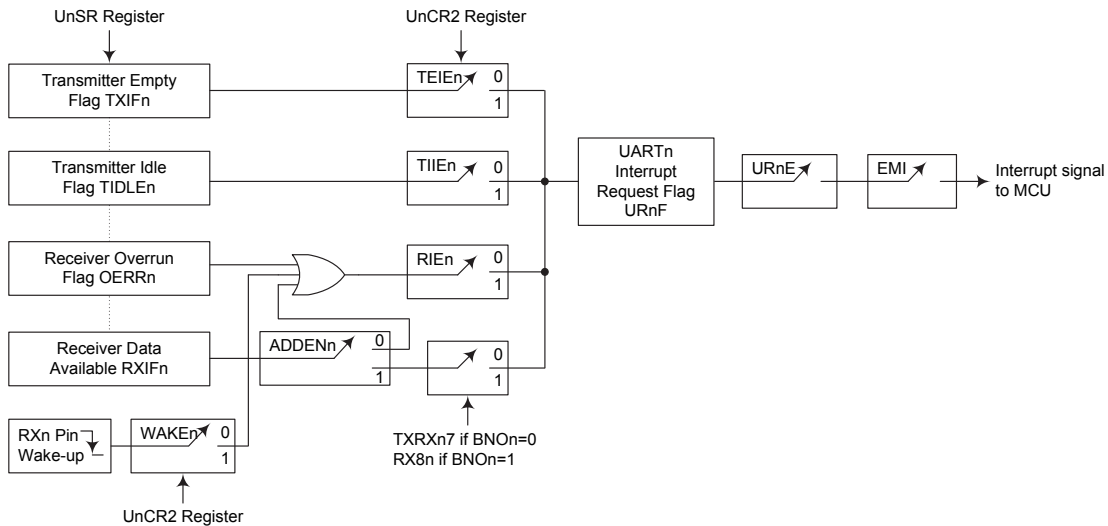
UARTn Interrupt Structure

Address Detect Mode

Setting the Address Detect Mode bit, ADDENn, in the UnCR2 register, enables this special mode. If this bit is enabled then an additional qualifier will be placed on the generation of a Receiver Data Available interrupt, which is requested by the RXIFn flag. If the ADDENn bit is enabled, then when data is available, an interrupt will only be generated, if the highest received bit has a high value. Note that the URnE and EMI interrupt enable bits must also be enabled for correct interrupt generation. This highest address bit is the 9th bit if BNOn=1 or the 8th bit if BNOn=0. If this bit is high, then the received word will be defined as an address rather than data. A Data Available interrupt will be generated every time the last bit of the received word is set. If the ADDENn bit is not enabled, then a Receiver Data Available interrupt will be generated each time the RXIFn flag is set, irrespective of the data last bit status. The address detect mode and parity enable are mutually exclusive functions. Therefore if the address detect mode is enabled, then to ensure correct operation, the parity function should be disabled by resetting the parity enable bit PRENn to zero.

ADDENn	Bit 9 if BNOn=1, Bit 8 if BNOn=0	UARTn Interrupt Generated
0	0	√
	1	√
1	0	×
	1	√

ADDENn Bit Function

UARTn Power Down and Wake-up

When the UARTn clock (f_H) is off, the UARTn will cease to function, all clock sources to the module are shutdown. If the UARTn clock (f_H) is off while a transmission is still in progress, then the transmission will be paused until the UARTn clock source derived from the microcontroller is activated. In a similar way, if the MCU enters the Power Down Mode while receiving data, then the reception of data will likewise be paused. When the MCU enters the Power Down Mode, note that the UnSR, UnCR1, UnCR2, transmit and receive registers, as well as the BRGn register will not be affected. It is recommended to make sure first that the UARTn data transmission or reception has been finished before the microcontroller enters the Power Down mode.

The UARTn function contains a receiver RXn pin wake-up function, which is enabled or disabled by the WAKEn bit in the UnCR2 register. If this bit, along with the UARTn enable bit, UARTENn, the receiver enable bit, RXENn and the receiver interrupt bit, RIEn, are all set when the UARTn clock (f_H) is off, then a falling edge on the RXn pin will trigger an RXn pin wake-up UARTn interrupt. Note that as it takes certain system clock cycles after a wake-up, before normal microcontroller operation resumes, any data received during this time on the RXn pin will be ignored.

For a UARTn wake-up interrupt to occur, in addition to the bits for the wake-up being set, the global interrupt enable bit, EMI, and the UARTn interrupt enable bit, URnE, must be set. If the EMI and URnE bits are not set then only a wake up event will occur and no interrupt will be generated. Note also that as it takes certain system clock cycles after a wake-up before normal microcontroller resumes, the UARTn interrupt will not be generated until after this time has elapsed.

Interrupts

Interrupts are an important part of any microcontroller system. When an external event or an internal function such as a Timer Module or an A/D converter requires microcontroller attention, their corresponding interrupt will enforce a temporary suspension of the main program allowing the microcontroller to direct attention to their respective needs. The device contains several external interrupt and internal interrupt functions. The external interrupts are generated by the action of the external INT0~INT1 pins, while the internal interrupts are generated by various internal functions such as the Timer Modules (TMs), Time Bases, Serial Interface Module (SIM), Serial Peripheral Interface (SPIA), Low Voltage Detector (LVD), Over Voltage Protection (OVP), EEPROM and the A/D converter.

Interrupt Registers

Overall interrupt control, which basically means the setting of request flags when certain microcontroller conditions occur and the setting of interrupt enable bits by the application program, is controlled by a series of registers, located in the Special Purpose Data Memory. The registers fall into three categories. The first is the INTC0~INTC3 registers which setup the primary interrupts, the second is the MFI0~MFI2 registers which setup the Multi-function interrupts. Finally there is an INTEG register to setup the external interrupts trigger edge type.

Each register contains a number of enable bits to enable or disable individual registers as well as interrupt flags to indicate the presence of an interrupt request. The naming convention of these follows a specific pattern. First is listed an abbreviated interrupt type, then the (optional) number of that interrupt followed by either an "E" for enable/disable bit or "F" for request flag.

Function	Enable Bit	Request Flag	Notes
Global	EMI	—	—
INTn Pin	INTnE	INTnF	n=0~1
A/D Converter	ADE	ADF	—
Multi-function	MFnE	MFnF	n=0~2
Over Voltage Protection	OVPE	OVPF	—
Time Base	TBnE	TBnF	n=0~1
LVD	LVE	LVF	—
EEPROM	DEE	DEF	—
UART	URnE	URnF	n=0~1
SIM	SIME	SIMF	—
SPIA	SPIAE	SPIAF	—
STM	STMPE	STMPF	—
	STMAE	STMAF	
PTM	PTMnPE	PTMnPF	n=0~2
	PTMnAE	PTMnAF	

Interrupt Register Bit Naming Conventions

Register Name	Bit							
	7	6	5	4	3	2	1	0
INTEG	—	—	—	—	INT1S1	INT1S0	INT0S1	INT0S0
INTC0	—	ADF	INT1F	INT0F	ADE	INT1E	INT0E	EMI
INTC1	OVPF	MF2F	MF1F	MF0F	OVPE	MF2E	MF1E	MF0E
INTC2	SIMF	UR0F	TB1F	TB0F	SIME	UR0E	TB1E	TB0E
INTC3	—	—	UR1F	SPIAF	—	—	UR1E	SPIAE
MFI0	PTM0AF	PTM0PF	STMAF	STMPF	PTM0AE	PTM0PE	STMAE	STMPE

Register Name	Bit							
	7	6	5	4	3	2	1	0
MFI1	PTM2AF	PTM2PF	PTM1AF	PTM1PF	PTM2AE	PTM2PE	PTM1AE	PTM1PE
MFI2	—	—	DEF	LVF	—	—	DEE	LVE

Interrupt Register List

• **INTEG Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	INT1S1	INT1S0	INT0S1	INT0S0
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	—	—	—	—	0	0	0	0

Bit 7~4 Unimplemented, read as "0"

Bit 3~2 **INT1S1~INT1S0**: Interrupt Edge Control for INT1 Pin
      00: Disable
      01: Rising edge
      10: Falling edge
      11: Rising and falling edges

Bit 1~0 **INT0S1~INT0S0**: Interrupt Edge Control for INT0 Pin
      00: Disable
      01: Rising edge
      10: Falling edge
      11: Rising and falling edges

• **INTC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	ADF	INT1F	INT0F	ADE	INT1E	INT0E	EMI
R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	0	0	0	0	0	0	0

Bit 7   Unimplemented, read as "0"

Bit 6   **ADF**: A/D Converter Interrupt Request Flag
      0: No request
      1: Interrupt request

Bit 5   **INT1F**: External Interrupt 1Request Flag
      0: No request
      1: Interrupt request

Bit 4   **INT0F**: External Interrupt 0 Request Flag
      0: No request
      1: Interrupt request

Bit 3   **ADE**: A/D Converter Interrupt Control
      0: Disable
      1: Enable

Bit 2   **INT1E**: External Interrupt 1 Control
      0: Disable
      1: Enable

Bit 1   **INT0E**: External Interrupt 0 Control
      0: Disable
      1: Enable

Bit 0   **EMI**: Global Interrupt Control
      0: Disable
      1: Enable

- **INTC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	OVPF	MF2F	MF1F	MF0F	OVPE	MF2E	MF1E	MF0E
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7   **OVPF**: Over Voltage Protection Interrupt Request Flag
          0: No request
          1: Interrupt request

Bit 6   **MF2F**: Multi-function Interrupt 2 Request Flag
          0: No request
          1: Interrupt request

Bit 5   **MF1F**: Multi-function Interrupt 1 Request Flag
          0: No request
          1: Interrupt request

Bit 4   **MF0F**: Multi-function Interrupt 0 Request Flag
          0: No request
          1: Interrupt request

Bit 3   **OVPE**: Over Voltage Protection Interrupt Control
          0: Disable
          1: Enable

Bit 2   **MF2E**: Multi-function Interrupt 2 Control
          0: Disable
          1: Enable

Bit 1   **MF1E**: Multi-function Interrupt 1 Control
          0: Disable
          1: Enable

Bit 0   **MF0E**: Multi-function Interrupt 0 Control
          0: Disable
          1: Enable

- **INTC2 Register**

Bit	7	6	5	4	3	2	1	0
Name	SIMF	UR0F	TB1F	TB0F	SIME	UR0E	TB1E	TB0E
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7   **SIMF**: Serial Interface Module Interrupt Request Flag
          0: No request
          1: Interrupt request

Bit 6   **UR0F**: UART0 Interrupt Request Flag
          0: No request
          1: Interrupt request

Bit 5   **TB1F**: Time Base 1 Interrupt Request Flag
          0: No request
          1: Interrupt request

Bit 4   **TB0F**: Time Base 0 Interrupt Request Flag
          0: No request
          1: Interrupt request

Bit 3   **SIME**: Serial Interface Module Interrupt Control
          0: Disable
          1: Enable

Bit 2   **UR0E**: UART0 Interrupt Control
　　　　　0: Disable
　　　　　1: Enable

Bit 1   **TB1E**: Time Base 1 Interrupt Control
　　　　　0: Disable
　　　　　1: Enable

Bit 0   **TB0E**: Time Base 0 Interrupt Control
　　　　　0: Disable
　　　　　1: Enable

• **INTC3 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	UR1F	SPIAF	—	—	UR1E	SPIAE
R/W	—	—	R/W	R/W	—	—	R/W	R/W
POR	—	—	0	0	—	—	0	0

Bit 7~6   Unimplemented, read as "0"

Bit 5   **UR1F**: UART1 Interrupt Request Flag
　　　　　0: No request
　　　　　1: Interrupt request

Bit 4   **SPIAF**: SPIA Interrupt Request Flag
　　　　　0: No request
　　　　　1: Interrupt request

Bit 3~2   Unimplemented, read as "0"

Bit 1   **UR1E**: UART1 Interrupt Control
　　　　　0: Disable
　　　　　1: Enable

Bit 0   **SPIAE**: SPIA Interrupt Control
　　　　　0: Disable
　　　　　1: Enable

• **MFI0 Register**

Bit	7	6	5	4	3	2	1	0
Name	PTM0AF	PTM0PF	STMAF	STMPF	PTM0AE	PTM0PE	STMAE	STMPE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7   **PTM0AF**: PTM0 CCRA Comparator Interrupt Request Flag
　　　　　0: No request
　　　　　1: Interrupt request

Bit 6   **PTM0PF**: PTM0 CCRP Comparator Interrupt Request Flag
　　　　　0: No request
　　　　　1: Interrupt request

Bit 5   **STMAF**: STM CCRA Comparator Interrupt Request Flag
　　　　　0: No request
　　　　　1: Interrupt request

Bit 4   **STMPF**: STM CCRP Comparator Interrupt Request Flag
　　　　　0: No request
　　　　　1: Interrupt request

Bit 3   **PTM0AE**: PTM0 CCRA Comparator Interrupt Control
　　　　　0: Disable
　　　　　1: Enable

Bit 2   **PTM0PE**: PTM0 CCRP Comparator Interrupt Control
         0: Disable
         1: Enable

Bit 1   **STMAE**: STM CCRA Comparator Interrupt Control
         0: Disable
         1: Enable

Bit 0   **STMPE**: STM CCRP Comparator Interrupt Control
         0: Disable
         1: Enable

- **MFI1 Register**

Bit	7	6	5	4	3	2	1	0
Name	PTM2AF	PTM2PF	PTM1AF	PTM1PF	PTM2AE	PTM2PE	PTM1AE	PTM1PE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7   **PTM2AF**: PTM2 CCRA Comparator Interrupt Request Flag
         0: No request
         1: Interrupt request

Bit 6   **PTM2PF**: PTM2 CCRP Comparator Interrupt Request Flag
         0: No request
         1: Interrupt request

Bit 5   **PTM1AF**: PTM1 CCRA Comparator Interrupt Request Flag
         0: No request
         1: Interrupt request

Bit 4   **PTM1PF**: PTM1 CCRP Comparator Interrupt Request Flag
         0: No request
         1: Interrupt request

Bit 3   **PTM2AE**: PTM2 CCRA Comparator Interrupt Control
         0: Disable
         1: Enable

Bit 2   **PTM2PE**: PTM2 CCRP Comparator Interrupt Control
         0: Disable
         1: Enable

Bit 1   **PTM1AE**: PTM1 CCRA Comparator Interrupt Control
         0: Disable
         1: Enable

Bit 0   **PTM1PE**: PTM1 CCRP Comparator Interrupt Control
         0: Disable
         1: Enable

MFI2 Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	DEF	LVF	—	—	DEE	LVE
R/W	—	—	R/W	R/W	—	—	R/W	R/W
POR	—	—	0	0	—	—	0	0

Bit 7~6   Unimplemented, read as "0"

Bit 5   **DEF**: Data EEPROM Interrupt Request Flag
         0: No request
         1: Interrupt request

Bit 4   **LVF**: LVD Interrupt Request Flag
         0: No request
         1: Interrupt request

Bit 3~2   Unimplemented, read as "0"

Bit 1   **DEE**: Data EEPROM Interrupt Control
    0: Disable
    1: Enable

Bit 0   **LVE**: LVD Interrupt Control
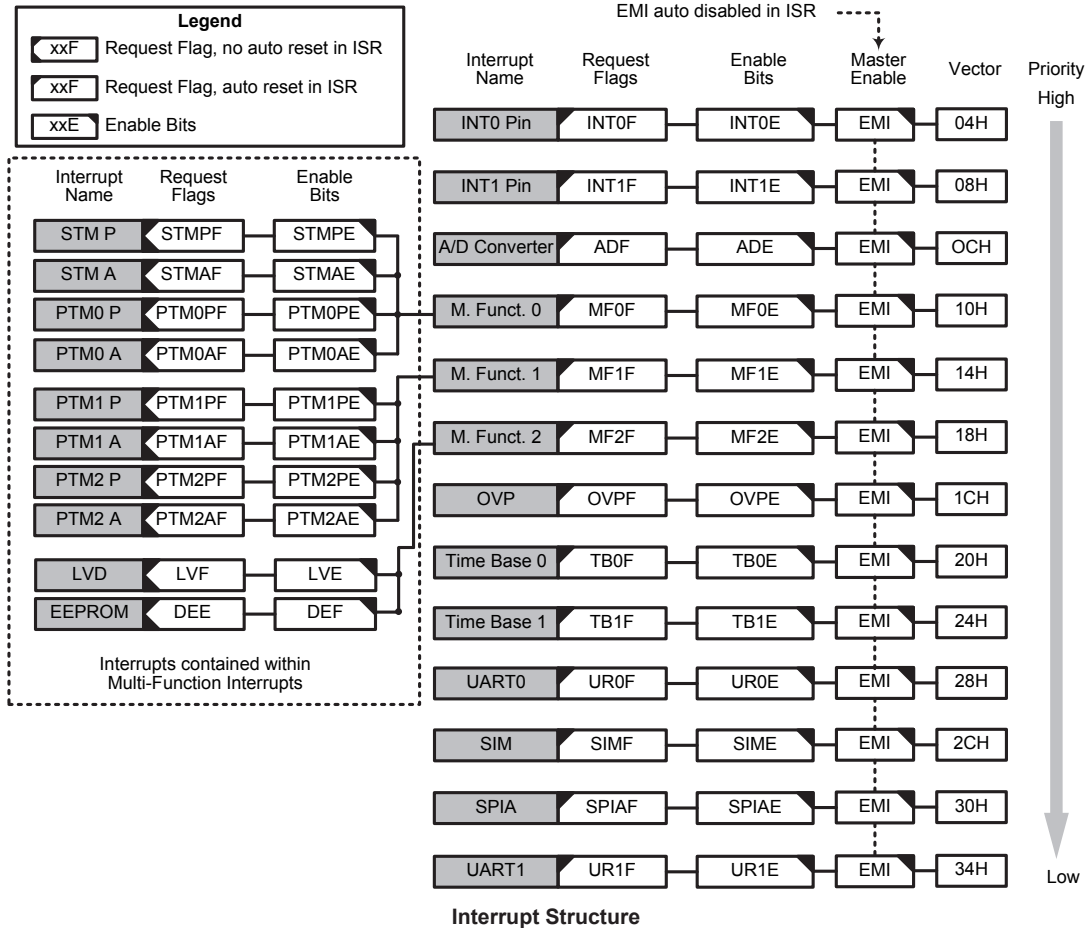   0: Disable
    1: Enable

Interrupt Operation

When the conditions for an interrupt event occur, such as a TM Comparator P, Comparator A match or A/D conversion completion etc., the relevant interrupt request flag will be set. Whether the request flag actually generates a program jump to the relevant interrupt vector is determined by the condition of the interrupt enable bit. If the enable bit is set high then the program will jump to its relevant vector; if the enable bit is zero then although the interrupt request flag is set an actual interrupt will not be generated and the program will not jump to the relevant interrupt vector. The global interrupt enable bit, if cleared to zero, will disable all interrupts.

When an interrupt is generated, the Program Counter, which stores the address of the next instruction to be executed, will be transferred onto the stack. The Program Counter will then be loaded with a new address which will be the value of the corresponding interrupt vector. The microcontroller will then fetch its next instruction from this interrupt vector. The instruction at this vector will usually be a "JMP" which will jump to another section of program which is known as the interrupt service routine. Here is located the code to control the appropriate interrupt. The interrupt service routine must be terminated with a "RETI", which retrieves the original Program Counter address from the stack and allows the microcontroller to continue with normal execution at the point where the interrupt occurred.

The various interrupt enable bits, together with their associated request flags, are shown in the accompanying diagrams with their order of priority. Some interrupt sources have their own individual vector while others share the same multi-function interrupt vector. Once an interrupt subroutine is serviced, all the other interrupts will be blocked, as the global interrupt enable bit, EMI bit will be cleared automatically. This will prevent any further interrupt nesting from occurring. However, if other interrupt requests occur during this interval, although the interrupt will not be immediately serviced, the request flag will still be recorded.

If an interrupt requires immediate servicing while the program is already in another interrupt service routine, the EMI bit should be set after entering the routine, to allow interrupt nesting. If the stack is full, the interrupt request will not be acknowledged, even if the related interrupt is enabled, until the Stack Pointer is decremented. If immediate service is desired, the stack must be prevented from becoming full. In case of simultaneous requests, the accompanying diagram shows the priority that is applied. All of the interrupt request flags when set will wake-up the device if it is in SLEEP or IDLE Mode, however to prevent a wake-up from occurring the corresponding flag should be set before the device is in SLEEP or IDLE Mode.

Legend

xxF	Request Flag, no auto reset in ISR
xxF	Request Flag, auto reset in ISR
xxE	Enable Bits

EMI auto disabled in ISR

Interrupts contained within Multi-Function Interrupts

Interrupt Name	Request Flags	Enable Bits
STM P	STMPF	STMPE
STM A	STMAF	STMAE
PTM0 P	PTM0PF	PTM0PE
PTM0 A	PTM0AF	PTM0AE
PTM1 P	PTM1PF	PTM1PE
PTM1 A	PTM1AF	PTM1AE
PTM2 P	PTM2PF	PTM2PE
PTM2 A	PTM2AF	PTM2AE
LVD	LVF	LVE
EEPROM	DEE	DEF

Interrupt Name	Request Flags	Enable Bits	Master Enable	Vector	Priority
INT0 Pin	INT0F	INT0E	EMI	04H	High
INT1 Pin	INT1F	INT1E	EMI	08H	
A/D Converter	ADF	ADE	EMI	0CH	
M. Funct. 0	MF0F	MF0E	EMI	10H	
M. Funct. 1	MF1F	MF1E	EMI	14H	
M. Funct. 2	MF2F	MF2E	EMI	18H	
OVP	OVPF	OVPE	EMI	1CH	
Time Base 0	TB0F	TB0E	EMI	20H	
Time Base 1	TB1F	TB1E	EMI	24H	
UART0	UR0F	UR0E	EMI	28H	
SIM	SIMF	SIME	EMI	2CH	
SPIA	SPIAF	SPIAE	EMI	30H	
UART1	UR1F	UR1E	EMI	34H	Low

Interrupt Structure

External Interrupts

The external interrupts are controlled by signal transitions on the pins INT0~INT1. An external interrupt request will take place when the external interrupt request flags, INT0F~INT1F, are set, which will occur when a transition, whose type is chosen by the edge select bits, appears on the external interrupt pins. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and respective external interrupt enable bit, INT0E~INT1E, must first be set. Additionally the correct interrupt edge type must be selected using the INTEG register to enable the external interrupt function and to choose the trigger edge type. As the external interrupt pins are pin-shared with I/O pins, they can only be configured as external interrupt pins if their external interrupt enable bit in the corresponding interrupt register has been set and the external interrupt pin is selected by the corresponding pin-shared function selection bits. The pin must also be setup as an input by setting the corresponding bit in the port control register.

When the interrupt is enabled, the stack is not full and the correct transition type appears on the external interrupt pin, a subroutine call to the external interrupt vector, will take place. When the interrupt is serviced, the external interrupt request flags, INT0F~INT1F, will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts. Note that any pull-high resistor selections on the external interrupt pins will remain valid even if the pin is used as an external interrupt input. The INTEG register is used to select the type of active edge that will trigger the external interrupt. A choice of either rising or falling or both edge types can be chosen to trigger an external interrupt. Note that the INTEG register can also be used to disable the external interrupt function.

LVD Interrupt

The Low Voltage Detector Interrupt is contained within the Multi-function Interrupt. An LVD Interrupt request will take place when the LVD Interrupt request flag, LVF, is set, which occurs when the Low Voltage Detector function detects a low power supply voltage or a low LVDIO input voltage. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, Low Voltage Interrupt enable bit, LVE, and associated Multi-function interrupt enable bit, must first be set. When the interrupt is enabled, the stack is not full and a low voltage condition occurs, a subroutine call to the Multi-function Interrupt vector, will take place. When the Low Voltage Interrupt is serviced, the EMI bit will be automatically cleared to disable other interrupts, however only the Multi-function interrupt request flag will be also automatically cleared. As the LVF flag will not be automatically cleared, it has to be cleared by the application program.

EEPROM Interrupt

The EEPROM Interrupt is contained within the Multi-function Interrupt. An EEPROM Interrupt request will take place when the EEPROM Interrupt request flag, DEF, is set, which occurs when an EEPROM Write cycle ends. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and EEPROM Interrupt enable bit, DEE, and associated Multi-function interrupt enable bit, must first be set. When the interrupt is enabled, the stack is not full and an EEPROM Write cycle ends, a subroutine call to the respective EEPROM Interrupt vector will take place. When the EEPROM Interrupt is serviced, the EMI bit will be automatically cleared to disable other interrupts, however only the Multi-function interrupt request flag will be also automatically cleared. As the DEF flag will not be automatically cleared, it has to be cleared by the application program.

A/D Converter Interrupt

The A/D Converter Interrupt is controlled by the termination of an A/D conversion process. An A/D Converter Interrupt request will take place when the A/D Converter Interrupt request flag, ADF, is set, which occurs when the A/D conversion process finishes. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and A/D Interrupt enable bit, ADE, must first be set. When the interrupt is enabled, the stack is not full and the A/D conversion process has ended, a subroutine call to the A/D Converter Interrupt vector, will take place. When the interrupt is serviced, the A/D Converter Interrupt flag, ADF, will be automatically cleared. The EMI bit will also be automatically cleared to disable other interrupts.

Multi-function Interrupts

Within this device there are three Multi-function interrupts. Unlike the other independent interrupts, these interrupts have no independent source, but rather are formed from other existing interrupt sources, namely the TM Interrupts, EEPROM interrupt and LVD interrupt.

A Multi-function interrupt request will take place when any of the Multi-function interrupt request flags, MFnF are set. The Multi-function interrupt flags will be set when any of their included functions generate an interrupt request flag. To allow the program to branch to its respective interrupt vector address, when the Multi-function interrupt is enabled and the stack is not full, and either one of the interrupts contained within each of Multi-function interrupt occurs, a subroutine call to one of the Multi-function interrupt vectors will take place. When the interrupt is serviced, the related Multi-Function request flag will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts.

However, it must be noted that, although the Multi-function Interrupt flags will be automatically reset when the interrupt is serviced, the request flags from the original source of the Multi-function interrupts will not be automatically reset and must be manually reset by the application program.

Serial Interface Module Interrupt

The Serial Interface Module Interrupt is also known as the SIM Interrupt. A SIM Interrupt request will take place when the SIM Interrupt request flag, SIMF, is set, which occurs when a byte of data has been received or transmitted by the SIM interface, an I²C address match or I²C time-out occurrence. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and the Serial Interface Interrupt enable bit, SIME, must first be set. When the interrupt is enabled, the stack is not full and any of the above described situations occurs, a subroutine call to the SIM interrupt vector, will take place. When the SIM Interface Interrupt is serviced, the interrupt request flag, SIMF, will be automatically reset and the EMI bit will be cleared to disable other interrupts.

SPIA Interrupt

The Serial Peripheral Interface Interrupt, also known as the SPIA Interrupt, will take place when the SPIA Interrupt request flag, SPIAF, is set, which occurs when a byte of data has been received or transmitted by the SPIA interface. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and the Serial Interface Interrupt enable bit, SPIAE, must first be set. When the interrupt is enabled, the stack is not full and a byte of data has been transmitted or received by the SPIA interface, a subroutine call to the respective Interrupt vector, will take place. When the interrupt is serviced, the Serial Interface Interrupt flag, SPIAF, will be automatically cleared. The EMI bit will also be automatically cleared to disable other interrupts.

UART Interrupts

Several individual UARTn conditions can generate a UARTn Interrupt. When these conditions exist, a low pulse will be generated to get the attention of the microcontroller. These conditions are a transmitter data register empty, transmitter idle, receiver data available, receiver overrun, address detect and an RXn pin wake-up. To allow the program to branch to the respective interrupt vector addresses, the global interrupt enable bit, EMI, and UARTn Interrupt enable bit, URnE, must first be set. When the interrupt is enabled, the stack is not full and any of these conditions are created, a subroutine call to the UARTn Interrupt vector will take place. When the interrupt is serviced, the UARTn Interrupt flag, URnF, will be automatically cleared. The EMI bit will also be automatically cleared to disable other interrupts. However, the UnSR register flags will be cleared automatically when certain actions are taken by the UARTn, the details of which are given in the UARTn section.

Over Voltage Protection Interrupt

The OVP Interrupt is controlled by detecting the OVP input voltage. An OVP Interrupt request will take place when the OVP Interrupt request flag, OVPF, is set, which occurs when the Over Voltage Protection circuit detects an over voltage condition. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and OVP Interrupt enable bit, OVPE, must first be set. When the interrupt is enabled, the stack is not full and an over voltage is detected, a subroutine call to the OVP Interrupt vector, will take place. When the interrupt is serviced, the OVP Interrupt flag, OVPF, will be automatically cleared. The EMI bit will also be automatically cleared to disable other interrupts.

Time Base Interrupts

The function of the Time Base Interrupts is to provide regular time signal in the form of an internal interrupt. They are controlled by the overflow signals from their respective timer functions. When these happens their respective interrupt request flags, TB0F or TB1F will be set. To allow the program to branch to their respective interrupt vector addresses, the global interrupt enable bit, EMI

and Time Base enable bits, TB0E or TB1E, must first be set. When the interrupt is enabled, the stack is not full and the Time Base overflows, a subroutine call to their respective vector locations will take place. When the interrupt is serviced, the respective interrupt request flag, TB0F or TB1F, will be automatically reset and the EMI bit will be cleared to disable other interrupts.

The purpose of the Time Base Interrupt is to provide an interrupt signal at fixed time periods. Its clock source, f_{PSC}, originates from the internal clock source f_{SYS}, $f_{SYS}/4$ or f_{SUB} and then passes through a divider, the division ratio of which is selected by programming the appropriate bits in the TB0C and TB1C registers to obtain longer interrupt periods whose value ranges. The clock source which in turn controls the Time Base interrupt period is selected using the CLKSEL1~CLKSEL0 bits in the PSCR register.

- **PSCR Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CLKSEL1	CLKSEL0
R/W	—	—	—	—	—	—	R/W	R/W
POR	—	—	—	—	—	—	0	0

Bit 7~2   Unimplemented, read as "0"

Bit 1~0   **CLKSEL1~CLKSEL0**: Prescaler clock source selection
　　　　　　00: f_{SYS}
　　　　　　01: $f_{SYS}/4$
　　　　　　1x: f_{SUB}

- **TB0C Register**

Bit	7	6	5	4	3	2	1	0
Name	TB0ON	—	—	—	—	TB02	TB01	TB00
R/W	R/W	—	—	—	—	R/W	R/W	R/W
POR	0	—	—	—	—	0	0	0

Bit 7   **TB0ON**: Time Base 0 Control
　　　　　0: Disable
　　　　　1: Enable

Bit 6~3   Unimplemented, read as "0"

Bit 2~0   **TB02~TB00**: Select Time Base 0 Time-out Period
　　　　　　000: $2^8/f_{PSC}$
　　　　　　001: $2^9/f_{PSC}$
　　　　　　010: $2^{10}/f_{PSC}$
　　　　　　011: $2^{11}/f_{PSC}$
　　　　　　100: $2^{12}/f_{PSC}$
　　　　　　101: $2^{13}/f_{PSC}$
　　　　　　110: $2^{14}/f_{PSC}$
　　　　　　111: $2^{15}/f_{PSC}$

- **TB1C Register**

Bit	7	6	5	4	3	2	1	0
Name	TB1ON	—	—	—	—	TB12	TB11	TB10
R/W	R/W	—	—	—	—	R/W	R/W	R/W
POR	0	—	—	—	—	0	0	0

Bit 7   **TB1ON**: Time Base 1 Control
　　　　　0: Disable
　　　　　1: Enable

Bit 6~3   Unimplemented, read as "0"

Bit 2~0　　**TB12~TB10**: Select Time Base 1 Time-out Period

000: $2^8/f_{PSC}$
001: $2^9/f_{PSC}$
010: $2^{10}/f_{PSC}$
011: $2^{11}/f_{PSC}$
100: $2^{12}/f_{PSC}$
101: $2^{13}/f_{PSC}$
110: $2^{14}/f_{PSC}$
111: $2^{15}/f_{PSC}$

Time Base Interrupt
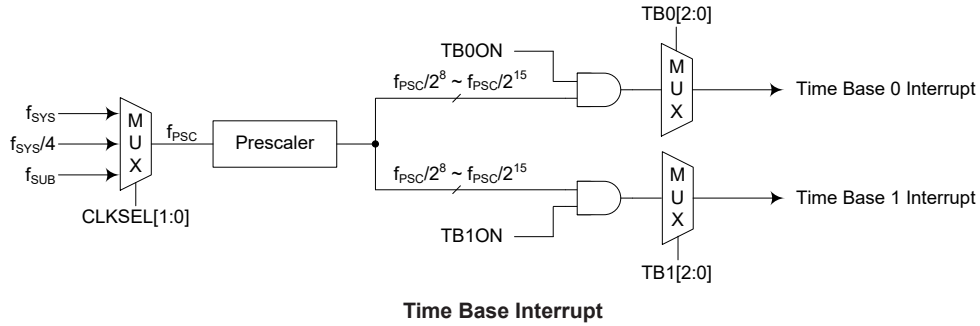
Timer Module Interrupts

Each of the Standard Type TM and Periodic Type TM has two interrupts. All of the TM interrupts are contained within the Multi-function Interrupts. For the Standard Type TM and the Periodic Type TM, each has two interrupt request flags of STMPF, STMAF and PTMnPF, PTMnAF and two enable bits of STMPE, STMAE and PTMnPE, PTMnAE. A TM interrupt request will take place when any of the TM request flags are set, a situation which occurs when a TM comparator P or A match situation happens.

To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, respective TM Interrupt enable bit, and relevant Multi-function Interrupt enable bit, MFnE, must first be set. When the interrupt is enabled, the stack is not full and a TM comparator match situation occurs, a subroutine call to the relevant Multi-function Interrupt vector locations, will take place. When the TM interrupt is serviced, the EMI bit will be automatically cleared to disable other interrupts, however only the related MFnF flag will be automatically cleared. As the TM interrupt request flags will not be automatically cleared, they have to be cleared by the application program.

Interrupt Wake-up Function

Each of the interrupt functions has the capability of waking up the microcontroller when in the SLEEP or IDLE Mode. A wake-up is generated when an interrupt request flag changes from low to high and is independent of whether the interrupt is enabled or not. Therefore, even though the device is in the SLEEP or IDLE Mode and its system oscillator stopped, situations such as external edge transitions on the external interrupt pins or a low power supply voltage may cause their respective interrupt flag to be set high and consequently generate an interrupt. Care must therefore be taken if spurious wake-up situations are to be avoided. If an interrupt wake-up function is to be disabled then the corresponding interrupt request flag should be set high before the device enters the SLEEP or IDLE Mode. The interrupt enable bits have no effect on the interrupt wake-up function.

Programming Considerations

By disabling the relevant interrupt enable bits, a requested interrupt can be prevented from being serviced, however, once an interrupt request flag is set, it will remain in this condition in the interrupt register until the corresponding interrupt is serviced or until the request flag is cleared by the application program.

Where a certain interrupt is contained within a Multi-function interrupt, then when the interrupt service routine is executed, as only the Multi-function interrupt request flags, MFnF, will be automatically cleared, the individual request flag for the function needs to be cleared by the application program.

It is recommended that programs do not use the "CALL" instruction within the interrupt service subroutine. Interrupts often occur in an unpredictable manner or need to be serviced immediately. If only one stack is left and the interrupt is not well controlled, the original control sequence will be damaged once a CALL subroutine is executed in the interrupt subroutine.

Every interrupt has the capability of waking up the microcontroller when it is in SLEEP or IDLE Mode, the wake up being generated when the interrupt request flag changes from low to high. If it is required to prevent a certain interrupt from waking up the microcontroller then its respective request flag should be first set high before enter SLEEP or IDLE Mode.

As only the Program Counter is pushed onto the stack, then when the interrupt is serviced, if the contents of the accumulator, status register or other registers are altered by the interrupt service program, their contents should be saved to the memory at the beginning of the interrupt service routine. To return from an interrupt subroutine, either a RET or RETI instruction may be executed. The RETI instruction in addition to executing a return to the main program also automatically sets the EMI bit high to allow further interrupts. The RET instruction however only executes a return to the main program leaving the EMI bit in its present zero state and therefore disabling the execution of further interrupts.

LCD Driver

For large volume applications, which incorporate an LCD in their design, the use of a custom display rather than a more expensive character based display reduces costs significantly. However, the corresponding COM and SEG signals required, which vary in both amplitude and time, to drive such a custom display require many special considerations for proper LCD operation to occur. This device contains an LCD Driver function, which with their internal LCD signal generating circuitry and various options will automatically generate these time and amplitude varying signals to provide a means of direct driving and easy interfacing to a range of custom LCDs.

This device includes a wide range of options to enable LCD displays of various types to be driven. The table shows the range of options available across the device range.

| Driver No.		Duty	Bias	Bias Type	Wave Type
80LQFP	64LQFP				
48×4	32×4	1/4	1/3	R or C	A or B
46×6	30×6	1/6	1/3	R or C	A or B
44×8	28×8	1/8	1/3	R	A or B
			1/4	R	A or B

LCD Selection

LCD Display Memory

An area of Data Memory is especially reserved for use for the LCD display data. This data area is known as the LCD Memory. Any data written here will be automatically read by the internal display driver circuits, which will in turn automatically generate the necessary LCD driving signals. Therefore any data written into this Memory will be immediately reflected into the actual display connected to the microcontroller.

This device provides an area of embedded data memory for the LCD display. This area is located at 00H to 2FH in Sector 4 of the Data Memory. If using the indirect addressing to access the Display Memory therefore requires first that Sector 4 is selected by writing a value of 04H to MP1H or MP2H. After this, the memory can then be accessed by using indirect addressing through the use of MP1L or MP2L. With Sector 4 selected, then using MP1L/MP2L to read or write to the memory area, from 00H to 2FH, will result in operations to the LCD memory. Directly addressing the Display Memory is not applicable and will result in a data access to the Sector 0 General Purpose Data Memory.

The LCD display memory can be read and written to only by indirect addressing mode using MP1L/MP1H and MP2L/MP2H. When data is written into the display data area, it is automatically read by the LCD driver which then generates the corresponding LCD driving signals. To turn the display on or off, a "1" or a "0" is written to the corresponding bit of the display memory, respectively. The figure illustrates the mapping between the display memory and LCD pattern for the device.

The unimplemented LCD RAM bits cannot be used as general purpose RAM for application. For example, if the LCD duty is selected as 1/4 duty (4COM), the COM bit 4~7 will be read as 0 only.
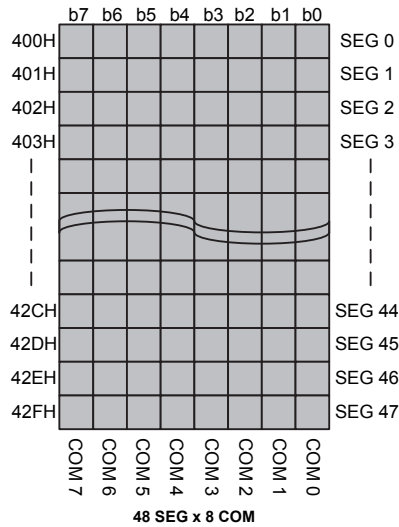
LCD Memory Map

LCD Clock Source

The LCD clock source is the internal clock signal, f_{SUB}, divided by 8, using an internal divider circuit. The f_{SUB} internal clock is supplied by either the LIRC or LXT oscillator, the choice of which is determined by the FSS bit in the SCC register. For proper LCD operation, this arrangement is provided to generate an ideal LCD clock source frequency of 4kHz.

f_{SUB} Clock Source	LCD Clock Frequency
LIRC	4kHz
LXT	4kHz

LCD Clock Source

C type LCD Pump Clock Source

The C-type LCD pump clock source is from the internal clock signal, f_{SUB}, which divided by an internal divider circuit. The divider value can be 2, 4, 8, 16, 32, 64, 128 and is selected by LCDPCK[2:0] bit field in the LCDC2 register.

LCD Registers

Control Registers in the Data Memory, are used to control the various setup features of the LCD Driver. There are several control registers for the LCD function, LCDCP, LCDC0 and LCDC2.

The LCDPR bit in the LCDCP register is used to select the PLCD pin or the internal charge pump regulator to supply the power for the R type LCD COMs and SEGs pins. Bits CPVS1 and CPVS0 in the same register are used to select an appropriate charge pump output voltage level for the R type LCD.

The TYPE bit in the LCDC0 register is used to select whether Type A or Type B LCD control signals are used. The RCT bit in the LCDC0 register is used to select whether R type or C type LCD drive bias. Bits LCDP1 and LCDP0 in the LCDC0 register are used to select the power source to supply the C type LCD panel with the correct bias voltages. Bits LCDIS0 and LCDIS1 in the LCDC0 register are used to select the internal bias current to supply the R type LCD panel with the correct bias voltages. A choice to best match the LCD panel used in the application can be selected also to minimise bias current. The LCDEN bit in the LCDC0 register, which provides the overall LCD enable/disable function, will only be effective when this device is in the Fast, Slow or Idle Mode. If this device is in the Sleep Mode then the display will always be disabled.

The LCDPCK2~LCDPCK0 bits in the LCDC2 register is used to select the C type LCD pump clock divider. The DTYC1~DTYC0 bit field and BIAS bit are used for LCD duty and bias selection.

Register Name	Bit							
	7	6	5	4	3	2	1	0
LCDC0	TYPE	RCT	LCDP1	LCDP0	—	LCDIS1	LCDIS0	LCDEN
LCDCP	—	—	—	—	LCDPR	—	CPVS1	CPVS0
LCDC2	LCDPCK2	LCDPCK1	LCDPCK0	—	—	DTYC1	DTYC0	BIAS

LCD Register List

* **LCDC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	TYPE	RCT	LCDP1	LCDP0	–	LCDIS1	LCDIS0	LCDEN
R/W	R/W	R/W	R/W	R/W	–	R/W	R/W	R/W
POR	0	0	0	0	–	0	0	0

Bit 7   **TYPE**: LCD waveform type selection
     0: Type A
     1: Type B

Bit 6   **RCT**: R or C LCD type control
     0: R type
     1: C type
When C type is selected, LCDPR bit in the LCDCP register should be fixed at 0.
When this bit is clear to 0, the LCDP[1:0] bits should be fixed at "00" and the power source is from the PLCD pin. The C1/C2/V2 pins are pin-shared with I/O or other functions, when the RCT=1, selected I/O or other pin-shared functions will interference with the C1/C2/V2 functions.

Bit 5~4   **LCDP1~LCDP0**: LCD power source selection for C type
     00: The power source is from PLCD/V1/V2
     01: The power source is from V_C = DPN V_{REF} (~1.08V)
     10: The power source is from V_B = 3V
     11: The power source is from V_A = V_{DD}

Bit 3   Unimplemented, read as "0"

Bit 2~1   **LCDIS1~LCDIS0**: LCD Bias Current Selection for R type (V_A=PLCD=V_{DD}, 1/3 bias)
        00: 25μA
        01: 50μA
        10: 100μA
        11: 200μA

Bit 0   **LCDEN**: LCD Enable Control
        0: Disable
        1: Enable

        In the Fast, Slow or Idle mode, the LCD on/off function can be controlled by this bit. In the Sleep mode, the LCD is always off.

- **LCDCP Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	LCDPR	—	CPVS1	CPVS0
R/W	—	—	—	—	R/W	—	R/W	R/W
POR	—	—	—	—	0	—	0	0

Bit 7~4   Unimplemented, read as "0"

Bit 3   **LCDPR**: LCD power source selection for R type
        0: From PLCD pin
        1: From R type Internal charge pump

        This bit is only available for R type LCD applications. When the LCDPR bit is set to 0, the R type LCD power will be derived from the PLCD pin and its internal charge pump circuit will be disabled. This internal charge pump will also be disabled when the C type LCD driver is selected by setting the RCT bit to 1 or the LCD driver is disabled by setting the LCDEN bit to 0.

Bit 2   Unimplemented, read as "0"

Bit 1~0   **CPVS1~CPVS0**: R type charge pump output voltage selection
        00: 3.3V
        01: 3.0V
        10: 2.7V
        11: 4.5V

- **LCDC2 Register**

Bit	7	6	5	4	3	2	1	0
Name	LCDPCK2	LCDPCK1	LCDPCK0	—	—	DTYC1	DTYC0	BIAS
R/W	R/W	R/W	R/W	—	—	R/W	R/W	R/W
POR	0	0	0	—	—	0	0	0

Bit7~5   **LCDPCK2 ~LCDPCK0**: C type LCD pump clock divider selection
        000: 250Hz (divided by 128).
        001: 500Hz (divided by 64)
        010: 1kHz (divided by 32)
        011: 2kHz (divided by 16)
        100: 4kHz (divided by 8).
        101: 8kHz (divided by 4)
        110: 16kHz (divided by 2)
        111: 16kHz (divided by 2)
        The selection is based on the 32kHz LCD clock source.

Bit 4~3   Unimplemented, read as "0"

Bit 2~1   **DTYC1~DTYC0**: LCD duty selection
        00: 1/4 duty (COM0~COM3)
        01: 1/6 duty (COM0~COM5)
        10: 1/8 duty (COM0~COM7), for R type only
        11: unimplemented

The unused COM pins are allowed to be configured as normal I/O or other pin-shared functions.

Bit 0   **BIAS**: LCD bias selection
  0: 1/3 bias
  1: 1/4 bias, for R type only

| Duty	1/3 Bias	1/4 Bias
1/4 (R type + C type)	√	—
1/6 (R type + C type)	√	—
1/8 (R type)	√	√ (Recommended)

Bias-duty Combinations Summary Table

LCD Voltage Source and Biasing

The time and amplitude varying signals generated by the LCD Driver function require the generation of several voltage levels for their operation. The device can have either R type or C type biasing selected via a software control bit RCT. Selecting the C type biasing will enable C type internal charge pump circuitry.

R Type Biasing

For R type biasing the LCD voltage source can be supplied by the PLCD pin input or the internal charge pump regulator, selected by the LCDPR bit in the LCDCP register. When the LCDPR bit is set low, the LCD driver power is supplied by the external PLCD pin. The PLCD pin voltage should be equal to or less than V_{DD} if the PLCD pin is selected to be used. If the LCDPR bit is set high, the LCD driver power is supplied by the internal charge pump circuit. There are four charge pump output voltage levels which are selected by the CPVS1~CPVS0 bits in the LCDCP register. If the internal charge pump circuit is used, an external 4.7μF capacitor should be connected to the external PLCD pin for output voltage stability.
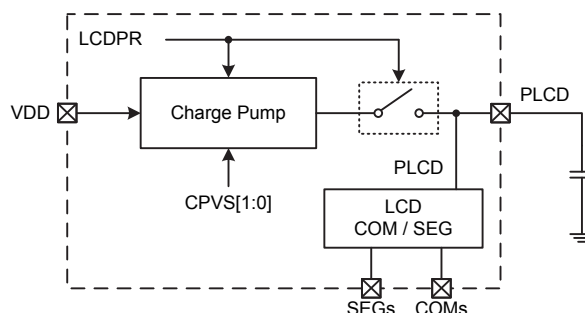
Note: when LCDPR=1, the external 4.7μF capacitor is required, when LCDPR=0, the capacitor can be removed.

R Type LCD Driver Charge Pump Circuit

LCDPR	CPVS[1:0]	R-type LCD Power Source
0	xx	From PLCD pin
1	00	Charge Pump Circuit output, 3.3V
	01	Charge Pump Circuit output, 3.0V
	10	Charge Pump Circuit output, 2.7V
	11	Charge Pump Circuit output, 4.5V

"x": Don't care

R Type LCD Driver Power Supply

For the R type 1/3 bias scheme, four voltage levels of V_{SS}, V_A, V_B and V_C are utilised. The voltage V_A is equal to PLCD. The voltage V_B is equal to PLCD×2/3 while the voltage V_C is equal to PLCD×1/3.

For the R type 1/4 bias scheme, five voltage levels of V_{SS}, V_A, V_B, V_C and V_D are utilised. The voltage V_A is equal to PLCD. The voltage V_B is equal to V_A×3/4, the voltage V_C is equal to V_A×2/4 and the voltage V_D is equal to V_A×1/4.

R Type 1/3 Bias   R Type 1/4 Bias
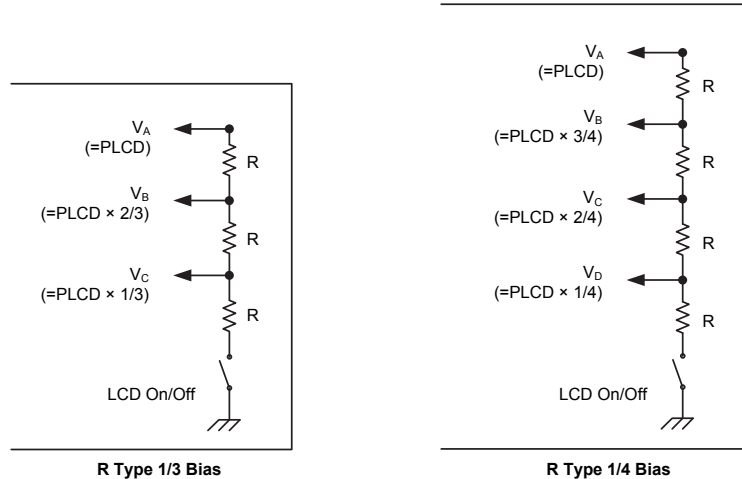
R Type Bias Voltage Generation

Different values of internal bias current can be selected using the LCDIS1~LCDIS0 bits in the LCDC0 register. The connection to the VMAX pin depends upon the voltage that is applied to the PLCD pin. If the V_{DD} voltage is greater than or equal to the voltage applied to the PLCD pin then the VMAX pin should be connected to VDD. Note that for R type biasing the voltage on the PLCD pin should not be greater than the VDD pin voltage.

Condition	VMAX Connection
$V_{DD} \geq$ PLCD	Connect VMAX to VDD
$V_{DD} <$ PLCD	Forbidden condition

R Type Bias VMAX Pin Connection

C Type Biasing

For C type biasing the LCD voltage source can be supplied on the external pin PLCD, V1 or V2 or derived from the internal power source to generate the required biasing voltages. The C type bias voltage source is selected using the LCDP1 and LCDP0 bits in the LCDC0 register.

When the LCD voltage source is from the PLCD pin, the C type biasing scheme uses an internal charge pump circuit, which can generate voltages higher than what is supplied on PLCD. This feature is useful in applications where the microcontroller supply voltage is less than the supply voltage required by the LCD. An additional charge pump capacitor must also be connected between pins C1 and C2 to generate the necessary voltage levels.
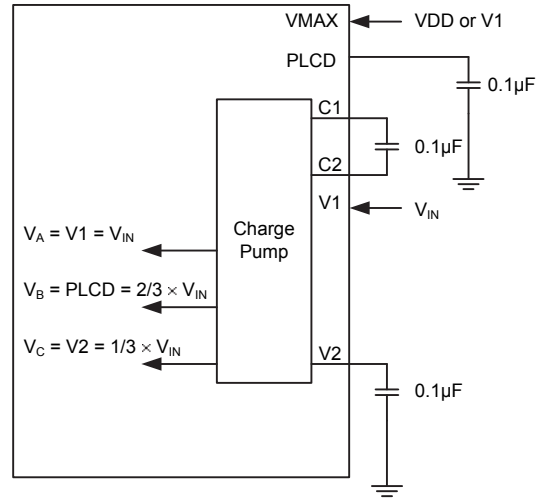
For C type 1/3 bias external power supply scheme, four voltage levels of V_{SS}, V_A, V_B and V_C are utilised. The LCD power can be supplied on PLCD, V1 or V2 pin. The device also has a built-in depletion circuit for LCD voltage source. This could be the DPN V_{REF} (~1.08V) or internal power (V_{DD}) to generate biasing voltage. These bias voltages have different levels depending upon different LCD power supply schemes.

LCDP[1:0]	C-type LCD Power Source		V_A Voltage	V_B Voltage	V_C Voltage
00	External Power Supply	From V1 pin	V_{IN}	$2/3 \times V_{IN}$	$1/3 \times V_{IN}$
		From PLCD pin	$3/2 \times V_{IN}$	V_{IN}	$1/2 \times V_{IN}$
		From V2 pin	$3 \times V_{IN}$	$2 \times V_{IN}$	V_{IN}
11	Internal Power Supply	V_A ($V_A=V_{DD}$)	V_{DD}	$2/3 \times V_{DD}$	$1/3 \times V_{DD}$
10		V_B ($V_B=3V$)	$3/2 \times 3V$	$3V$	$1/2 \times 3V$
01		V_C ($V_C=$DPN V_{REF})	DPN $V_{REF} \times 3$	DPN $V_{REF} \times 2$	DPN V_{REF}

C Type Bias Power Supply Scheme
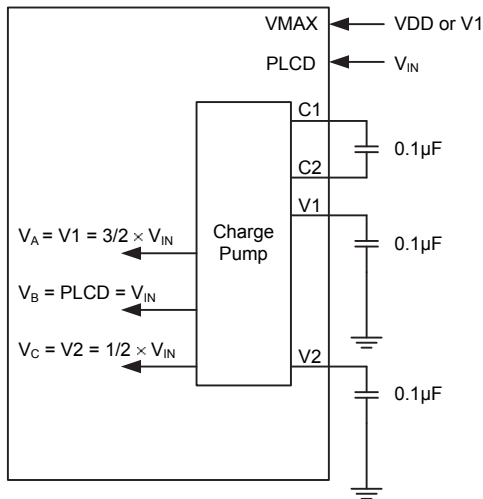
Power Supply from pin PLCD

Power Supply from pin V1
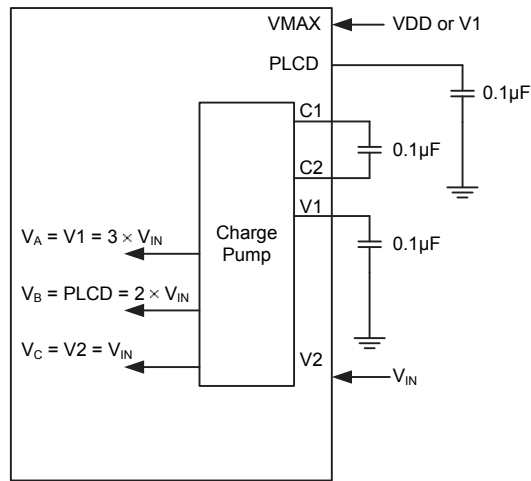
Power Supply from pin V2

Note: The pin VMAX must be connected to the maximum voltage to prevent from the pad leakage.

C Type Bias External Power Supply Configuration – 1/3 Bias
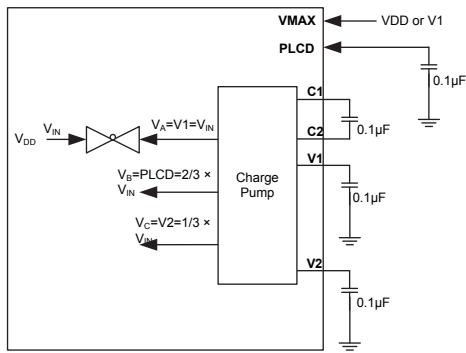
Power Supply from V_A (internal power)
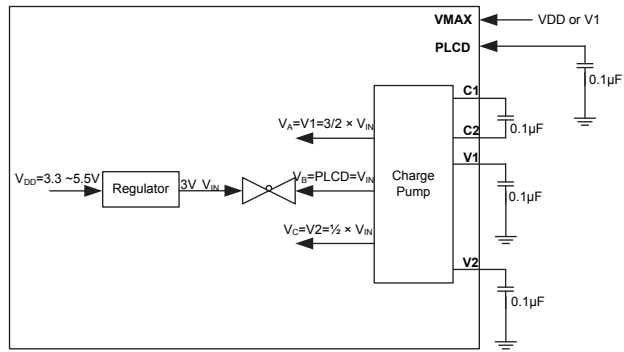
Power Supply from V_B (internal power)
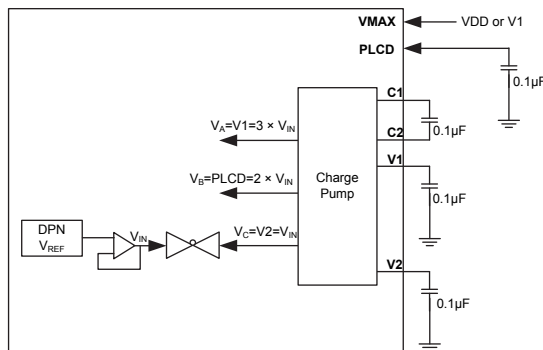
Power Supply from V_C (internal power)

Note: The pin VMAX must connect to the maximum voltage to prevent from the pad leakage.

C Type Bias Internal Power Supply Configuration – 1/3 Bias

The connection to the VMAX pin depends upon the bias and the voltage that is applied to the PLCD pin, the details are shown in the table. It is extremely important to ensure that these charge pump generated internal voltages do not exceed the maximum V_{DD} voltage of 5.5V.

Condition	VMAX Connection
$V_{DD} > PLCD \times 1.5$	Connect VMAX to VDD
Otherwise	Connect VMAX to V1

C Type Bias VMAX Pin Connection

LCD Reset Status

The LCD has an internal reset function that is an OR function of the inverted LCDEN bit in the LCDC0 register and the SLEEP function. Clearing the LCDEN bit to zero will reset the LCD function. The LCD function will also be reset after the device enters the SLEEP mode even if the LCDEN bit is set to 1 to enable the LCD driver function.

When the LCDEN bit is set to 1 to enable the LCD driver and then an MCU reset occurs, the LCD driver will be reset and the COM and SEG outputs will be in a floating state during the MCU reset duration. The reset operation will take a time of $t_{RSTD}+t_{SST}$. Refer to the System Start Up Time Characteristics for t_{RSTD} and t_{SST} details.

MCU Reset	SLEEP Mode	LCDEN	LCD Reset	COM & SEG Voltage Level
No	Off	1	No	Normal Operation
No	Off	0	Yes	Low
No	On	x	Yes	Low
Yes	x	x	Yes	Floating

"x": Don't care.

Note: The watchdog time-out reset in the IDLE or SLEEP Mode is excluded from the MCU Reset conditions.

LCD Reset Status

LCD Driver Output

The number of COM and SEG outputs supplied by the LCD driver, as well as its biasing and wave type selections, are dependent upon how the LCD control bits are programmed. The Bias Type, whether C or R type is also selected by a software control bit.

The nature of Liquid Crystal Displays require that only AC voltages can be applied to their pixels as the application of DC voltages to LCD pixels may cause permanent damage. For this reason the relative contrast of an LCD display is controlled by the actual RMS voltage applied to each pixel, which is equal to the RMS value of the voltage on the COM pin minus the voltage applied to the SEG pin. This differential RMS voltage must be greater than the LCD saturation voltage for the pixel to be on and less than the threshold voltage for the pixel to be off.

The requirement to limit the DC voltage to zero and to control as many pixels as possible with a minimum number of connections requires that both a time and amplitude signal is generated and applied to the application LCD. These time and amplitude varying signals are automatically generated by the LCD driver circuits in the microcontroller. What is known as the duty determines the number of common lines used, which are also known as backplanes or COMs. For example, the duty is 1/4 and equates to a COM number of 4, therefore defines the number of time divisions within each LCD signal frame. Two types of signal generation are also provided, known as Type A and Type B, the required type is selected via the TYPE bit in the LCDC register. Type B offers lower frequency signals, however lower frequencies may introduce flickering and influence display clarity.

R & C Type, 4-COM, 1/3 Bias

LCD Display Off Mode

COM0 ~ COM3

All segment outputs

Normal Operation Mode

COM0

COM1

COM2

COM3

All segments are OFF

COM0 side segments are ON

COM1 side segments are ON

COM2 side segments are ON

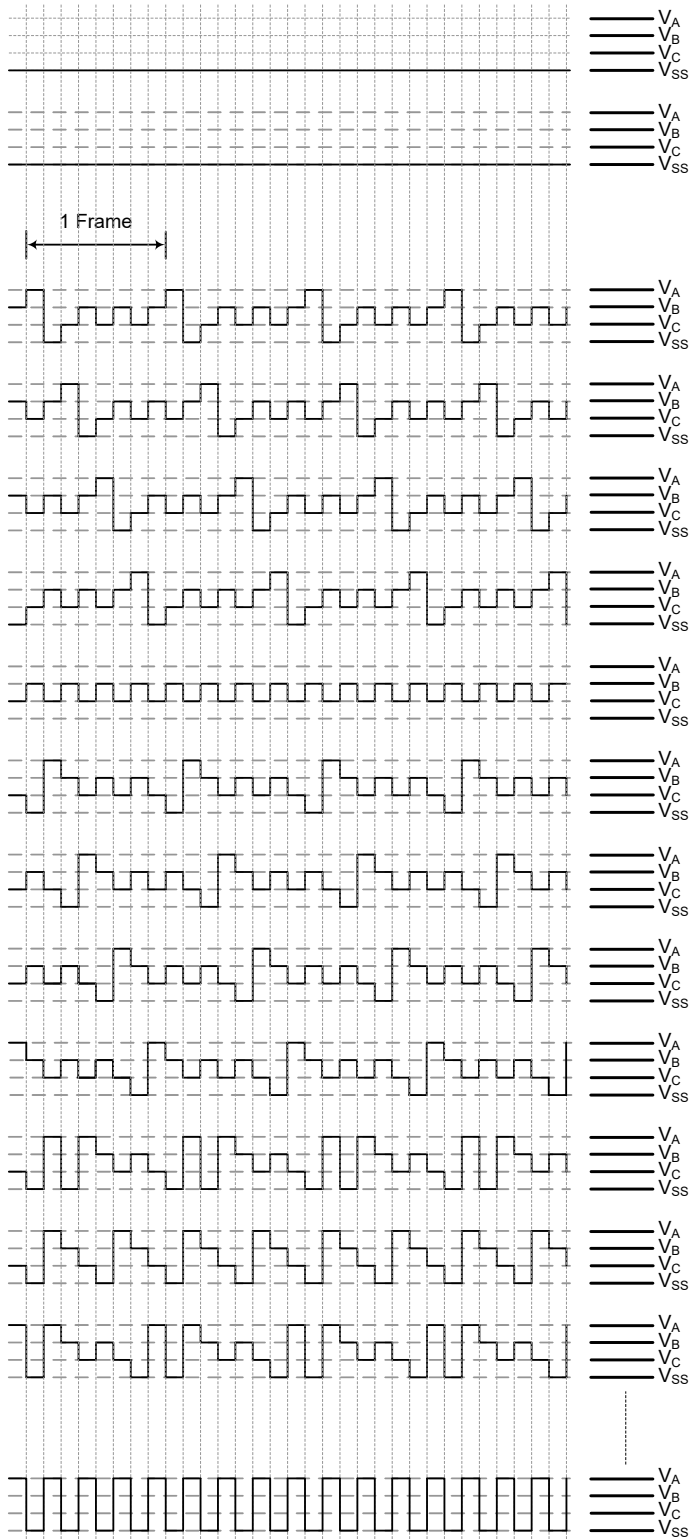COM3 side segments are ON

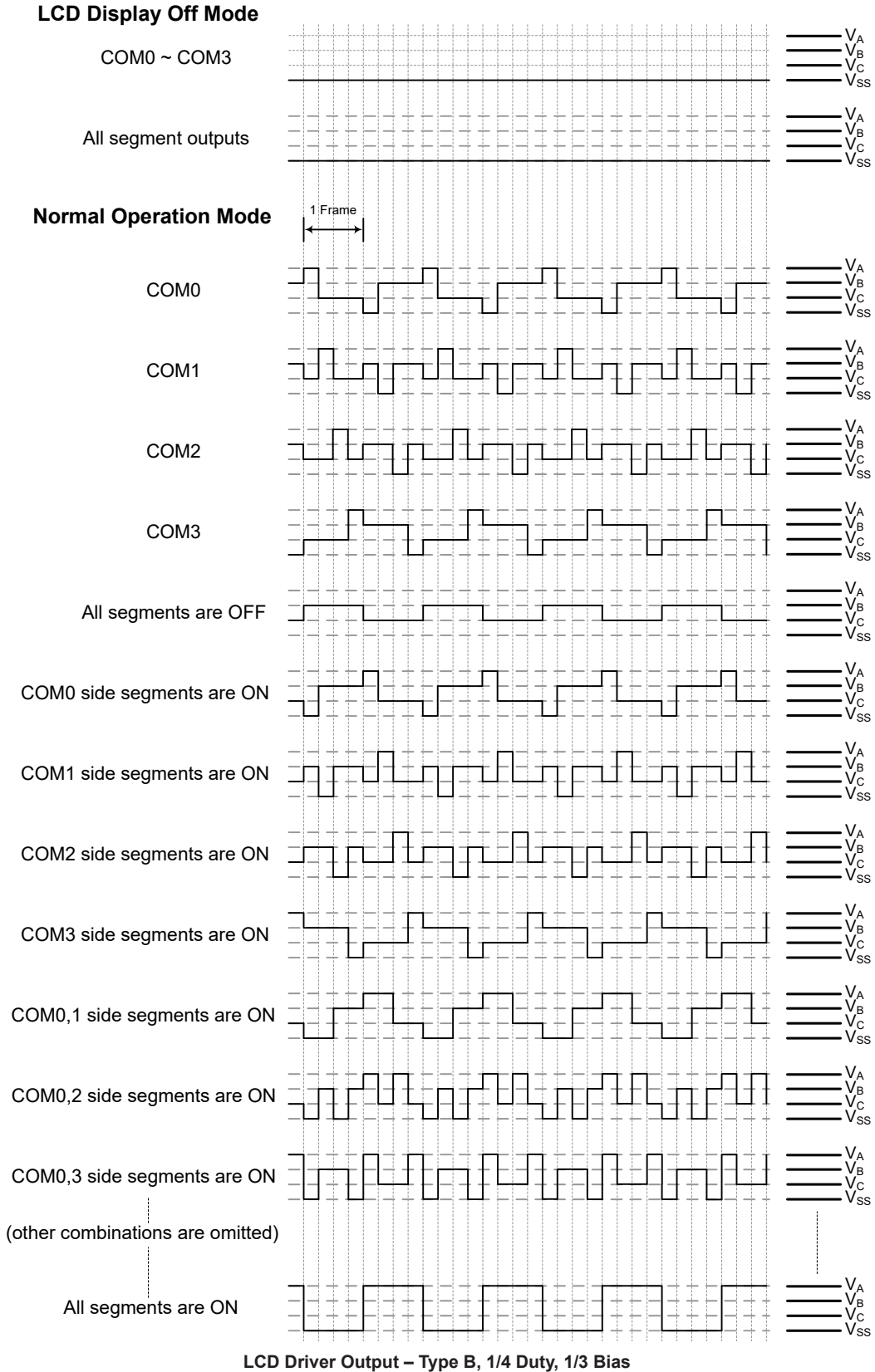COM0,1 side segments are ON

COM0,2 side segments are ON

COM0,3 side segments are ON

(other combinations are omitted)

All segments are ON

LCD Driver Output – Type A, 1/4 Duty, 1/3 Bias

LCD Display Off Mode

COM0 ~ COM3

All segment outputs

Normal Operation Mode

1 Frame

COM0

COM1

COM2

COM3

All segments are OFF

COM0 side segments are ON

COM1 side segments are ON

COM2 side segments are ON

COM3 side segments are ON

COM0,1 side segments are ON

COM0,2 side segments are ON

COM0,3 side segments are ON

(other combinations are omitted)

All segments are ON

LCD Driver Output – Type B, 1/4 Duty, 1/3 Bias

R & C Type, 6-COM, 1/3 Bias

LCD Driver Output – Type A, 1/6 Duty, 1/3 Bias

LCD Display Off Mode

COM0 ~ COM5

All segment outputs

Normal Operation Mode

1 Frame

COM0

COM1

COM2

COM3

COM4

COM5

All segments are OFF

COM0 side segments are ON

COM1 side segments are ON

COM2 side segments are ON

COM3 side segments are ON

COM4 side segments are ON

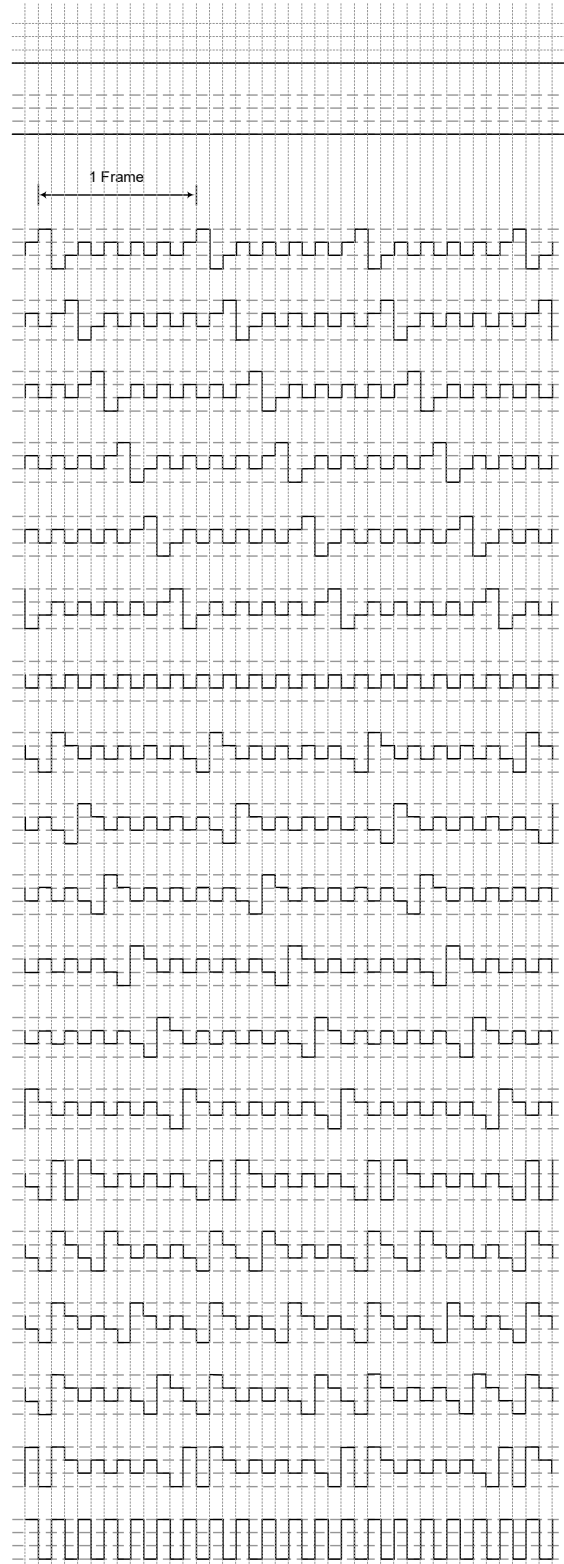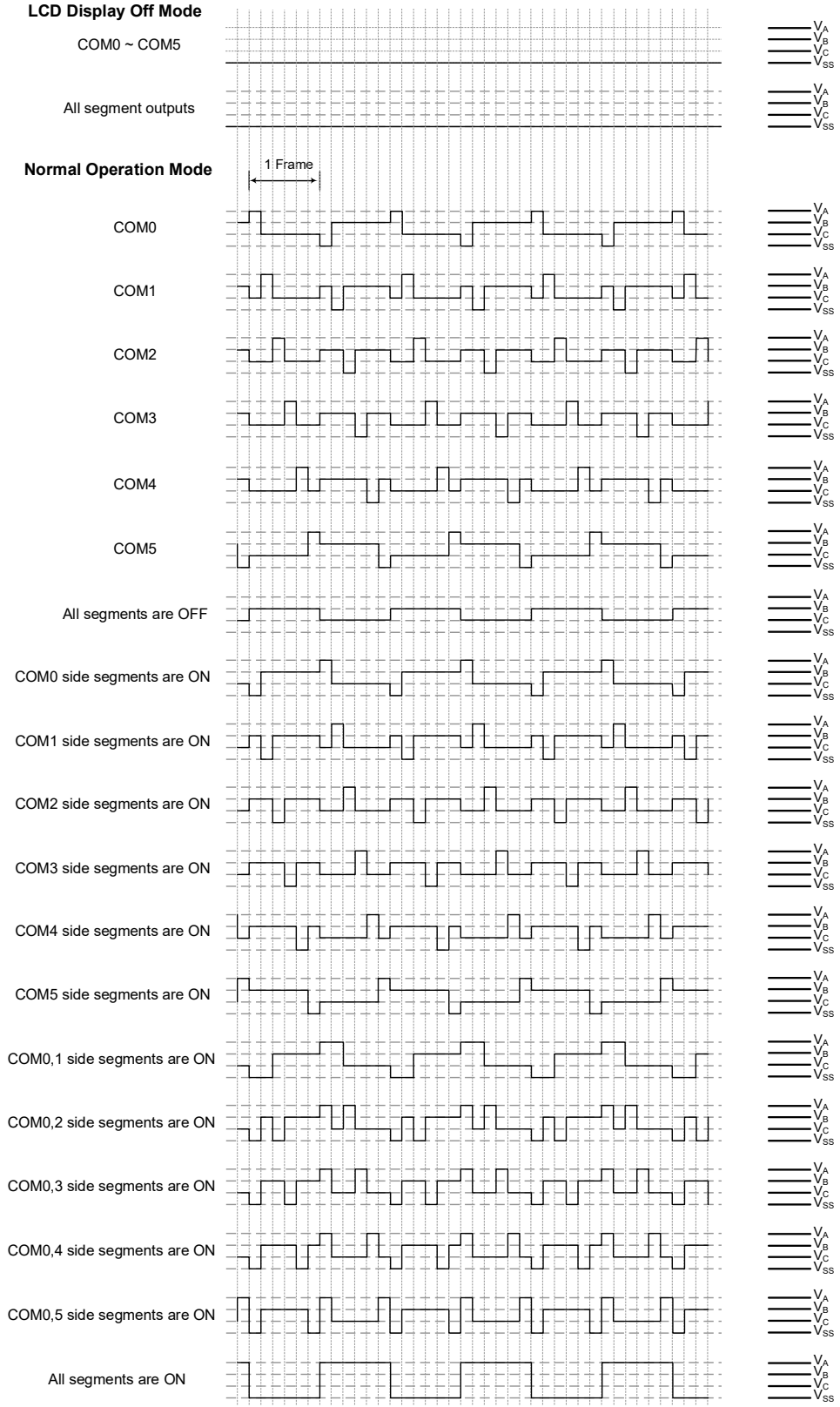COM5 side segments are ON

COM0,1 side segments are ON

COM0,2 side segments are ON

COM0,3 side segments are ON

COM0,4 side segments are ON

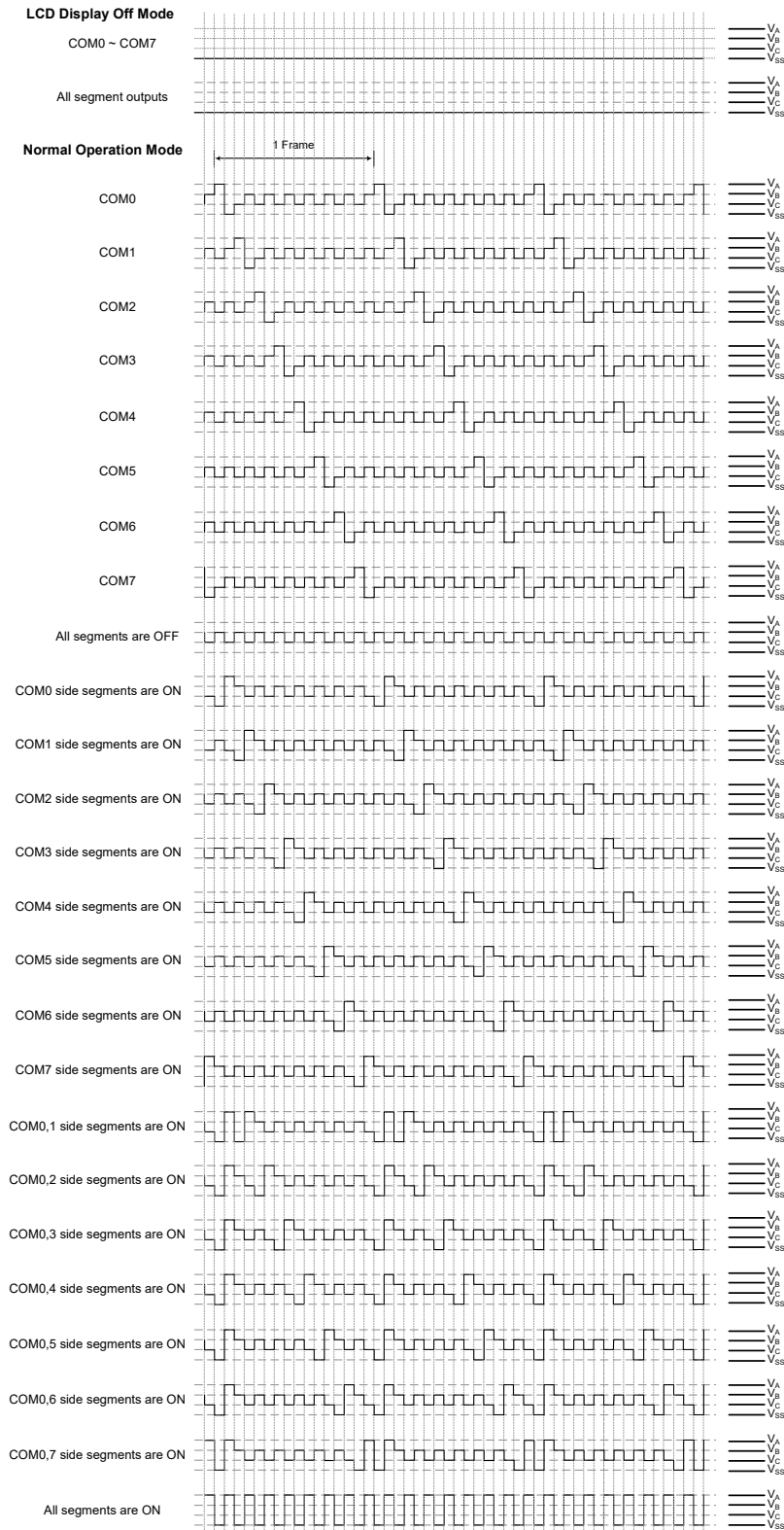COM0,5 side segments are ON

All segments are ON
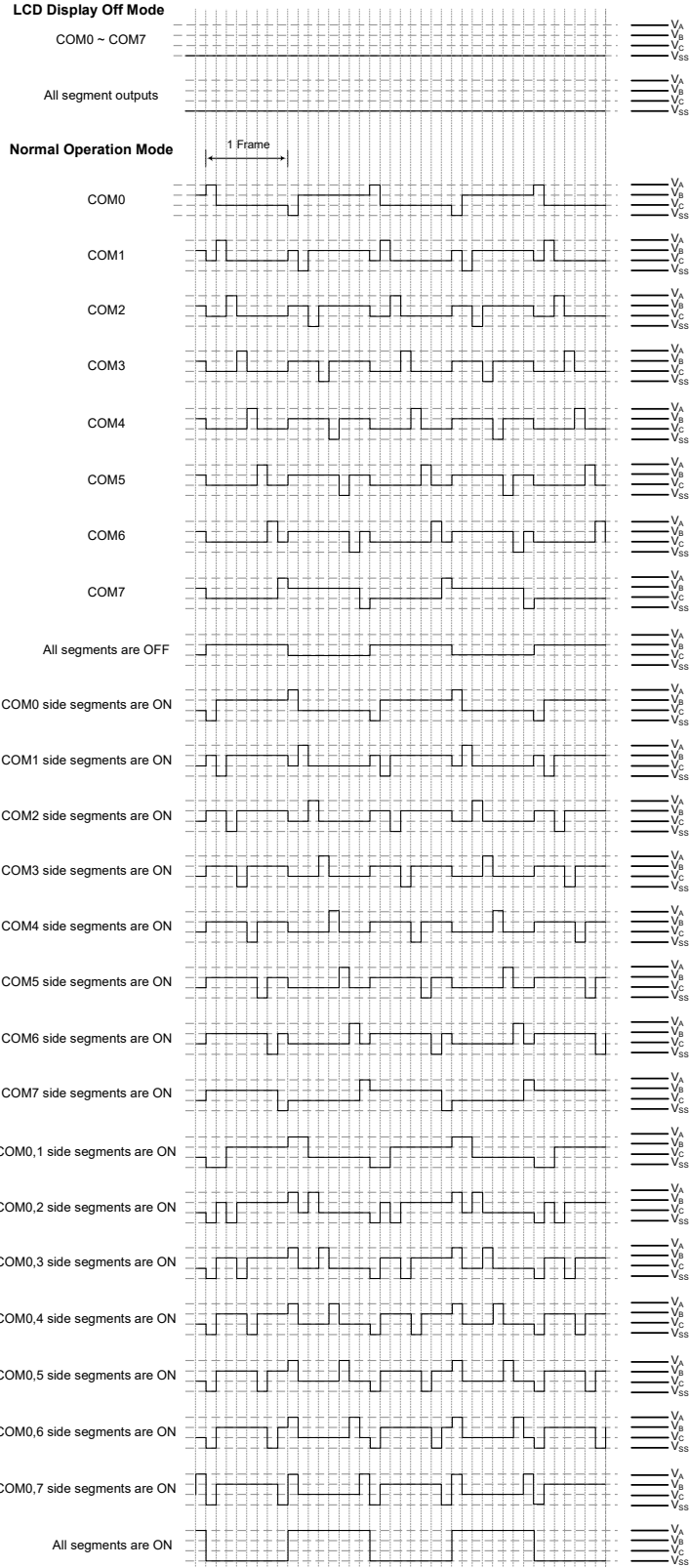
LCD Driver Output – Type B, 1/6 Duty, 1/3 Bias
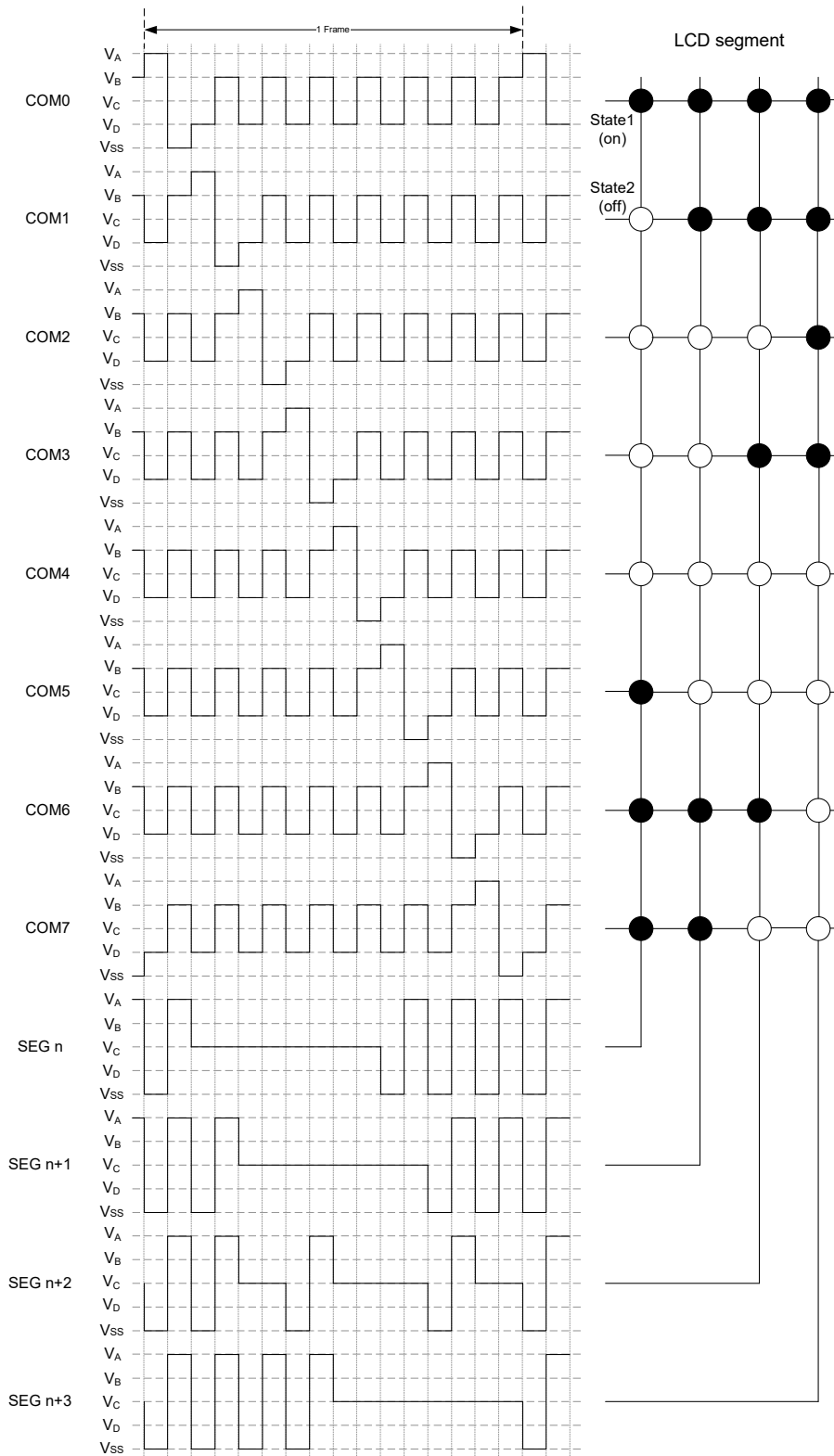
R Type, 8-COM, 1/3 Bias

LCD Driver Output – Type A, 1/8 Duty, 1/3 Bias
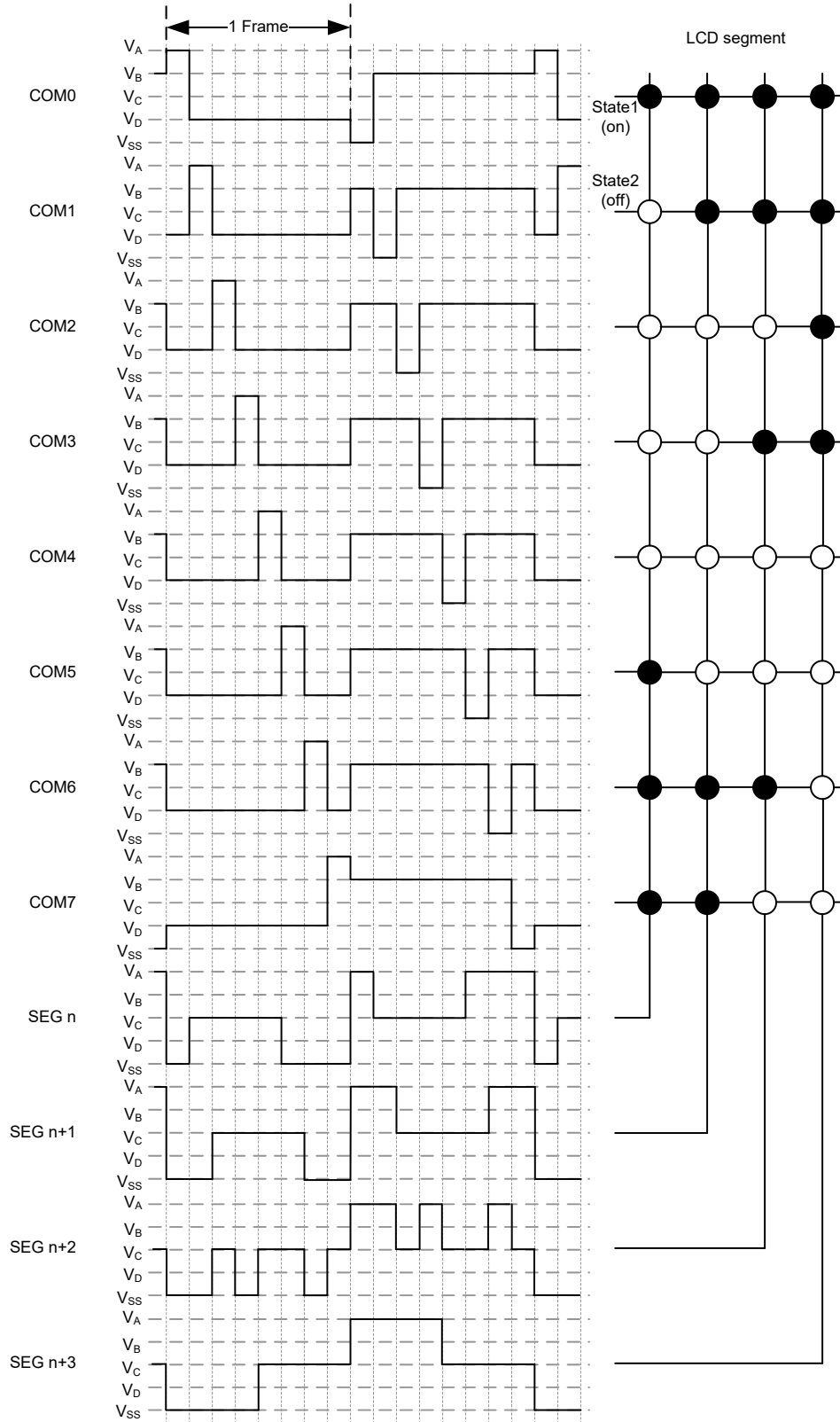
LCD Driver Output – Type B, 1/8 Duty, 1/3 Bias

R Type, 8-COM, 1/4 Bias

LCD Driver Output – Type A, 1/8 Duty, 1/4 Bias

**LCD Driver Output – Type B, 1/8 Duty, 1/4 Bias**

Programming Considerations

Certain precautions must be taken when programming the LCD. One of these is to ensure that the LCD Memory is properly initialised after the microcontroller is powered on. Like the General Purpose Data Memory, the contents of the LCD Memory are in an unknown condition after power-on. As the contents of the LCD Memory will be mapped into the actual display, it is important to initialise this memory area into a known condition soon after applying power to obtain a proper display pattern.

Consideration must also be given to the capacitive load of the actual LCD used in the application. As the load presented to the microcontroller by LCD pixels can be generally modeled as mainly capacitive in nature, it is important that this is not excessive, a point that is particularly true in the case of the COM lines which may be connected to many LCD pixels. The accompanying diagram depicts the equivalent circuit of the LCD.

One additional consideration that must be taken into account is what happens when the microcontroller enters SLEEP Mode. The LCDEN control bit in the LCDC0 register permits the display to be powered off to reduce power consumption. If the microcontroller enters the SLEEP Mode or the LCDEN bit is zero, the driving signals to the display will cease, producing a blank display pattern but reducing any power consumption associated with the LCD.

After Power-on, note that as the LCDEN bit will be cleared to zero, the display function will be disabled.

LCD Panel Equivalent Circuit
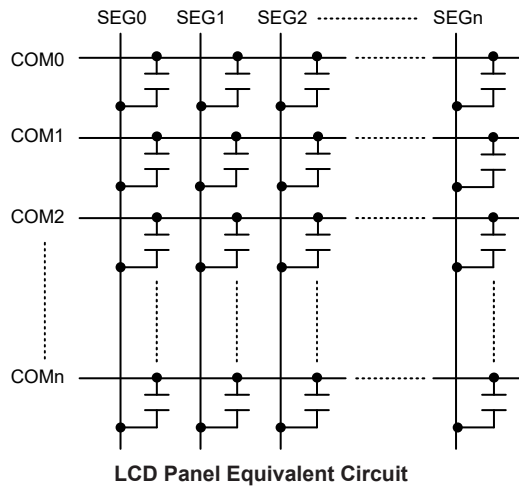
Low Voltage Detector – LVD

The device has a Low Voltage Detector function, also known as LVD. This enabled the device to monitor the power supply voltage, V_{DD}, or LVDIN pin input voltage, and provides a warning signal when it falls below a certain level. This function may be especially useful in battery applications where the supply voltage will gradually reduce as the battery ages, as it allows an early warning battery low signal to be generated. The Low Voltage Detector also has the capability of generating an interrupt signal.

LVD Register

The Low Voltage Detector function is controlled using a single register with the name LVDC. Three bits in this register, VLVD2~VLVD0, are used to select one of eight fixed voltages below which a low voltage condition will be determined. A low voltage condition is indicated when the LVDO bit is set. If the LVDO bit is low, this indicates that the V_{DD} or LVDIN pin input voltage is above the preset low voltage value. The LVDEN bit is used to control the overall on/off function of the low voltage detector. Setting the bit high will enable the low voltage detector. Clearing the bit to zero will switch off the internal low voltage detector circuits. As the low voltage detector will consume a certain amount of power, it may be desirable to switch off the circuit when not in use, an important consideration in power sensitive battery powered applications.

- **LVDC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	LVDO	LVDEN	VBGEN	VLVD2	VLVD1	VLVD0
R/W	—	—	R	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

Bit 7~6　　Unimplemented, read as "0"

Bit 5　　**LVDO**: LVD detection output flag
　　　　　0: No Low Voltage Detected
　　　　　1: Low Voltage Detected

Bit 4　　**LVDEN**: Low Voltage Detector Control
　　　　　0: Disable
　　　　　1: Enable

Bit 3　　**VBGEN**: Bandgap Buffer Control
　　　　　0: Disable
　　　　　1: Enable

Bit 2~0　　**VLVD2~VLVD0**: Select LVD Voltage
　　　　　000: $V_{LVDIN} \leq 1.04V$
　　　　　001: 2.2V
　　　　　010: 2.4V
　　　　　011: 2.7V
　　　　　100: 3.0V
　　　　　101: 3.3V
　　　　　110: 3.6V
　　　　　111: 4.0V

　　　　Note : When the VLVD2~VLVD0 bits are set to 000B, the LVD function will be implemented by comparing the LVDIN pin input voltage with the LVD reference voltage of 1.04V. When the VLVD2~VLVD0 bits are set to any other value except 000B the LVD function will operate by comparing the V_{DD} voltage level with the LVD reference voltage with a specific voltage value which is generated by the internal LVD circuit.

LVD Operation

The Low Voltage Detector function operates by comparing the power supply voltage V_{DD} or LVDIN pin input voltage with a pre-specified voltage level stored in the LVDC register. When the power supply voltage, V_{DD} or LVDIN pin input voltage fall below this pre-determined value, the LVDO bit will be set high indicating a low power supply voltage condition. The Low Voltage Detector function is supplied by a reference voltage which will be automatically enabled. When the device is in the SLEEP mode, the low voltage detector will be disabled even if the LVDEN bit is high. After enabling the Low Voltage Detector, a time delay t_{LVDS} should be allowed for the circuitry to stabilise before reading the LVDO bit. Note also that as the V_{DD} voltage or LVDIN pin input voltage may rise and fall rather slowly, at the voltage nears that of V_{LVD}, there may be multiple bit LVDO transitions.
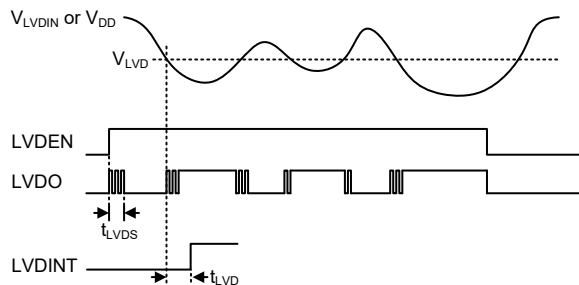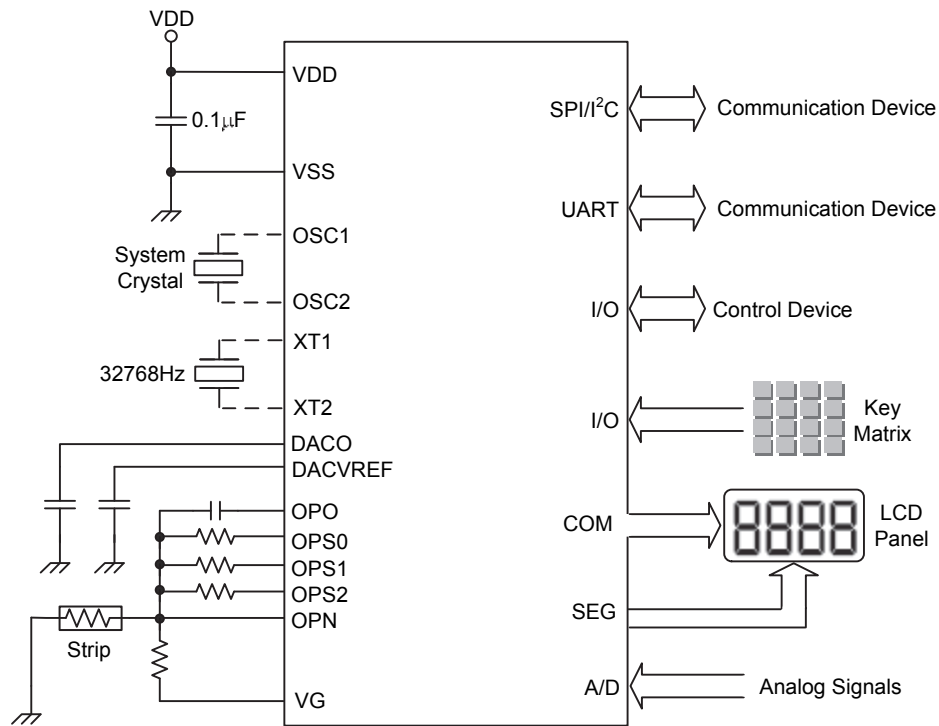

LVD Operation

The Low Voltage Detector interrupt is contained within the Multi-function interrupt, providing an alternative means of low voltage detection, in addition to polling the LVDO bit. The interrupt will only be generated after a delay of t_{LVD} after the LVDO bit has been set high by a low voltage condition. When the device is powered down the Low Voltage Detector will remain active if the LVDEN bit is high. In this case, the LVF interrupt request flag will be set, causing an interrupt to be generated if V_{DD} or LVDIN pin input voltage falls below the preset LVD voltage. This will cause the device to wake-up from the SLEEP or IDLE Mode, however if the Low Voltage Detector wake up function is not required then the LVF flag should be first set high before the device enters the SLEEP or IDLE Mode.

When LVD function is enabled, it is recommenced to clear LVD flag first, and then enables interrupt function to avoid mistake action.

Application Circuits

Instruction Set

Introduction

Central to the successful operation of any microcontroller is its instruction set, which is a set of program instruction codes that directs the microcontroller to perform certain operations. In the case of Holtek microcontroller, a comprehensive and flexible set of over 60 instructions is provided to enable programmers to implement their application with the minimum of programming overheads.

For easier understanding of the various instruction codes, they have been subdivided into several functional groupings.

Instruction Timing

Most instructions are implemented within one instruction cycle. The exceptions to this are branch, call, or table read instructions where two instruction cycles are required. One instruction cycle is equal to 4 system clock cycles, therefore in the case of an 8MHz system oscillator, most instructions would be implemented within 0.5μs and branch or call instructions would be implemented within 1μs. Although instructions which require one more cycle to implement are generally limited to the JMP, CALL, RET, RETI and table read instructions, it is important to realize that any other instructions which involve manipulation of the Program Counter Low register or PCL will also take one more cycle to implement. As instructions which change the contents of the PCL will imply a direct jump to that new address, one more cycle will be required. Examples of such instructions would be "CLR PCL" or "MOV PCL, A". For the case of skip instructions, it must be noted that if the result of the comparison involves a skip operation then this will also take one more cycle, if no skip is involved then only one cycle is required.

Moving and Transferring Data

The transfer of data within the microcontroller program is one of the most frequently used operations. Making use of several kinds of MOV instructions, data can be transferred from registers to the Accumulator and vice-versa as well as being able to move specific immediate data directly into the Accumulator. One of the most important data transfer applications is to receive data from the input ports and transfer data to the output ports.

Arithmetic Operations

The ability to perform certain arithmetic operations and data manipulation is a necessary feature of most microcontroller applications. Within the Holtek microcontroller instruction set are a range of add and subtract instruction mnemonics to enable the necessary arithmetic to be carried out. Care must be taken to ensure correct handling of carry and borrow data when results exceed 255 for addition and less than 0 for subtraction. The increment and decrement instructions such as INC, INCA, DEC and DECA provide a simple means of increasing or decreasing by a value of one of the values in the destination specified.

Logical and Rotate Operation

The standard logical operations such as AND, OR, XOR and CPL all have their own instruction within the Holtek microcontroller instruction set. As with the case of most instructions involving data manipulation, data must pass through the Accumulator which may involve additional programming steps. In all logical data operations, the zero flag may be set if the result of the operation is zero. Another form of logical data manipulation comes from the rotate instructions such as RR, RL, RRC and RLC which provide a simple means of rotating one bit right or left. Different rotate instructions exist depending on program requirements. Rotate instructions are useful for serial port programming applications where data can be rotated from an internal register into the Carry bit from where it can be examined and the necessary serial bit set high or low. Another application which rotate data operations are used is to implement multiplication and division calculations.

Branches and Control Transfer

Program branching takes the form of either jumps to specified locations using the JMP instruction or to a subroutine using the CALL instruction. They differ in the sense that in the case of a subroutine call, the program must return to the instruction immediately when the subroutine has been carried out. This is done by placing a return instruction "RET" in the subroutine which will cause the program to jump back to the address right after the CALL instruction. In the case of a JMP instruction, the program simply jumps to the desired location. There is no requirement to jump back to the original jumping off point as in the case of the CALL instruction. One special and extremely useful set of branch instructions are the conditional branches. Here a decision is first made regarding the condition of a certain data memory or individual bits. Depending upon the conditions, the program will continue with the next instruction or skip over it and jump to the following instruction. These instructions are the key to decision making and branching within the program perhaps determined by the condition of certain input switches or by the condition of internal data bits.

Bit Operations

The ability to provide single bit operations on Data Memory is an extremely flexible feature of all Holtek microcontrollers. This feature is especially useful for output port bit programming where individual bits or port pins can be directly set high or low using either the "SET [m].i" or "CLR [m].i" instructions respectively. The feature removes the need for programmers to first read the 8-bit output port, manipulate the input data to ensure that other bits are not changed and then output the port with the correct new data. This read-modify-write process is taken care of automatically when these bit operation instructions are used.

Table Read Operations

Data storage is normally implemented by using registers. However, when working with large amounts of fixed data, the volume involved often makes it inconvenient to store the fixed data in the Data Memory. To overcome this problem, Holtek microcontrollers allow an area of Program Memory to be setup as a table where data can be directly stored. A set of easy to use instructions provides the means by which this fixed data can be referenced and retrieved from the Program Memory.

Other Operations

In addition to the above functional instructions, a range of other instructions also exist such as the "HALT" instruction for Power-down operations and instructions to control the operation of the Watchdog Timer for reliable program operations under extreme electric or electromagnetic environments. For their relevant operations, refer to the functional related sections.

Instruction Set Summary

The instructions related to the data memory access in the following table can be used when the desired data memory is located in Data Memory sector 0.

Table Conventions

x: Bits immediate data

m: Data Memory address

A: Accumulator

i: 0~7 number of bits

addr: Program memory address

Mnemonic	Description	Cycles	Flag Affected
Arithmetic			
ADD A,[m]	Add Data Memory to ACC	1	Z, C, AC, OV, SC
ADDM A,[m]	Add ACC to Data Memory	1[Note]	Z, C, AC, OV, SC
ADD A,x	Add immediate data to ACC	1	Z, C, AC, OV, SC
ADC A,[m]	Add Data Memory to ACC with Carry	1	Z, C, AC, OV, SC
ADCM A,[m]	Add ACC to Data memory with Carry	1[Note]	Z, C, AC, OV, SC
SUB A,x	Subtract immediate data from the ACC	1	Z, C, AC, OV, SC, CZ
SUB A,[m]	Subtract Data Memory from ACC	1	Z, C, AC, OV, SC, CZ
SUBM A,[m]	Subtract Data Memory from ACC with result in Data Memory	1[Note]	Z, C, AC, OV, SC, CZ
SBC A,x	Subtract immediate data from ACC with Carry	1	Z, C, AC, OV, SC, CZ
SBC A,[m]	Subtract Data Memory from ACC with Carry	1	Z, C, AC, OV, SC, CZ
SBCM A,[m]	Subtract Data Memory from ACC with Carry, result in Data Memory	1[Note]	Z, C, AC, OV, SC, CZ
DAA [m]	Decimal adjust ACC for Addition with result in Data Memory	1[Note]	C
Logic Operation			
AND A,[m]	Logical AND Data Memory to ACC	1	Z
OR A,[m]	Logical OR Data Memory to ACC	1	Z
XOR A,[m]	Logical XOR Data Memory to ACC	1	Z
ANDM A,[m]	Logical AND ACC to Data Memory	1[Note]	Z
ORM A,[m]	Logical OR ACC to Data Memory	1[Note]	Z
XORM A,[m]	Logical XOR ACC to Data Memory	1[Note]	Z
AND A,x	Logical AND immediate Data to ACC	1	Z
OR A,x	Logical OR immediate Data to ACC	1	Z
XOR A,x	Logical XOR immediate Data to ACC	1	Z
CPL [m]	Complement Data Memory	1[Note]	Z
CPLA [m]	Complement Data Memory with result in ACC	1	Z
Increment & Decrement			
INCA [m]	Increment Data Memory with result in ACC	1	Z
INC [m]	Increment Data Memory	1[Note]	Z
DECA [m]	Decrement Data Memory with result in ACC	1	Z
DEC [m]	Decrement Data Memory	1[Note]	Z
Rotate			
RRA [m]	Rotate Data Memory right with result in ACC	1	None
RR [m]	Rotate Data Memory right	1[Note]	None
RRCA [m]	Rotate Data Memory right through Carry with result in ACC	1	C
RRC [m]	Rotate Data Memory right through Carry	1[Note]	C
RLA [m]	Rotate Data Memory left with result in ACC	1	None
RL [m]	Rotate Data Memory left	1[Note]	None
RLCA [m]	Rotate Data Memory left through Carry with result in ACC	1	C
RLC [m]	Rotate Data Memory left through Carry	1[Note]	C

Mnemonic	Description	Cycles	Flag Affected
Data Move			
MOV A,[m]	Move Data Memory to ACC	1	None
MOV [m],A	Move ACC to Data Memory	1[Note]	None
MOV A,x	Move immediate data to ACC	1	None
Bit Operation			
CLR [m].i	Clear bit of Data Memory	1[Note]	None
SET [m].i	Set bit of Data Memory	1[Note]	None
Branch Operation			
JMP addr	Jump unconditionally	2	None
SZ [m]	Skip if Data Memory is zero	1[Note]	None
SZA [m]	Skip if Data Memory is zero with data movement to ACC	1[Note]	None
SZ [m].i	Skip if bit i of Data Memory is zero	1[Note]	None
SNZ [m]	Skip if Data Memory is not zero	1[Note]	None
SNZ [m].i	Skip if bit i of Data Memory is not zero	1[Note]	None
SIZ [m]	Skip if increment Data Memory is zero	1[Note]	None
SDZ [m]	Skip if decrement Data Memory is zero	1[Note]	None
SIZA [m]	Skip if increment Data Memory is zero with result in ACC	1[Note]	None
SDZA [m]	Skip if decrement Data Memory is zero with result in ACC	1[Note]	None
CALL addr	Subroutine call	2	None
RET	Return from subroutine	2	None
RET A,x	Return from subroutine and load immediate data to ACC	2	None
RETI	Return from interrupt	2	None
Table Read Operation			
TABRD [m]	Read table (specific page) to TBLH and Data Memory	2[Note]	None
TABRDL [m]	Read table (last page) to TBLH and Data Memory	2[Note]	None
ITABRD [m]	Increment table pointer TBLP first and Read table (specific page) to TBLH and Data Memory	2[Note]	None
ITABRDL [m]	Increment table pointer TBLP first and Read table (last page) to TBLH and Data Memory	2[Note]	None
Miscellaneous			
NOP	No operation	1	None
CLR [m]	Clear Data Memory	1[Note]	None
SET [m]	Set Data Memory	1[Note]	None
CLR WDT	Clear Watchdog Timer	1	TO, PDF
SWAP [m]	Swap nibbles of Data Memory	1[Note]	None
SWAPA [m]	Swap nibbles of Data Memory with result in ACC	1	None
HALT	Enter power down mode	1	TO, PDF

Note: 1. For skip instructions, if the result of the comparison involves a skip then two cycles are required, if no skip takes place only one cycle is required.

2. Any instruction which changes the contents of the PCL will also require 2 cycles for execution.

Extended Instruction Set

The extended instructions are used to support the full range address access for the data memory. When the accessed data memory is located in any data memory sector except sector 0, the extended instruction can be used to directly access the data memory instead of using the indirect addressing access. This can not only reduce the use of Flash memory space but also improve the CPU execution efficiency.

Mnemonic	Description	Cycles	Flag Affected
Arithmetic			
LADD A,[m]	Add Data Memory to ACC	2	Z, C, AC, OV, SC
LADDM A,[m]	Add ACC to Data Memory	2[Note]	Z, C, AC, OV, SC
LADC A,[m]	Add Data Memory to ACC with Carry	2	Z, C, AC, OV, SC
LADCM A,[m]	Add ACC to Data memory with Carry	2[Note]	Z, C, AC, OV, SC
LSUB A,[m]	Subtract Data Memory from ACC	2	Z, C, AC, OV, SC, CZ
LSUBM A,[m]	Subtract Data Memory from ACC with result in Data Memory	2[Note]	Z, C, AC, OV, SC, CZ
LSBC A,[m]	Subtract Data Memory from ACC with Carry	2	Z, C, AC, OV, SC, CZ
LSBCM A,[m]	Subtract Data Memory from ACC with Carry, result in Data Memory	2[Note]	Z, C, AC, OV, SC, CZ
LDAA [m]	Decimal adjust ACC for Addition with result in Data Memory	2[Note]	C
Logic Operation			
LAND A,[m]	Logical AND Data Memory to ACC	2	Z
LOR A,[m]	Logical OR Data Memory to ACC	2	Z
LXOR A,[m]	Logical XOR Data Memory to ACC	2	Z
LANDM A,[m]	Logical AND ACC to Data Memory	2[Note]	Z
LORM A,[m]	Logical OR ACC to Data Memory	2[Note]	Z
LXORM A,[m]	Logical XOR ACC to Data Memory	2[Note]	Z
LCPL [m]	Complement Data Memory	2[Note]	Z
LCPLA [m]	Complement Data Memory with result in ACC	2	Z
Increment & Decrement			
LINCA [m]	Increment Data Memory with result in ACC	2	Z
LINC [m]	Increment Data Memory	2[Note]	Z
LDECA [m]	Decrement Data Memory with result in ACC	2	Z
LDEC [m]	Decrement Data Memory	2[Note]	Z
Rotate			
LRRA [m]	Rotate Data Memory right with result in ACC	2	None
LRR [m]	Rotate Data Memory right	2[Note]	None
LRRCA [m]	Rotate Data Memory right through Carry with result in ACC	2	C
LRRC [m]	Rotate Data Memory right through Carry	2[Note]	C
LRLA [m]	Rotate Data Memory left with result in ACC	2	None
LRL [m]	Rotate Data Memory left	2[Note]	None
LRLCA [m]	Rotate Data Memory left through Carry with result in ACC	2	C
LRLC [m]	Rotate Data Memory left through Carry	2[Note]	C
Data Move			
LMOV A,[m]	Move Data Memory to ACC	2	None
LMOV [m],A	Move ACC to Data Memory	2[Note]	None
Bit Operation			
LCLR [m].i	Clear bit of Data Memory	2[Note]	None
LSET [m].i	Set bit of Data Memory	2[Note]	None

Mnemonic	Description	Cycles	Flag Affected
Branch			
LSZ [m]	Skip if Data Memory is zero	2[Note]	None
LSZA [m]	Skip if Data Memory is zero with data movement to ACC	2[Note]	None
LSNZ [m]	Skip if Data Memory is not zero	2[Note]	None
LSZ [m].i	Skip if bit i of Data Memory is zero	2[Note]	None
LSNZ [m].i	Skip if bit i of Data Memory is not zero	2[Note]	None
LSIZ [m]	Skip if increment Data Memory is zero	2[Note]	None
LSDZ [m]	Skip if decrement Data Memory is zero	2[Note]	None
LSIZA [m]	Skip if increment Data Memory is zero with result in ACC	2[Note]	None
LSDZA [m]	Skip if decrement Data Memory is zero with result in ACC	2[Note]	None
Table Read			
LTABRD [m]	Read table (specific page) to TBLH and Data Memory	3[Note]	None
LTABRDL [m]	Read table (last page) to TBLH and Data Memory	3[Note]	None
LITABRD [m]	Increment table pointer TBLP first and Read table (specific page) to TBLH and Data Memory	3[Note]	None
LITABRDL [m]	Increment table pointer TBLP first and Read table (last page) to TBLH and Data Memory	3[Note]	None
Miscellaneous			
LCLR [m]	Clear Data Memory	2[Note]	None
LSET [m]	Set Data Memory	2[Note]	None
LSWAP [m]	Swap nibbles of Data Memory	2[Note]	None
LSWAPA [m]	Swap nibbles of Data Memory with result in ACC	2	None

Note: 1. For these extended skip instructions, if the result of the comparison involves a skip then three cycles are required, if no skip takes place two cycles is required.

2. Any extended instruction which changes the contents of the PCL register will also require three cycles for execution.

Instruction Definition

ADC A,[m]   Add Data Memory to ACC with Carry

Description   The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the Accumulator.

Operation $ACC \leftarrow ACC + [m] + C$

Affected flag(s)   OV, Z, AC, C, SC

ADCM A,[m]   Add ACC to Data Memory with Carry

Description   The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the specified Data Memory.

Operation $[m] \leftarrow ACC + [m] + C$

Affected flag(s)   OV, Z, AC, C, SC

ADD A,[m]   Add Data Memory to ACC

Description   The contents of the specified Data Memory and the Accumulator are added. The result is stored in the Accumulator.

Operation $ACC \leftarrow ACC + [m]$

Affected flag(s)   OV, Z, AC, C, SC

ADD A,x   Add immediate data to ACC

Description   The contents of the Accumulator and the specified immediate data are added. The result is stored in the Accumulator.

Operation $ACC \leftarrow ACC + x$

Affected flag(s)   OV, Z, AC, C, SC

ADDM A,[m]   Add ACC to Data Memory

Description   The contents of the specified Data Memory and the Accumulator are added. The result is stored in the specified Data Memory.

Operation $[m] \leftarrow ACC + [m]$

Affected flag(s)   OV, Z, AC, C, SC

AND A,[m]   Logical AND Data Memory to ACC

Description   Data in the Accumulator and the specified Data Memory perform a bitwise logical AND operation. The result is stored in the Accumulator.

Operation $ACC \leftarrow ACC \ ''AND'' \ [m]$

Affected flag(s)   Z

AND A,x   Logical AND immediate data to ACC

Description   Data in the Accumulator and the specified immediate data perform a bit wise logical AND operation. The result is stored in the Accumulator.

Operation $ACC \leftarrow ACC \ ''AND'' \ x$

Affected flag(s)   Z

ANDM A,[m]   Logical AND ACC to Data Memory

Description   Data in the specified Data Memory and the Accumulator perform a bitwise logical AND operation. The result is stored in the Data Memory.

Operation $[m] \leftarrow ACC \ ''AND'' \ [m]$

Affected flag(s)   Z

CALL addr	Subroutine call
Description	Unconditionally calls a subroutine at the specified address. The Program Counter then increments by 1 to obtain the address of the next instruction which is then pushed onto the stack. The specified address is then loaded and the program continues execution from this new address. As this instruction requires an additional operation, it is a two cycle instruction.
Operation	Stack ← Program Counter + 1
	Program Counter ← addr
Affected flag(s)	None

CLR [m]	Clear Data Memory
Description	Each bit of the specified Data Memory is cleared to 0.
Operation	[m] ← 00H
Affected flag(s)	None

CLR [m].i	Clear bit of Data Memory
Description	Bit i of the specified Data Memory is cleared to 0.
Operation	[m].i ← 0
Affected flag(s)	None

CLR WDT	Clear Watchdog Timer
Description	The TO, PDF flags and the WDT are all cleared.
Operation	WDT cleared
	TO ← 0
	PDF ← 0
Affected flag(s)	TO, PDF

CPL [m]	Complement Data Memory
Description	Each bit of the specified Data Memory is logically complemented (1′s complement). Bits which previously contained a 1 are changed to 0 and vice versa.
Operation	[m] ← $\overline{[m]}$
Affected flag(s)	Z

CPLA [m]	Complement Data Memory with result in ACC
Description	Each bit of the specified Data Memory is logically complemented (1′s complement). Bits which previously contained a 1 are changed to 0 and vice versa. The complemented result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	ACC ← $\overline{[m]}$
Affected flag(s)	Z

DAA [m]	Decimal-Adjust ACC for addition with result in Data Memory
Description	Convert the contents of the Accumulator value to a BCD (Binary Coded Decimal) value resulting from the previous addition of two BCD variables. If the low nibble is greater than 9 or if AC flag is set, then a value of 6 will be added to the low nibble. Otherwise the low nibble remains unchanged. If the high nibble is greater than 9 or if the C flag is set, then a value of 6 will be added to the high nibble. Essentially, the decimal conversion is performed by adding 00H, 06H, 60H or 66H depending on the Accumulator and flag conditions. Only the C flag may be affected by this instruction which indicates that if the original BCD sum is greater than 100, it allows multiple precision decimal addition.
Operation	[m] ← ACC + 00H or
	[m] ← ACC + 06H or
	[m] ← ACC + 60H or
	[m] ← ACC + 66H
Affected flag(s)	C

DEC [m]

Description	Data in the specified Data Memory is decremented by 1.
Operation	$[m] \leftarrow [m] - 1$
Affected flag(s)	Z

DECA [m]   Decrement Data Memory with result in ACC

Description	Data in the specified Data Memory is decremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	$ACC \leftarrow [m] - 1$
Affected flag(s)	Z

HALT   Enter power down mode

Description	This instruction stops the program execution and turns off the system clock. The contents of the Data Memory and registers are retained. The WDT and prescaler are cleared. The power down flag PDF is set and the WDT time-out flag TO is cleared.
Operation	$TO \leftarrow 0$ $PDF \leftarrow 1$
Affected flag(s)	TO, PDF

INC [m]   Increment Data Memory

Description	Data in the specified Data Memory is incremented by 1.
Operation	$[m] \leftarrow [m] + 1$
Affected flag(s)	Z

INCA [m]   Increment Data Memory with result in ACC

Description	Data in the specified Data Memory is incremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	$ACC \leftarrow [m] + 1$
Affected flag(s)	Z

JMP addr   Jump unconditionally

Description	The contents of the Program Counter are replaced with the specified address. Program execution then continues from this new address. As this requires the insertion of a dummy instruction while the new address is loaded, it is a two cycle instruction.
Operation	Program Counter $\leftarrow$ addr
Affected flag(s)	None

MOV A,[m]   Move Data Memory to ACC

Description	The contents of the specified Data Memory are copied to the Accumulator.
Operation	$ACC \leftarrow [m]$
Affected flag(s)	None

MOV A,x   Move immediate data to ACC

Description	The immediate data specified is loaded into the Accumulator.
Operation	$ACC \leftarrow x$
Affected flag(s)	None

MOV [m],A   Move ACC to Data Memory

Description	The contents of the Accumulator are copied to the specified Data Memory.
Operation	$[m] \leftarrow ACC$
Affected flag(s)	None

NOP	No operation
Description	No operation is performed. Execution continues with the next instruction.
Operation	No operation
Affected flag(s)	None

OR A,[m]	Logical OR Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical OR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″OR″ [m]
Affected flag(s)	Z

OR A,x	Logical OR immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bitwise logical OR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″OR″ x
Affected flag(s)	Z

ORM A,[m]	Logical OR ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical OR operation. The result is stored in the Data Memory.
Operation	[m] ← ACC ″OR″ [m]
Affected flag(s)	Z

RET	Return from subroutine
Description	The Program Counter is restored from the stack. Program execution continues at the restored address.
Operation	Program Counter ← Stack
Affected flag(s)	None

RET A,x	Return from subroutine and load immediate data to ACC
Description	The Program Counter is restored from the stack and the Accumulator loaded with the specified immediate data. Program execution continues at the restored address.
Operation	Program Counter ← Stack ACC ← x
Affected flag(s)	None

RETI	Return from interrupt
Description	The Program Counter is restored from the stack and the interrupts are re-enabled by setting the EMI bit. EMI is the master interrupt global enable bit. If an interrupt was pending when the RETI instruction is executed, the pending Interrupt routine will be processed before returning to the main program.
Operation	Program Counter ← Stack EMI ← 1
Affected flag(s)	None

RL [m]	Rotate Data Memory left
Description	The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0.
Operation	[m].(i+1) ← [m].i; (i=0~6) [m].0 ← [m].7
Affected flag(s)	None

RLA [m]	Rotate Data Memory left with result in ACC
Description	The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	ACC.(i+1) ← [m].i; (i=0~6) ACC.0 ← [m].7
Affected flag(s)	None

RLC [m]	Rotate Data Memory left through Carry
Description	The contents of the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into bit 0.
Operation	[m].(i+1) ← [m].i; (i=0~6) [m].0 ← C C ← [m].7
Affected flag(s)	C

RLCA [m]	Rotate Data Memory left through Carry with result in ACC
Description	Data in the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into the bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	ACC.(i+1) ← [m].i; (i=0~6) ACC.0 ← C C ← [m].7
Affected flag(s)	C

RR [m]	Rotate Data Memory right
Description	The contents of the specified Data Memory are rotated right by 1 bit with bit 0 rotated into bit 7.
Operation	[m].i ← [m].(i+1); (i=0~6) [m].7 ← [m].0
Affected flag(s)	None

RRA [m]	Rotate Data Memory right with result in ACC
Description	Data in the specified Data Memory is rotated right by 1 bit with bit 0 rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	ACC.i ← [m].(i+1); (i=0~6) ACC.7 ← [m].0
Affected flag(s)	None

RRC [m]	Rotate Data Memory right through Carry
Description	The contents of the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7.
Operation	[m].i ← [m].(i+1); (i=0~6) [m].7 ← C C ← [m].0
Affected flag(s)	C

RRCA [m]   Rotate Data Memory right through Carry with result in ACC

Description   Data in the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces
                 the Carry bit and the original carry flag is rotated into bit 7. The rotated result is stored in the
                 Accumulator and the contents of the Data Memory remain unchanged.

Operation $ACC.i \leftarrow [m].(i+1); (i=0\sim6)$
                 $ACC.7 \leftarrow C$
                 $C \leftarrow [m].0$

Affected flag(s) C

SBC A,[m]   Subtract Data Memory from ACC with Carry

Description   The contents of the specified Data Memory and the complement of the carry flag are
                 subtracted from the Accumulator. The result is stored in the Accumulator. Note that if the
                 result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is
                 positive or zero, the C flag will be set to 1.

Operation $ACC \leftarrow ACC - [m] - \overline{C}$

Affected flag(s) OV, Z, AC, C, SC, CZ

SBC A, x   Subtract immediate data from ACC with Carry

Description   The immediate data and the complement of the carry flag are subtracted from the
                 Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is
                 negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag
                 will be set to 1.

Operation $ACC \leftarrow ACC - [m] - \overline{C}$

Affected flag(s) OV, Z, AC, C, SC, CZ

SBCM A,[m]   Subtract Data Memory from ACC with Carry and result in Data Memory

Description   The contents of the specified Data Memory and the complement of the carry flag are
                 subtracted from the Accumulator. The result is stored in the Data Memory. Note that if the
                 result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is
                 positive or zero, the C flag will be set to 1.

Operation $[m] \leftarrow ACC - [m] - \overline{C}$

Affected flag(s) OV, Z, AC, C, SC, CZ

SDZ [m]   Skip if decrement Data Memory is 0

Description   The contents of the specified Data Memory are first decremented by 1. If the result is 0 the
                 following instruction is skipped. As this requires the insertion of a dummy instruction while
                 the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program
                 proceeds with the following instruction.

Operation $[m] \leftarrow [m] - 1$
                 Skip if [m]=0

Affected flag(s) None

SDZA [m]   Skip if decrement Data Memory is zero with result in ACC

Description   The contents of the specified Data Memory are first decremented by 1. If the result is 0, the
                 following instruction is skipped. The result is stored in the Accumulator but the specified
                 Data Memory contents remain unchanged. As this requires the insertion of a dummy
                 instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0,
                 the program proceeds with the following instruction.

Operation $ACC \leftarrow [m] - 1$
                 Skip if ACC=0

Affected flag(s) None

SET [m]	Set Data Memory
Description	Each bit of the specified Data Memory is set to 1.
Operation	[m] ← FFH
Affected flag(s)	None

SET [m].i	Set bit of Data Memory
Description	Bit i of the specified Data Memory is set to 1.
Operation	[m].i ← 1
Affected flag(s)	None

SIZ [m]	Skip if increment Data Memory is 0
Description	The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	[m] ← [m] + 1 Skip if [m]=0
Affected flag(s)	None

SIZA [m]	Skip if increment Data Memory is zero with result in ACC
Description	The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	ACC ← [m] + 1 Skip if ACC=0
Affected flag(s)	None

SNZ [m].i	Skip if bit i of Data Memory is not 0
Description	If bit i of the specified Data Memory is not 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is 0 the program proceeds with the following instruction.
Operation	Skip if [m].i ≠ 0
Affected flag(s)	None

SNZ [m]	Skip if Data Memory is not 0
Description	The contents of the specified Data Memory are read out and then written back to the specified Data Memory again. If the specified Data Memory is not 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is 0 the program proceeds with the following instruction.
Operation	Skip if [m]≠ 0
Affected flag(s)	None

SUB A,[m]	Subtract Data Memory from ACC
Description	The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	ACC ← ACC − [m]
Affected flag(s)	OV, Z, AC, C, SC, CZ

SUBM A,[m]	Subtract Data Memory from ACC with result in Data Memory
Description	The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	$[m] \leftarrow ACC - [m]$
Affected flag(s)	OV, Z, AC, C, SC, CZ

SUB A,x	Subtract immediate data from ACC
Description	The immediate data specified by the code is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	$ACC \leftarrow ACC - x$
Affected flag(s)	OV, Z, AC, C, SC, CZ

SWAP [m]	Swap nibbles of Data Memory
Description	The low-order and high-order nibbles of the specified Data Memory are interchanged.
Operation	$[m].3\sim[m].0 \leftrightarrow [m].7\sim[m].4$
Affected flag(s)	None

SWAPA [m]	Swap nibbles of Data Memory with result in ACC
Description	The low-order and high-order nibbles of the specified Data Memory are interchanged. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	$ACC.3\sim ACC.0 \leftarrow [m].7\sim[m].4$ $ACC.7\sim ACC.4 \leftarrow [m].3\sim[m].0$
Affected flag(s)	None

SZ [m]	Skip if Data Memory is 0
Description	The contents of the specified Data Memory are read out and then written back to the specified Data Memory again. If the contents of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	Skip if [m]=0
Affected flag(s)	None

SZA [m]	Skip if Data Memory is 0 with data movement to ACC
Description	The contents of the specified Data Memory are copied to the Accumulator. If the value is zero, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	$ACC \leftarrow [m]$ Skip if [m]=0
Affected flag(s)	None

SZ [m].i	Skip if bit i of Data Memory is 0
Description	If bit i of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction.
Operation	Skip if [m].i=0
Affected flag(s)	None

TABRD [m]	Read table (specific page) to TBLH and Data Memory
Description	The low byte of the program code (specific page) addressed by the table pointer (TBLP and TBHP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None

TABRDL [m]	Read table (last page) to TBLH and Data Memory
Description	The low byte of the program code (last page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None

ITABRD [m]	Increment table pointer low byte first and read table (specific page) to TBLH and Data Memory
Description	Increment table pointer low byte, TBLP, first and then the program code (specific page) addressed by the table pointer (TBHP and TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None

ITABRDL [m]	Increment table pointer low byte first and read table (last page) to TBLH and Data Memory
Description	Increment table pointer low byte, TBLP, first and then the low byte of the program code (last page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None

XOR A,[m]	Logical XOR Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical XOR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″XOR″ [m]
Affected flag(s)	Z

XORM A,[m]	Logical XOR ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical XOR operation. The result is stored in the Data Memory.
Operation	[m] ← ACC ″XOR″ [m]
Affected flag(s)	Z

XOR A,x	Logical XOR immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bitwise logical XOR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″XOR″ x
Affected flag(s)	Z

Extended Instruction Definition

The extended instructions are used to directly access the data stored in any data memory sections.

LADC A,[m]	Add Data Memory to ACC with Carry
Description	The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC + [m] + C$
Affected flag(s)	OV, Z, AC, C, SC

LADCM A,[m]	Add ACC to Data Memory with Carry
Description	The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the specified Data Memory.
Operation	$[m] \leftarrow ACC + [m] + C$
Affected flag(s)	OV, Z, AC, C, SC

LADD A,[m]	Add Data Memory to ACC
Description	The contents of the specified Data Memory and the Accumulator are added. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC + [m]$
Affected flag(s)	OV, Z, AC, C, SC

LADDM A,[m]	Add ACC to Data Memory
Description	The contents of the specified Data Memory and the Accumulator are added. The result is stored in the specified Data Memory.
Operation	$[m] \leftarrow ACC + [m]$
Affected flag(s)	OV, Z, AC, C, SC

LAND A,[m]	Logical AND Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical AND operation. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC \ ''AND'' \ [m]$
Affected flag(s)	Z

LANDM A,[m]	Logical AND ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical AND operation. The result is stored in the Data Memory.
Operation	$[m] \leftarrow ACC \ ''AND'' \ [m]$
Affected flag(s)	Z

LCLR [m]	Clear Data Memory
Description	Each bit of the specified Data Memory is cleared to 0.
Operation	$[m] \leftarrow 00H$
Affected flag(s)	None

LCLR [m].i	Clear bit of Data Memory
Description	Bit i of the specified Data Memory is cleared to 0.
Operation	$[m].i \leftarrow 0$
Affected flag(s)	None

LCPL [m]   Complement Data Memory

Description	Each bit of the specified Data Memory is logically complemented (1′s complement). Bits which previously contained a 1 are changed to 0 and vice versa.
Operation	$[m] \leftarrow \overline{[m]}$
Affected flag(s)	Z

LCPLA [m]   Complement Data Memory with result in ACC

Description	Each bit of the specified Data Memory is logically complemented (1′s complement). Bits which previously contained a 1 are changed to 0 and vice versa. The complemented result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	$ACC \leftarrow \overline{[m]}$
Affected flag(s)	Z

LDAA [m]   Decimal-Adjust ACC for addition with result in Data Memory

Description	Convert the contents of the Accumulator value to a BCD (Binary Coded Decimal) value resulting from the previous addition of two BCD variables. If the low nibble is greater than 9 or if AC flag is set, then a value of 6 will be added to the low nibble. Otherwise the low nibble remains unchanged. If the high nibble is greater than 9 or if the C flag is set, then a value of 6 will be added to the high nibble. Essentially, the decimal conversion is performed by adding 00H, 06H, 60H or 66H depending on the Accumulator and flag conditions. Only the C flag may be affected by this instruction which indicates that if the original BCD sum is greater than 100, it allows multiple precision decimal addition.
Operation	$[m] \leftarrow ACC + 00H$ or $[m] \leftarrow ACC + 06H$ or $[m] \leftarrow ACC + 60H$ or $[m] \leftarrow ACC + 66H$
Affected flag(s)	C

LDEC [m]   Decrement Data Memory

Description	Data in the specified Data Memory is decremented by 1.
Operation	$[m] \leftarrow [m] - 1$
Affected flag(s)	Z

LDECA [m]   Decrement Data Memory with result in ACC

Description	Data in the specified Data Memory is decremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	$ACC \leftarrow [m] - 1$
Affected flag(s)	Z

LINC [m]   Increment Data Memory

Description	Data in the specified Data Memory is incremented by 1.
Operation	$[m] \leftarrow [m] + 1$
Affected flag(s)	Z

LINCA [m]   Increment Data Memory with result in ACC

Description	Data in the specified Data Memory is incremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	$ACC \leftarrow [m] + 1$
Affected flag(s)	Z

LMOV A,[m]   Move Data Memory to ACC

Description   The contents of the specified Data Memory are copied to the Accumulator.

Operation   ACC ← [m]

Affected flag(s)   None

LMOV [m],A   Move ACC to Data Memory

Description   The contents of the Accumulator are copied to the specified Data Memory.

Operation   [m] ← ACC

Affected flag(s)   None

LOR A,[m]   Logical OR Data Memory to ACC

Description   Data in the Accumulator and the specified Data Memory perform a bitwise logical OR operation. The result is stored in the Accumulator.

Operation   ACC ← ACC ″OR″ [m]

Affected flag(s)   Z

LORM A,[m]   Logical OR ACC to Data Memory

Description   Data in the specified Data Memory and the Accumulator perform a bitwise logical OR operation. The result is stored in the Data Memory.

Operation   [m] ← ACC ″OR″ [m]

Affected flag(s)   Z

LRL [m]   Rotate Data Memory left

Description   The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0.

Operation   [m].(i+1) ← [m].i; (i=0~6)
          [m].0 ← [m].7

Affected flag(s)   None

LRLA [m]   Rotate Data Memory left with result in ACC

Description   The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation   ACC.(i+1) ← [m].i; (i=0~6)
          ACC.0 ← [m].7

Affected flag(s)   None

LRLC [m]   Rotate Data Memory left through Carry

Description   The contents of the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into bit 0.

Operation   [m].(i+1) ← [m].i; (i=0~6)
          [m].0 ← C
          C ← [m].7

Affected flag(s)   C

LRLCA [m]   Rotate Data Memory left through Carry with result in ACC

Description   Data in the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into the bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation   ACC.(i+1) ← [m].i; (i=0~6)
          ACC.0 ← C
          C ← [m].7

Affected flag(s)   C

LRR [m]   Rotate Data Memory right

Description   The contents of the specified Data Memory are rotated right by 1 bit with bit 0 rotated into bit 7.

Operation   [m].i ← [m].(i+1); (i=0~6)
                            [m].7 ← [m].0

Affected flag(s)   None

LRRA [m]   Rotate Data Memory right with result in ACC

Description   Data in the specified Data Memory is rotated right by 1 bit with bit 0
                            rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the
                            Data Memory remain unchanged.

Operation   ACC.i ← [m].(i+1); (i=0~6)
                            ACC.7 ← [m].0

Affected flag(s)   None

LRRC [m]   Rotate Data Memory right through Carry

Description   The contents of the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0
                            replaces the Carry bit and the original carry flag is rotated into bit 7.

Operation   [m].i ← [m].(i+1); (i=0~6)
                            [m].7 ← C
                            C ← [m].0

Affected flag(s)   C

LRRCA [m]   Rotate Data Memory right through Carry with result in ACC

Description   Data in the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces
                            the Carry bit and the original carry flag is rotated into bit 7. The rotated result is stored in the
                            Accumulator and the contents of the Data Memory remain unchanged.

Operation   ACC.i ← [m].(i+1); (i=0~6)
                            ACC.7 ← C
                            C ← [m].0

Affected flag(s)   C

LSBC A,[m]   Subtract Data Memory from ACC with Carry

Description   The contents of the specified Data Memory and the complement of the carry flag are
                            subtracted from the Accumulator. The result is stored in the Accumulator. Note that if the
                            result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is
                            positive or zero, the C flag will be set to 1.

Operation $ACC \leftarrow ACC - [m] - \overline{C}$

Affected flag(s)   OV, Z, AC, C, SC, CZ

LSBCM A,[m]   Subtract Data Memory from ACC with Carry and result in Data Memory

Description   The contents of the specified Data Memory and the complement of the carry flag are
                            subtracted from the Accumulator. The result is stored in the Data Memory. Note that if the
                            result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is
                            positive or zero, the C flag will be set to 1.

Operation $[m] \leftarrow ACC - [m] - \overline{C}$

Affected flag(s)   OV, Z, AC, C, SC, CZ

LSDZ [m]	Skip if decrement Data Memory is 0
Description	The contents of the specified Data Memory are first decremented by 1. If the result is 0 the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a three cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	$[m] \leftarrow [m] - 1$ Skip if [m]=0
Affected flag(s)	None

LSDZA [m]	Skip if decrement Data Memory is zero with result in ACC
Description	The contents of the specified Data Memory are first decremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a three cycle instruction. If the result is not 0, the program proceeds with the following instruction.
Operation	$ACC \leftarrow [m] - 1$ Skip if ACC=0
Affected flag(s)	None

LSET [m]	Set Data Memory
Description	Each bit of the specified Data Memory is set to 1.
Operation	$[m] \leftarrow FFH$
Affected flag(s)	None

LSET [m].i	Set bit of Data Memory
Description	Bit i of the specified Data Memory is set to 1.
Operation	$[m].i \leftarrow 1$
Affected flag(s)	None

LSIZ [m]	Skip if increment Data Memory is 0
Description	The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a three cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	$[m] \leftarrow [m] + 1$ Skip if [m]=0
Affected flag(s)	None

LSIZA [m]	Skip if increment Data Memory is zero with result in ACC
Description	The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a three cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	$ACC \leftarrow [m] + 1$ Skip if ACC=0
Affected flag(s)	None

LSNZ [m].i	Skip if bit i of Data Memory is not 0
Description	If bit i of the specified Data Memory is not 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a three cycle instruction. If the result is 0 the program proceeds with the following instruction.
Operation	Skip if $[m].i \neq 0$
Affected flag(s)	None

LSNZ [m] Skip if Data Memory is not 0

Description	The contents of the specified Data Memory are read out and then written to the specified Data Memory again. If the content of the specified Data Memory is not 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a three cycle instruction. If the result is 0 the program proceeds with the following instruction.
Operation	Skip if $[m] \neq 0$
Affected flag(s)	None

LSUB A,[m] Subtract Data Memory from ACC

Description	The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	$ACC \leftarrow ACC - [m]$
Affected flag(s)	OV, Z, AC, C, SC, CZ

LSUBM A,[m] Subtract Data Memory from ACC with result in Data Memory

Description	The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	$[m] \leftarrow ACC - [m]$
Affected flag(s)	OV, Z, AC, C, SC, CZ

LSWAP [m] Swap nibbles of Data Memory

Description	The low-order and high-order nibbles of the specified Data Memory are interchanged.
Operation	$[m].3 \sim [m].0 \leftrightarrow [m].7 \sim [m].4$
Affected flag(s)	None

LSWAPA [m] Swap nibbles of Data Memory with result in ACC

Description	The low-order and high-order nibbles of the specified Data Memory are interchanged. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	$ACC.3 \sim ACC.0 \leftarrow [m].7 \sim [m].4$ $ACC.7 \sim ACC.4 \leftarrow [m].3 \sim [m].0$
Affected flag(s)	None

LSZ [m] Skip if Data Memory is 0

Description	The contents of the specified Data Memory are read out and then written to the specified Data Memory again. If the contents of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a three cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	Skip if $[m]=0$
Affected flag(s)	None

LSZA [m] Skip if Data Memory is 0 with data movement to ACC

Description	The contents of the specified Data Memory are copied to the Accumulator. If the value is zero, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a three cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	$ACC \leftarrow [m]$ Skip if $[m]=0$
Affected flag(s)	None

LSZ [m].i	Skip if bit i of Data Memory is 0
Description	If bit i of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a three cycle instruction. If the result is not 0, the program proceeds with the following instruction.
Operation	Skip if [m].i=0
Affected flag(s)	None

LTABRD [m]	Read table (specific page) to TBLH and Data Memory
Description	The low byte of the program code (specific page) addressed by the table pointer (TBHP and TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None

LTABRDL [m]	Read table (last page) to TBLH and Data Memory
Description	The low byte of the program code (last page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None

LITABRD [m]	Increment table pointer low byte first and read table (specific page) to TBLH and Data Memory
Description	Increment table pointer low byte, TBLP, first and then the program code (specific page) addressed by the table pointer (TBHP and TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None

LITABRDL [m]	Increment table pointer low byte first and read table (last page) to TBLH and Data Memory
Description	Increment table pointer low byte, TBLP, first and then the low byte of the program code (last page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None

LXOR A,[m]	Logical XOR Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical XOR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″XOR″ [m]
Affected flag(s)	Z

| **LXORM A,[m]**	Logical XOR ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical XOR operation. The result is stored in the Data Memory.
Operation	[m] ← ACC ″XOR″ [m]
Affected flag(s)	Z

Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

• Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)

• Packing Meterials Information

• Carton information

64-pin LQFP (7mm×7mm) Outline Dimensions
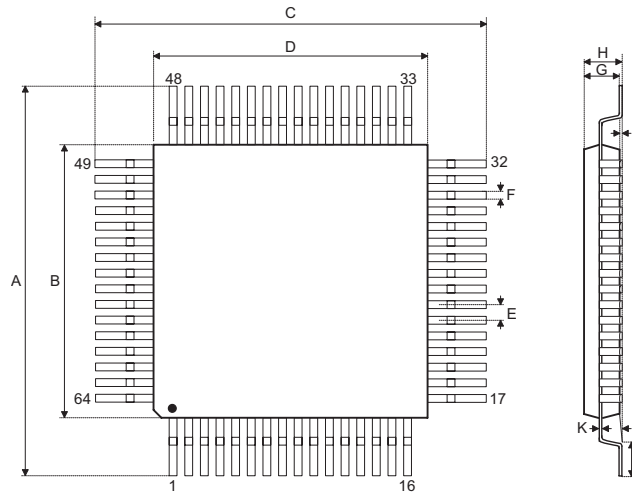
Symbol	Dimensions in inch		
	Min.	**Nom.**	**Max.**
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.016 BSC	—
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	**Nom.**	**Max.**
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.40 BSC	—
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

80-pin LQFP (10mm×10mm) Outline Dimensions
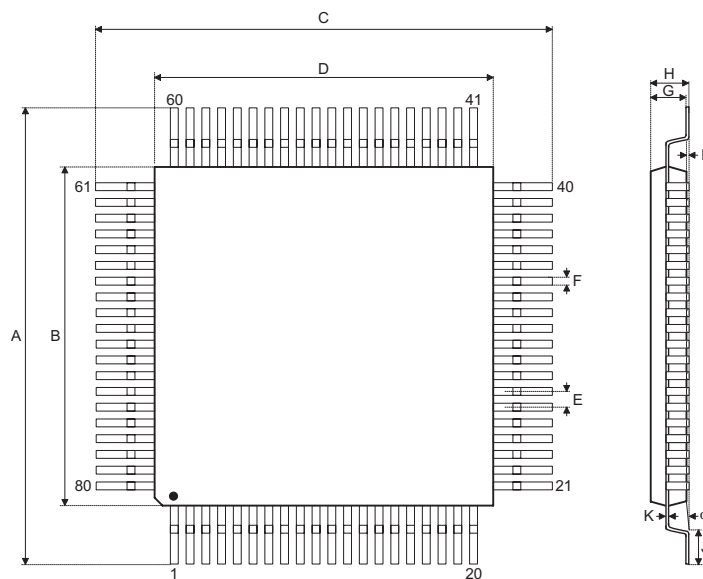
Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.472 BSC	—
B	—	0.394 BSC	—
C	—	0.472 BSC	—
D	—	0.394 BSC	—
E	—	0.016 BSC	—
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	12.00 BSC	—
B	—	10.00 BSC	—
C	—	12.00 BSC	—
D	—	10.00 BSC	—
E	—	0.40 BSC	—
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°