Features

- V_{IN} Input Range from 7.5V to 36V
- Accumulative Cell Voltage Monitor
  - 8-to-1 Analog Multiplexer with divided ratio accuracy: 1/n ± 0.5%
- Cell Charging Balance Switches
- 5V/50mA internal Voltage Regulator with ±1% accuracy
- Two Discharge N-type MOSFET Gate Drivers
- Single Charge N-type MOSFET Gate Driver
- Sleep Mode with 0.1μA ultra-low standby current
- Direct High Voltage Wake-up function
- I^2C Bus Communication with Host MCU
- Operating Temperature Range: -40°C to +85°C
- Package Types: 24-pin SSOP-EP/QFN

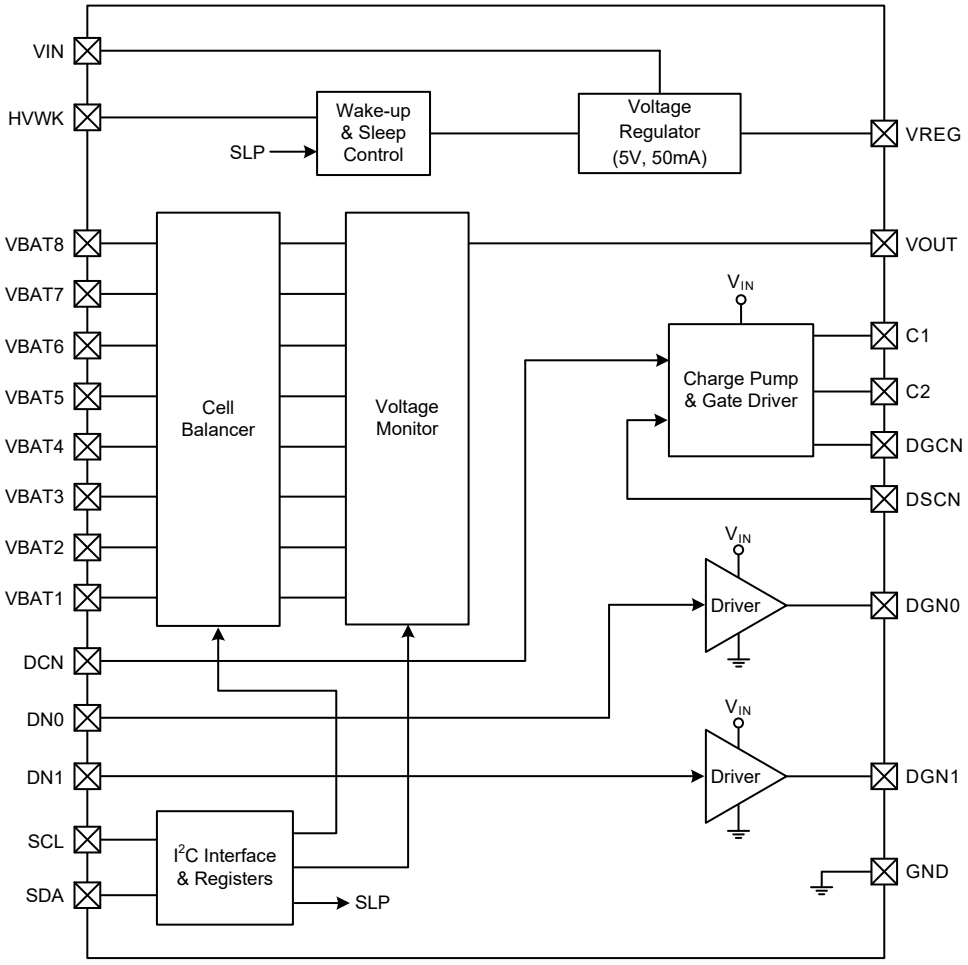
Applications

- Handheld vacuum cleaners
- Electric power tools

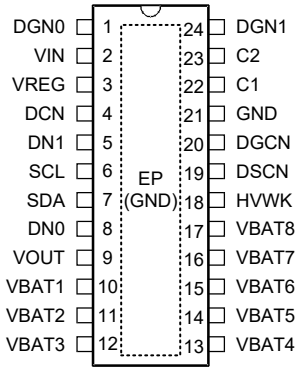
General Description

The HT7Q1531 is a high voltage analog-front-end IC for 3 to 8 cell Li-ion rechargeable battery protection. It consists of an accumulative cell voltage monitor, a high accuracy voltage regulator, two discharge N-type MOSFET gate drivers and a charge N-type MOSFET gate driver. The device is designed to monitor an accumulative voltage from 1 to N and outputs the divide-by-N voltage to the analog multiplexer with a ±0.5% divided ratio accuracy. The device can directly drive external power N-type MOSFETs to control charge and discharge by charge and discharge gate drivers. The integrated battery balance circuitry provides a cell balance current without the need of external transistors. The anti-reverse current switch is implemented to prevent a backflow current even if V_{OUT} is higher than V_{BATn}. Each divided accumulative cell voltage can be observed sequentially from VBAT1 to VBAT8 which benefits MCUs with a lower number of ADCs. An integrated regulator provides a 5V supply to the MCU with a 50mA driving current capability and which has ±1% accuracy. The voltage regulator, cell voltage monitor and gate drivers are shut down with an ultra-low standby current of 0.1μA when the device is in the Sleep mode. When the HVWK pin is triggered by a voltage greater than its threshold, the device will return to the standby state.

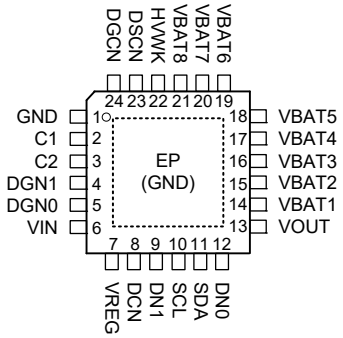
Functional Block Diagram



Pin Assignment



HT7Q1531
24 SSOP-EP-A



HT7Q1531
24 QFN-A

Pin Description

Pin No.		Name	Type	Pin Description
24SSOP-EP	24QFN			
1	5	DGN0	O	Gate driver output 0 for driving discharge N-type MOSFET. Recommended for applying on primary loading path
2	6	VIN	P	Input supply voltage. Connect to the top VBATn
3	7	VREG	O	Regulator 5V/50mA output. Connect a 4.7μF capacitor typically
4	8	DCN	I	Gate driver DGCN control input *
5	9	DN1	I	Gate driver DGN1 control input *
6	10	SCL	I/O	I^2C serial clock line
7	11	SDA	I/O	I^2C serial data line
8	12	DN0	I	Gate driver DGN0 control input *
9	13	VOUT	O	Voltage monitor output
10	14	VBAT1	I	Battery cell 1 positive terminal and battery cell 2 negative terminal
11	15	VBAT2	I	Battery cell 2 positive terminal and battery cell 3 negative terminal
12	16	VBAT3	I	Battery cell 3 positive terminal and battery cell 4 negative terminal
13	17	VBAT4	I	Battery cell 4 positive terminal and battery cell 5 negative terminal
14	18	VBAT5	I	Battery cell 5 positive terminal and battery cell 6 negative terminal
15	19	VBAT6	I	Battery cell 6 positive terminal and battery cell 7 negative terminal
16	20	VBAT7	I	Battery cell 7 positive terminal and battery cell 8 negative terminal
17	21	VBAT8	I	Battery cell 8 positive terminal
18	22	HVWK	I	High voltage wake-up function sense and trigger pin
19	23	DSCN	I	Charge pump reference voltage input. Connect to charge N-type MOSFET source pin
20	24	DGCN	O	Gate driver output for driving charge N-type MOSFET with 12V clamped from DGCN to DSCN
21	1	GND	G	Ground terminal
22	2	C1	O	Charge pump capacitor for DGCN. Connect an capacitor between C1 and C2
23	3	C2	O	Charge pump capacitor for DGCN. Connect an capacitor between C1 and C2
24	4	DGN1	O	Gate driver output 1 for driving discharge N-type MOSFET. Recommended for applying on secondary loading path
EP	EP	GND	G	Connect to GND

Note: I: Input; O: Output; P: Power; G: Ground;

*: Internal pull down with 430kΩ.

Absolute Maximum Ratings

Pin / Parameter		Value	Unit
VIN, DSCN, HVWK, C2		-0.3 to +48	V
DGCN, C1		-0.3 to +60	V
VREG, VOUT		-0.3 to +5.5	V
DGN0, DGN1		-0.3 to 18	V
SCL, SDA, DN0, DN1, DCN		-0.3 to +5.5	V
$\Delta[V_{BATi}\sim V_{BAT(i-1)}]$, i=2~8		-0.3 to +5.5	V
Operating Temperature Range		-40 to +85	°C
Maximum Junction Temperature		+125	°C
Storage Temperature Range		-60 to +150	°C
Lead Temperature (Soldering 10sec)		+260	°C
ESD Susceptibility	Human Body Model	±2000	V
	Machine Model	±200	V
Junction-to-Ambient Thermal Resistance, θ_{JA}	24SSOP-EP/QFN	40	°C/W

Note: Absolute Maximum Ratings indicate limitations beyond which damage to the device may occur.

Recommended Operating Ratings

Pin / Parameter	Value	Unit
VIN	7.5 to 36.0	V
Ta	-40 to +85	°C

Note: Recommended Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specified performance limits.

Electrical Characteristics

V_{IN}=36V, C_{VREG}=4.7μF, C_{VOUT}=2.2nF, Ta=25°C, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply and Input						
V_{IN}	Supply Voltage	—	7.5	—	36.0	V
$I_{IN(VM\_ACT)}$	Supply Current When Voltage Monitor is Activated	EN_S=1	6	11	16	μA
$I_{IN(STB)}$	Supply Current – Standby	B2=B1=B0=EN_S=0, V_{DN0}=V_{DN1}=V_{DCN}=0V	—	3.5	6.0	μA
$I_{IN(STB\_DSG)}$	VIN Supply Current When DGN0 is Activated	B2=B1=B0=EN_S=0, V_{DN0}=5V, V_{DN1}=V_{DCN}=0V	—	35	42	μA
I_{SLP}	Standby Current in SLEEP Mode	V_{SLP}=5V, V_{HVWK}=0V	—	0.1	0.2	μA
Voltage Regulator						
V_{REG}	Regulator Output Voltage	I_{LOAD}=10mA	4.95	5.00	5.05	V
I_{REG}	Regulator Maximum Output Current	V_{IN}=7.5V, Ta=-40°C~85°C	50	—	—	mA
ΔV_{REG}	Load Regulation	I_{LOAD}=0mA~50mA	—	30	80	mV
$\Delta V_{REG}/(V_{REG}\times\Delta V_{IN})$	Line Regulation	V_{IN}=7.5V~36V, I_{LOAD}=10mA	—	0.02	—	%/V
$\Delta V_{REG}/(V_{REG}\times\Delta Ta)$	Temperature Coefficient	I_{LOAD}=1mA, Ta=-40°C~85°C	—	±100	—	ppm/°C
R_{DIS}	VREG Discharge Resistance	SLP=1, V_{REG}=1V, I_{REG1} denotes VREG input current at V_{REG}=1V, R_{DIS}=V_{REG}/I_{REG1}	—	85	—	Ω

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Cell Balancer						
R_{CB}	Charge Balance Resistance	V_{Bi}=4.5V (i=1~8), VBATn series resistors=0Ω	55	85	115	Ω
		V_{Bi}=2.5V (i=1~8), VBATn series resistors=0Ω	80	120	160	Ω
Input/Output Logic						
V_{IL}	DN0, DN1, DCN Input Logic Low Voltage	—	—	—	0.8	V
V_{IH}	DN0, DN1, DCN Input Logic High Voltage	—	2.5	—	—	V
R_{PD}	DN0, DN1, DCN Pull-Down Resistance	—	—	430	—	kΩ
High Voltage Wake-Up						
V_{WKTH}	HVWK Trigger Threshold Voltage	—	4.5	5.5	6.5	V
t_{WKDB1}	HVWK Trigger Debounce Time	—	1	—	—	ms
I_{WK}	HVWK Input Current	V_{HVWK}=36V	—	50	—	μA
Accumulative Cell Voltage Monitor						
V_{Bi}	Cell Voltage	i=1~8	2.5	—	4.5	V
$V_{B(MIN)}$	Input Voltage between VBATi and VBAT(i-1) for Charge Balance and Voltage Monitor	—	1.5	—	—	V
$I_{Bi(PWR)}$	Cell Input Leakage Current When V_{IN} is Powered	V_{BATi}=5V×i, EN_S=0, V_{IN}=V_{BAT8}, i=1~8	-0.1	—	0.1	μA
$I_{Bi(ACT)}$	Cell Input Current When Voltage Monitoring	V_{Bi}=4.5V, EN_S=1, V_{IN}=36V, i=1~8	19	24	35	μA
R	Divided Resistance	—	140	200	260	kΩ
$Ratio8_{(NORM)}$	VBAT8 Accumulative Cell Voltage Divided Ratio (Normalized)	V_{BAT8}=20V~36V, B2~B0=0b111	0.995	1	1.005	V/V
		V_{BAT8}=20V~36V, B2~B0=0b111, Ta=-40°C~85°C	0.99	1	1.01	V/V
$Ratio7_{(NORM)}$	VBAT7 Accumulative Cell Voltage Divided Ratio (Normalized)	V_{BAT7}=17.5V~31.5V, B2~B0=0b110	0.995	1	1.005	V/V
		V_{BAT7}=17.5V~31.5V, B2~B0=0b110, Ta=-40°C~85°C	0.99	1	1.01	V/V
$Ratio6_{(NORM)}$	VBAT6 Accumulative Cell Voltage Divided Ratio (Normalized)	V_{BAT6}=15V~27V, B2~B0=0b101	0.995	1	1.005	V/V
		V_{BAT6}=15V~27V, B2~B0=0b101, Ta=-40°C~85°C	0.99	1	1.01	V/V
$Ratio5_{(NORM)}$	VBAT5 Accumulative Cell Voltage Divided Ratio (Normalized)	V_{BAT5}=12.5V~22.5V, B2~B0=0b100	0.995	1	1.005	V/V
		V_{BAT5}=12.5V~22.5V, B2~B0=0b100, Ta=-40°C~85°C	0.99	1	1.01	V/V
$Ratio4_{(NORM)}$	VBAT4 Accumulative Cell Voltage Divided Ratio (Normalized)	V_{BAT4}=10V~18V, B2~B0=0b011	0.995	1	1.005	V/V
		V_{BAT4}=10V~18V, B2~B0=0b011, Ta=-40°C~85°C	0.99	1	1.01	V/V
$Ratio3_{(NORM)}$	VBAT3 Accumulative Cell Voltage Divided Ratio (Normalized)	V_{BAT3}=7.5V~13.5V, B2~B0=0b010	0.995	1	1.005	V/V
		V_{BAT3}=7.5V~13.5V, B2~B0=0b010, Ta=-40°C~85°C	0.99	1	1.01	V/V
$Ratio2_{(NORM)}$	VBAT2 Accumulative Cell Voltage Divided Ratio (Normalized)	V_{BAT2}=5V~9V, B2~B0=0b001	0.995	1	1.005	V/V
		V_{BAT2}=5V~9V, B2~B0=0b001, Ta=-40°C~85°C	0.99	1	1.01	V/V
$Ratio1_{(NORM)}$	VBAT1 Accumulative Cell Voltage Divided Ratio (Normalized)	V_{BAT1}=2.5V~4.5V, B2~B0=0b000	0.995	1	1.005	V/V
		V_{BAT1}=2.5V~4.5V, B2~B0=0b000, Ta=-40°C~85°C	0.99	1	1.01	V/V

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{MAX}	Voltage Monitor Channel to Channel Scan Frequency	C_{VOUT}=2.2nF	—	—	100	Hz
Gate Drivers						
V_Z	DGNx Clamp Voltage	V_{DN0}=V_{DN1}=5V, V_{IN}>13V	10	12	16	V
		V_{DN0}=V_{DN1}=5V, V_{IN}≤13V	—	V_{IN}-0.7	—	V
	V(DGCN,DSCN) Clamp Voltage	V_{DCN}=5V, V_{IN}>15V	10	12	16	V
		V_{DCN}=5V, V_{IN}≤15V	—	V_{IN}-3.2	—	V
t_{r0}	DGN0 Rising Time	C_{DGN0}=15nF	—	0.5	1.0	μs
t_{f0}	DGN0 Falling Time	C_{DGN0}=15nF	—	0.5	1.0	μs
t_{PD_HL0}	DGN0 Falling Propagation Delay Time	C_{DGN0}=15nF	—	0.5	1.0	μs
t_{MM0}	DGN0 Delay Time Mismatch	C_{DGN0}=15nF, t_{MM0}=|t_{PD_LH0}-t_{PD_HL0}|	—	0.5	1.0	μs
$I_{SOURCE0}$	DGN0 Source Current	C_{DGN0}=1μF, peak current at DN0 rising edge (0→1)	—	850	—	mA
I_{SINK0}	DGN0 Sink Current	C_{DGN0}=1μF, peak current at DN0 falling edge (1→0)	—	400	—	mA
f_{PWM0}	DGN0 PWM Frequency	C_{DGN0}=15nF	—	—	10	kHz
t_{r1}	DGN1 Rising Time	C_{DGN1}=15nF	—	1.2	2.5	μs
t_{f1}	DGN1 Falling Time	C_{DGN1}=15nF	—	1.2	2.5	μs
t_{PD_HL1}	DGN1 Falling Propagation Delay Time	C_{DGN1}=15nF	—	1.2	2.5	μs
t_{MM1}	DGN1 Delay Time Mismatch	C_{DGN1}=15nF, t_{MM1}=|t_{PD_LH1}-t_{PD_HL1}|	—	1.2	2.5	μs
$I_{SOURCE1}$	DGN1 Source Current	C_{DGN1}=1μF, peak current at DN1 rising edge (0→1)	—	350	—	mA
I_{SINK1}	DGN1 Sink Current	C_{DGN1}=1μF, peak current at DN1 falling edge (1→0)	—	180	—	mA
f_{PWM1}	DGN1 PWM Frequency	C_{DGN1}=15nF	—	—	2	kHz
f_{CP}	Charge Pump Switching Frequency	External capacitor is 22nF between C1 and C2	—	150	—	kHz
t_{rC}	Rising Time of The Voltage Difference between DGCN and DSCN	$C_{DGCN-DSCN}$=15nF, V_{IN}=36V	—	500	—	μs
t_{fC}	Falling Time of The Voltage Difference between DGCN and DSCN	$C_{DGCN-DSCN}$=15nF, V_{IN}=36V	—	5	10	μs
$R_{PL\_SLP\_G}$	DGCN Pull-Low Resistance in Sleep Mode	SLP=1, resistance between DGCN and GND	—	830	—	Ω
$R_{PL\_SLP\_S}$	DSCN Pull-Low Resistance in Sleep Mode	SLP=1, resistance between DSCN and GND	—	830	—	Ω
$R_{PL\_SLP\_GS}$	DGCN to DSCN Pull-Low Resistance in Sleep Mode	SLP=1, resistance between DGCN and DSCN	—	1.65	—	kΩ
$R_{PL\_STB\_G}$	DGCN Pull-Low Resistance in Standby Mode	SLP=0, V_{DCN}=0V, resistance between DGCN and GND	—	50	—	Ω
$R_{PL\_STB\_S}$	DSCN Pull-Low Resistance in Standby Mode	SLP=0, V_{DCN}=0V, resistance between DSCN and GND	—	50	—	Ω
$R_{PL\_STB\_GS}$	DGCN to DSCN Pull-Low Resistance in Standby Mode	SLP=0, V_{DCN}=0V, resistance between DGCN and DSCN	—	90	—	Ω
$R_{PL\_S\_0}$	DGN0 Pull-Low Resistance in Sleep and Standby Mode	V_{DN0}=0V, SLP=0 or 1, resistance between DGN0 and GND	—	5	—	Ω
$R_{PL\_S\_1}$	DGN1 Pull-Low Resistance in Sleep and Standby Mode	V_{DN1}=0V, SLP=0 or 1, resistance between DGN1 and GND	—	8.5	—	Ω

I²C Interface Characteristics

D.C. Characteristics

V_{IN}=36V, Ta=25°C, unless otherwise specified

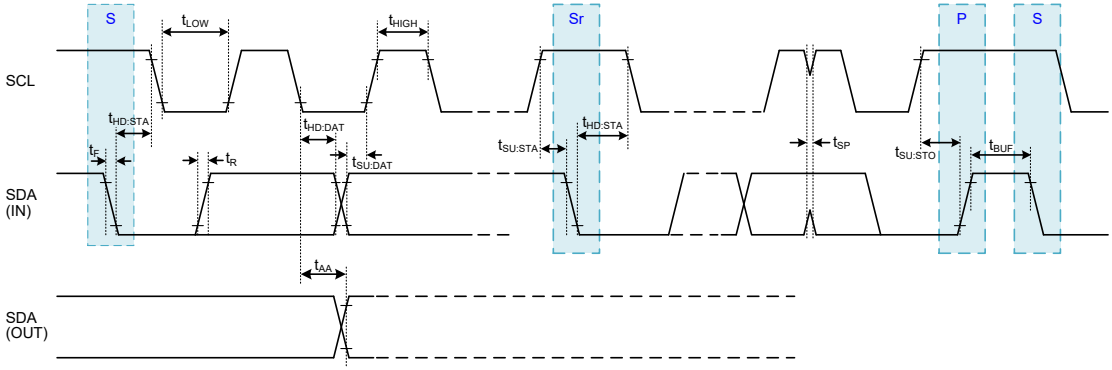
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IH_I2C}	Input High Threshold Voltage	—	2.5	—	—	V
V_{IL_I2C}	Input Low Threshold Voltage	—	—	—	0.8	V

A.C. Characteristics

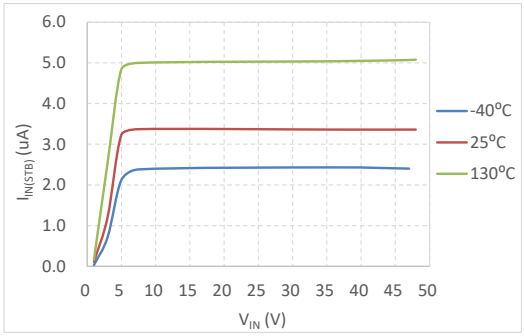
V_{IN}=36V, Ta=25°C, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Clock Frequency	—	—	—	400	kHz
t_{BMF}	Bus Free Time	Bus free time between STOP and START	1.3	—	—	μs
$t_{HD:STA}$	START Hold Time	After this period, the first clock pulse is generated	0.6	—	—	μs
t_{LOW}	SCL Low Time	—	1.3	—	—	μs
t_{HIGH}	SCL High Time	—	0.6	—	—	μs
$t_{SU:STA}$	START Setup Time	Only relevant for Repeated START	0.6	—	—	μs
$t_{HD:DAT}$	Data Hold Time	—	0	—	—	ns
$t_{SU:DAT}$	Data Setup Time	—	100	—	—	ns
t_{R_I2C}	Rising Time	SDA and SCL (Note)	—	—	0.3	μs
t_{F_I2C}	Falling Time	SDA and SCL (Note)	—	—	0.3	μs
$t_{SU:STO}$	STOP Setup Time	—	0.6	—	—	μs
t_{AA}	Output Valid from Clock	—	—	—	0.9	μs
t_{SP}	Input Filter Time Constant	SDA and SCL noise suppression time	—	—	20	ns
t_{OUT}	I²C Time Out	Trimming selection 1 (default setting)	—	32	—	ms
		Trimming selection 2	—	64	—	ms

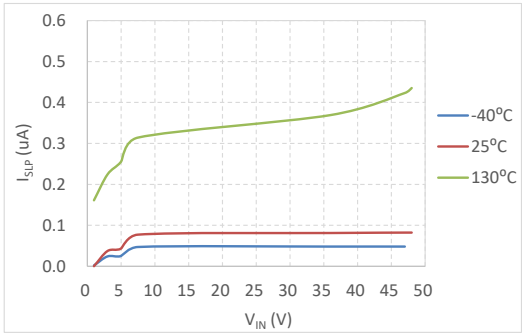
Note: These parameters are periodically sampled but not 100% tested.



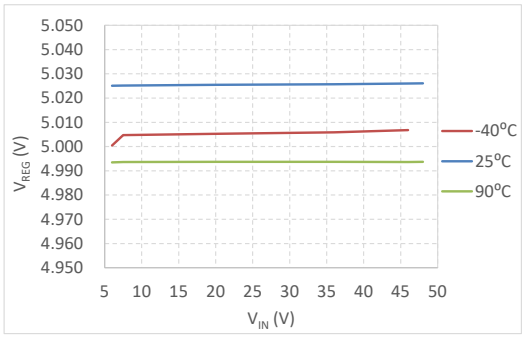
Typical Performance Characteristics



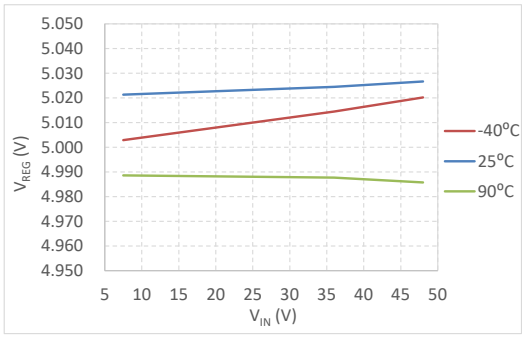
$I_{IN(STB)}$ vs. V_{IN}



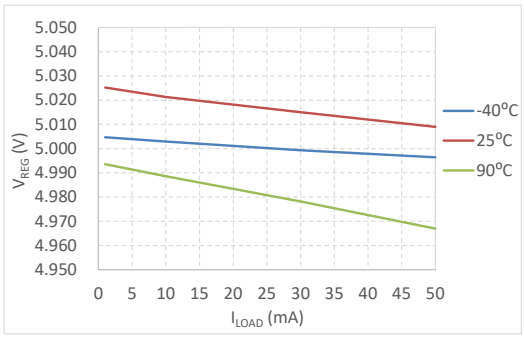
I_{SLP} vs. V_{IN}



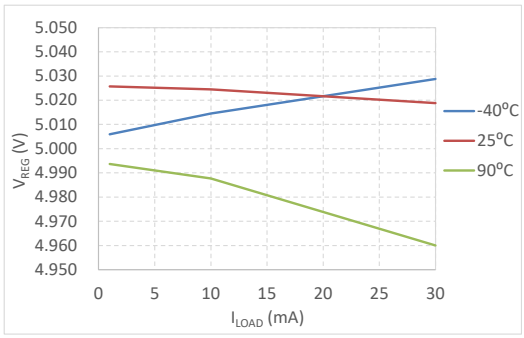
V_{REG} vs. V_{IN}
(VREG output current=1mA)



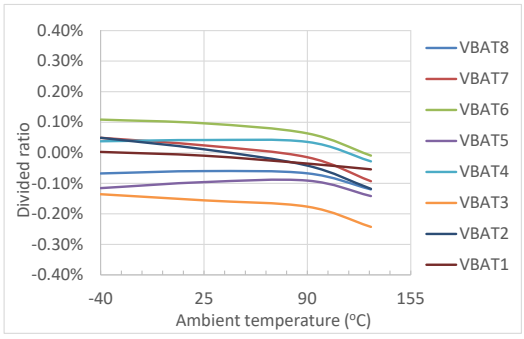
V_{REG} vs. V_{IN}
VREG output current=10mA



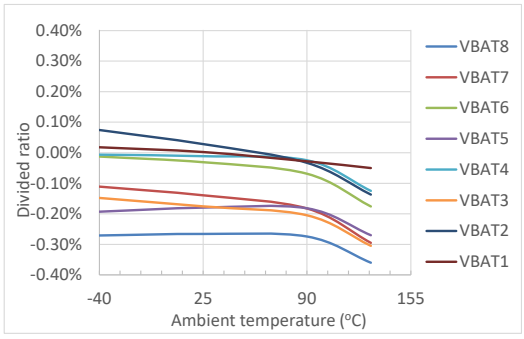
V_{REG} vs. VREG Output Current (V_{IN}=7.5V)



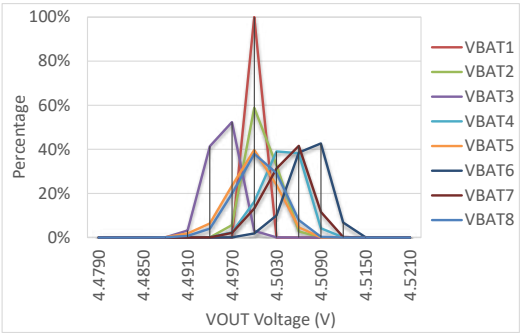
V_{REG} vs. VREG Output Current (V_{IN}=36V)



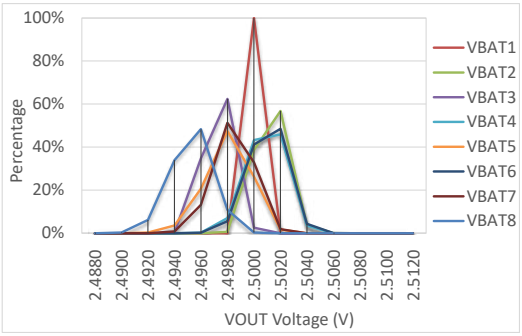
Cell Voltage Divided Ratio vs. Ambient Temperature (V_{Bn}=4.5V)



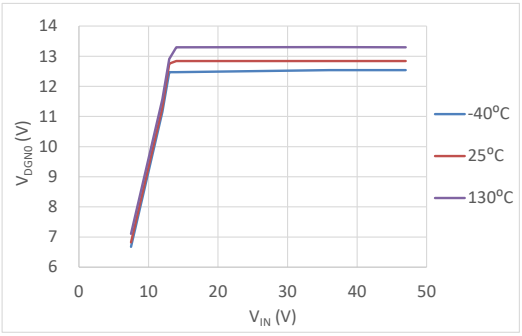
Cell Voltage Divided Ratio vs. Ambient Temperature (V_{Bn}=2.5V)



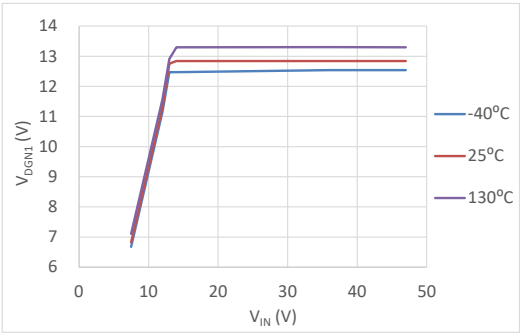
Wafer Level VOUT Voltage Statistics Distribution (V_{Bn}=4.5V)



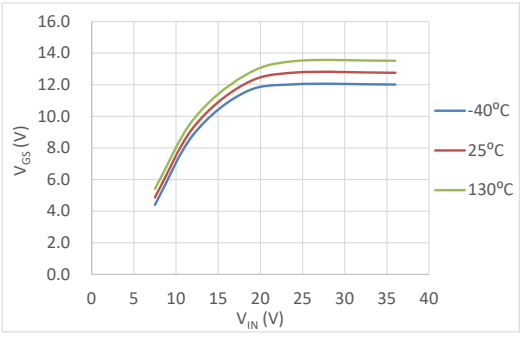
Wafer Level VOUT Voltage Statistics Distribution (V_{Bn}=2.5V)



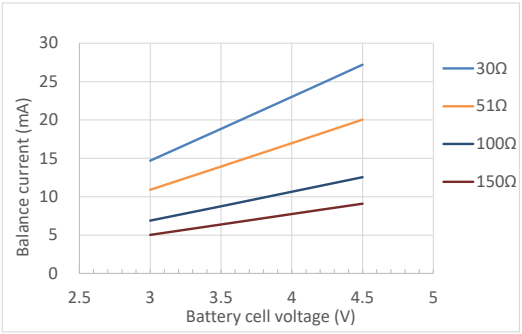
DGN0 Output Voltage vs. V_{IN}



DGN1 Output Voltage vs. V_{IN}



Voltage Difference between DGCN and DSCN vs. V_{IN}



Balance Current vs. VBATn Series Resistance

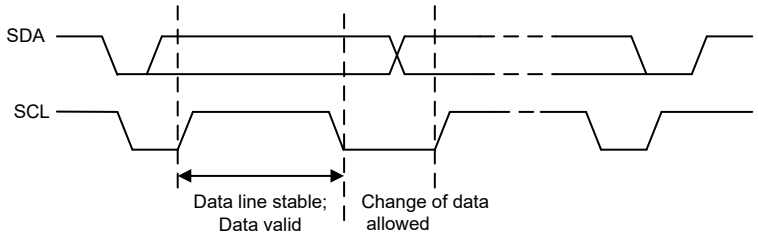
Functional Description

I²C Serial Interface

The device includes an I²C serial interface. The I²C bus is used for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are open-drain structure and two external pull-high resistors are required. When the bus is free, both lines are high. The output stages of devices connected to the bus must have an open-drain or open-collector to implement the Wired-AND function. Data transfer is initiated only when the bus is not busy.

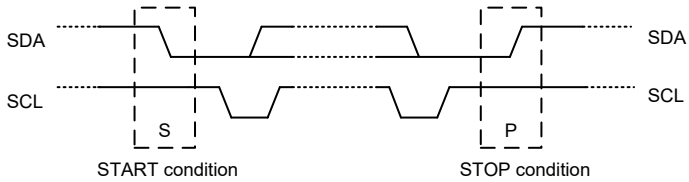
Data Validity

The data on the SDA line must be stable during the clock high period. The high or low state of the data line can only change when the clock signal on the SCL line is low.



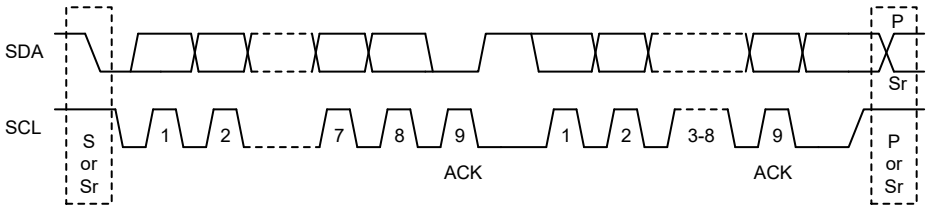
START and STOP Conditions

- A high to low transition on the SDA line while SCL is high defines a START (S).
- A low to high transition on the SDA line while SCL is high defines a STOP (P).
- START and STOP are always generated by the master. The bus is considered to be busy after the START. The bus is considered to be free again a certain time after the STOP.
- The bus remains busy if a Repeated START (Sr) is generated instead of a STOP. In the respect, the START and Repeated START are functionally identical.



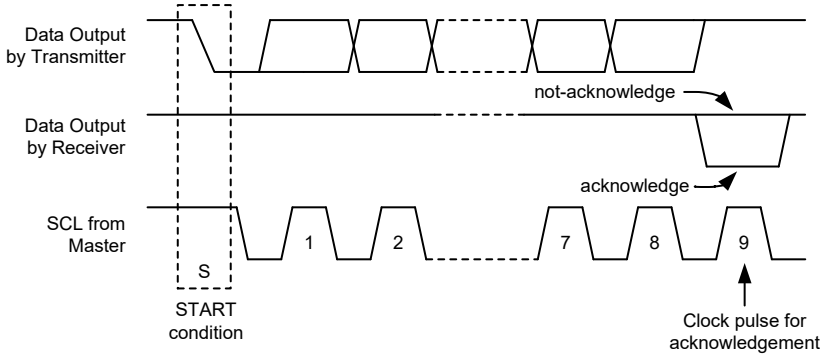
Byte Format

Every byte placed on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.



Acknowledge

- Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level placed on the bus by the receiver, the master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an acknowledge (ACK) after the reception of each byte.
- The device that provides an acknowledge must pull down the SDA line during the acknowledge clock pulse so that it remains at a stable low level during the high period of this clock pulse.
- A master receiver must signal an end of data to the slave by generating a not-acknowledge (NACK) bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse so as to not acknowledge. The master will generate a STOP or a Repeated START.

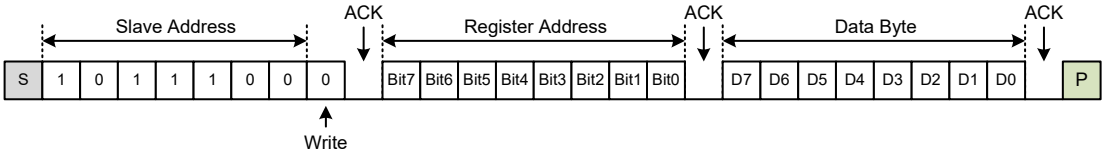


I²C Time-out Control

In order to reduce the I²C lockup problem due to reception of erroneous clock sources, a time-out function is provided. The I²C time-out function starts timing for the specified I²C time-out period (t_{OUT}) when receiving START (S) from I²C bus. The timer is reset by every falling edge of SCL and gets interrupted when receiving STOP (P). If the next falling edge of SCL or STOP (P) does not appear throughout the I²C time-out period (t_{OUT}), the SDA and SCL are set to their default states at the end of timing and meanwhile the registers remains unchanged. The I²C time-out period can be specified to 32ms or 64ms by Trim-fuse selection.

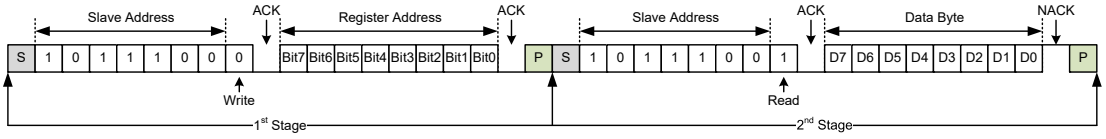
Write Operation

An I²C write operation combines a START bit, a Slave address with a Write bit, a Register command byte, a Data byte and a STOP bit.



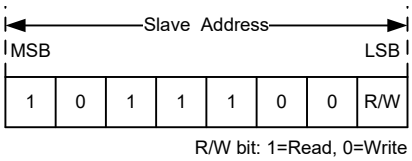
Read Sequence

The complete read mode consists of two stages. For the 1st stage, write the Register Address Byte to the device. For the 2nd stage, reads out the Data Byte from the device. The following diagram shows the complete read format.



Slave Address

- The slave address byte is the first byte received following the START condition from the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines whether a read or write operation is to be performed. When the R/W bit is "1", then a read operation is selected. When the R/W bit is "0", it selects a write operation.
- The slave address of the device is "1011100". When an address byte is sent, the device compares the first seven bits after the START condition. If matched, the device outputs an Acknowledge on the SDA line.



I²C Register Map

The I²C register map is listed below.

Address	Acronym	Access Type	Value after POR	Register Description
00H	REG00	R/W	0000 0000	Sleep and Voltage monitor
01H	REG01	R/W	0000 0000	Charge balance

- **Sleep and Voltage Monitor Register**

Bit	7	6	5	4	3	2	1	0
Name	SLP	EXT_WK	EN_S	Reserved	Reserved	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **SLP**: Sleep mode enable control

0: Stay in normal operation

1: Start Sleep procedure

At the state of EXT_WK="1", SLP is reset to "0" and keep the "0" state until EXT_WK is cleared to "0". The Sleep command from I²C master is ignored during the state of EXT_WK="1".

Bit 6 **EXT_WK**: External wake-up event status

0: Denotes that external wake-up event does not exist

1: Denotes that external wake-up event exists or is written by MCU

(1) When the voltage applied on HVWK pin remains higher than V_{WKTH} over 10μs, the EXT_WK will be set to "1" and the SLP will be reset to "0". The EXT_WK is cleared to "0" immediately when the voltage applied on HVWK pin is less than 1.5V.

(2) The EXT_WK can be written as "1" by MCU for the purpose of sending a wake-up signal. The EXT_WK and SLP have to be written as "0" through the I²C interface after the EXT_WK is set to "1" by MCU, otherwise the external wake-up event on HVWK pin cannot be recognized and the follow-up Sleep command will be failed.

(3) Writing both EXT_WK and SLP as "1" is not permitted for avoiding unpredictable status.

(4) Reading EXT_WK reveals the external wake-up even status of the HVWK pin only.

Bit 5 **EN_S**: Voltage monitor function enable control

0: Voltage monitor function is disabled, V_{OUT}=0V

1: Voltage monitor function is enabled, $V_{OUT}=V_{BATn}/n$

Bit 4~3 Reserved bits

Bit 2~0 **B2~B0**: 8-to-1 analog multiplexer selection bits (MSB: B2, LSB: B0)
Control B2~B0 to select which accumulative cell voltage to be output to VOUT.

EN_S	B2	B1	B0	V_{OUT} (V)
0	—	—	—	0
1	0	0	0	V_{BAT1} × 1/1
1	0	0	1	V_{BAT2} × 1/2
1	0	1	0	V_{BAT3} × 1/3
1	0	1	1	V_{BAT4} × 1/4
1	1	0	0	V_{BAT5} × 1/5
1	1	0	1	V_{BAT6} × 1/6
1	1	1	0	V_{BAT7} × 1/7
1	1	1	1	V_{BAT8} × 1/8

- **Charge Balance Register**

Bit	7	6	5	4	3	2	1	0
Name	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **CB8**: Enable control of the charge balance switch between VBAT8 and VBAT7
0: Balance switch OFF
1: Balance switch ON

Bit 6 **CB7**: Enable control of the charge balance switch between VBAT7 and VBAT6
0: Balance switch OFF
1: Balance switch ON

Bit 5 **CB6**: Enable control of the charge balance switch between VBAT6 and VBAT5
0: Balance switch OFF
1: Balance switch ON

Bit 4 **CB5**: Enable control of the charge balance switch between VBAT5 and VBAT4
0: Balance switch OFF
1: Balance switch ON

Bit 3 **CB4**: Enable control of the charge balance switch between VBAT4 and VBAT3
0: Balance switch OFF
1: Balance switch ON

Bit 2 **CB3**: Enable control of the charge balance switch between VBAT3 and VBAT2
0: Balance switch OFF
1: Balance switch ON

Bit 1 **CB2**: Enable control of the charge balance switch between VBAT2 and VBAT1
0: Balance switch OFF
1: Balance switch ON

Bit 0 **CB1**: Enable control of the charge balance switch between VBAT1 and GND
0: Balance switch OFF
1: Balance switch ON

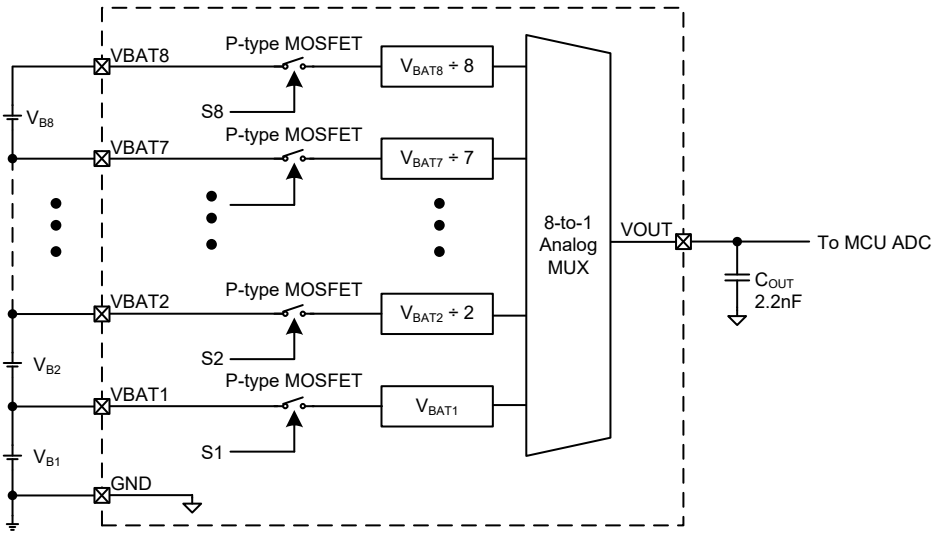
Accumulative Cell Voltage Monitor

The accumulative cell voltage monitor consists of high voltage switches, voltage dividers and an 8-to-1 analog multiplexer as shown in the following diagram. The high voltage switches are implemented using an anti-reverse current topology which provides isolation between the output voltage and the unselected VBATn.

EN_S, B2, B1 and B0 are four control bits from I²C interface and are used to control the P-type MOSFET S1~S8 only if EN_S="1". The control truth table is shown below. This produces an accumulative cell voltage, VBATn, divided by "n" on VOUT. This accurate ±0.5% voltage divided ratio is designed to minimize any mismatch errors.

EN_S	B2	B1	B0	S8	S7	S6	S5	S4	S3	S2	S1	V_{OUT} (V)
0	X	X	X	1	1	1	1	1	1	1	1	0
1	0	0	0	1	1	1	1	1	1	1	0	V_{BAT1} × 1/1
1	0	0	1	1	1	1	1	1	1	0	1	V_{BAT2} × 1/2
1	0	1	0	1	1	1	1	1	0	1	1	V_{BAT3} × 1/3
1	0	1	1	1	1	1	1	0	1	1	1	V_{BAT4} × 1/4
1	1	0	0	1	1	1	0	1	1	1	1	V_{BAT5} × 1/5
1	1	0	1	1	1	0	1	1	1	1	1	V_{BAT6} × 1/6
1	1	1	0	1	0	1	1	1	1	1	1	V_{BAT7} × 1/7
1	1	1	1	0	1	1	1	1	1	1	1	V_{BAT8} × 1/8

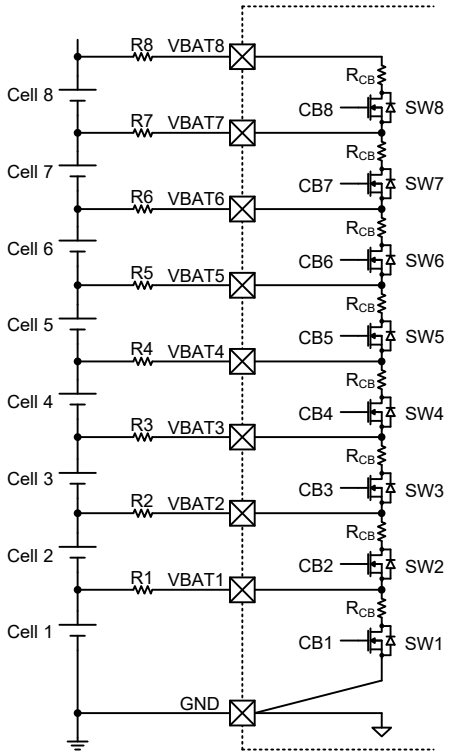
Accumulative Cell Voltage Monitor Truth Table



Accumulative Cell Voltage Monitor Functional Block

Charge Balance

Multiple channels of charge balance switch can be turned on by host MCU via I²C interface. The register address of charge balance function is 01H, and the Bit 7 ~ Bit 0 of Data byte correspond to the charge balance switch of each channel from CB8 to CB1, respectively. More than one switch can be turned on at the same time, **but side-by-side cell balancing switches are recommended not to be turned on simultaneously to ensure equal balance current between each channel**. After receiving a turn on command, the charge balance switch remains turned on until it is turned off by a "0" data or getting a command of SLP bit="1". The typical charge balance current is 10mA when the battery cell voltage is 4.2V and the external series resistance is 100Ω, and the balance current can be adjusted by series resistors R1~R8. **Note that for the reason of keeping voltage monitor accuracy, do not proceed voltage monitor while charge balance is activated**.



CB1	CB2	CB3	CB4	CB5	CB6	CB7	CB8	Balance Switch ON/OFF
1	0	0	0	0	0	0	0	SW1 ON, others OFF
0	1	0	0	0	0	0	0	SW2 ON, others OFF
0	0	1	0	0	0	0	0	SW3 ON, others OFF
0	0	0	1	0	0	0	0	SW4 ON, others OFF
0	0	0	0	1	0	0	0	SW5 ON, others OFF
0	0	0	0	0	1	0	0	SW6 ON, others OFF
0	0	0	0	0	0	1	0	SW7 ON, others OFF
0	0	0	0	0	0	0	1	SW8 ON, others OFF

Note: More than one switch can be turned on in the same time.

Discharge N-type MOSFET Gate Driver

Two discharge NMOS gate drivers DGN0 and DGN1 are fabricated in the chip as discharge switch controllers. The output voltage of DGN0 and DGN1 are both clamped at 12V. A 430kΩ pull-down resistor is integrated in the discharge gate control input pins DN0 and DN1. The gate driver capability of DGN0 is better than that of DGN1, therefore it is recommended to apply DGN0 on primary loading path and DGN1 on secondary loading path. While operating in the Standby or Sleep mode, the DGN0 and DGN1 are pulled down by 5Ω and 8.5Ω respectively. The control logic and output status of DGN0 and DGN1 in each state are listed in the following table.

SLP	DN0	V(DGN0, GND)	Note
0	Floating	0	Pulled low to GND by 5Ω.
0	0	0	
0	1	V_Z	Normal operation.
1	Floating	0	Pulled low to GND by 5Ω.
1	0	0	

SLP	DN1	V(DGN1, GND)	Note
0	Floating	0	Pulled low to GND by 8.5Ω.
0	0	0	
0	1	V_Z	Normal operation.
1	Floating	0	Pulled low to GND by 8.5Ω.
1	0	0	

Charge N-type MOSFET Gate Driver

A charge NMOS gate driver DGCN is provided as a charge switch controller. A charge pump circuit is fabricated to provide 12V between the gate and source node of external charge NMOS. A 430kΩ pull-down resistor is integrated in the control input pin DCN. The control logic of DCN and output status of DGCN and DSCN in each state are listed in the following table.

SLP	DCN	V(DGCN, DSCN)	Note
0	Floating	0	DGCN and DSCN pulled low to GND by 50Ω respectively. DGCN pulled low to DSCN by 90Ω.
0	0	0	
0	1	V_Z	Normal operation.
1	Floating	0	DGCN and DSCN pulled low to GND by 830Ω respectively. DGCN pulled low to DSCN by 1.65kΩ.
1	0	0	

Sleep Mode

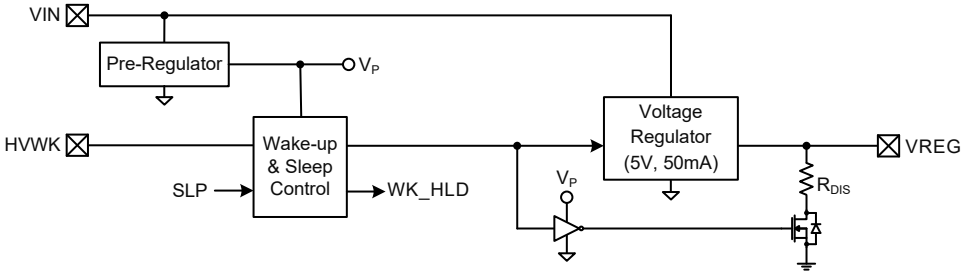
EXT_WK represents the external wake-up event status. EXT_WK="0" means that high voltage applied on the HVWK pin is not detected, on the contrary EXT_WK="1" denotes that wake-up event is happening such as charger connecting or power switch on. When receiving a sleep command from I²C master at EXT_WK="0", the SLP bit is set to "1" and the chip enters the Sleep mode. During the Sleep mode, all outputs are shut down and the capacitor of VREG is discharged through internal discharge resistor. The pre-regulator and high voltage wake-up circuit are the only blocks that are still working in the Sleep mode and operate with an ultra-low standby current of 0.1μA (typical).

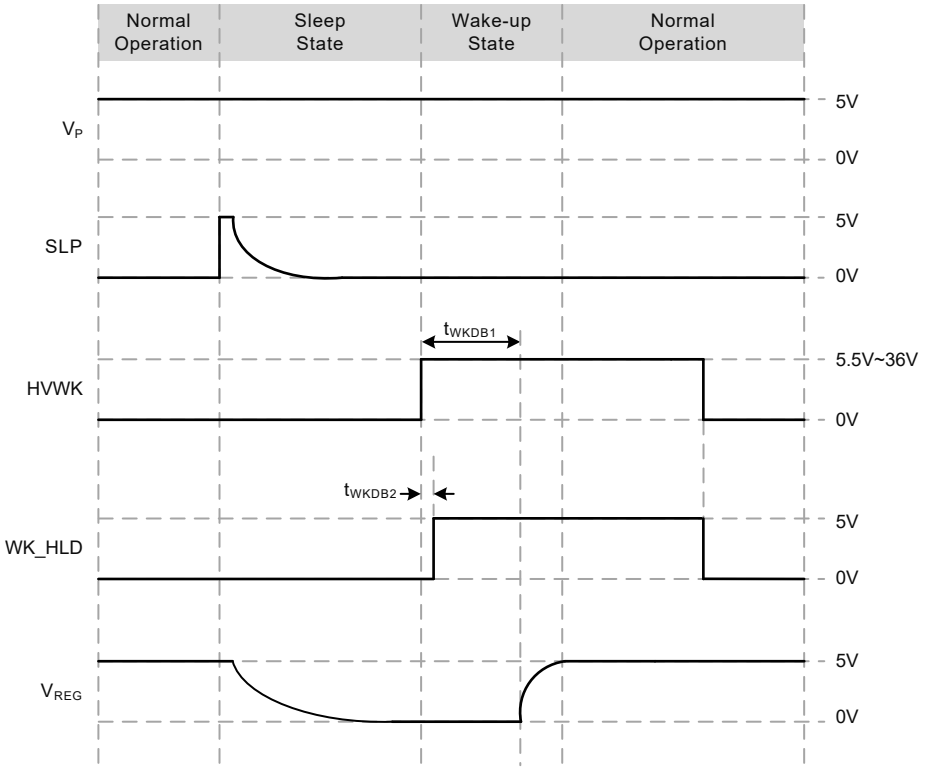
When EXT_WK="1", the SLP will be cleared to "0" and the sleep command from I²C master will be abandoned until EXT_WK is cleared to "0".

EXT_WK Status	SLP Status
0	According to I²C master command or POR default.
1	0

Wake up from Sleep Mode

The HVWK pin can be used for detecting charger plugged-in, switch turned on, or load connected events. When the device is under the Sleep mode, if the HVWK pin is triggered by a pulse with requiring at least 5.5V voltage and 1ms width, the output of VREG will resume and the whole chip is ready for normal operation. The reference timing diagram of entering the Sleep mode and waked up is listed below.

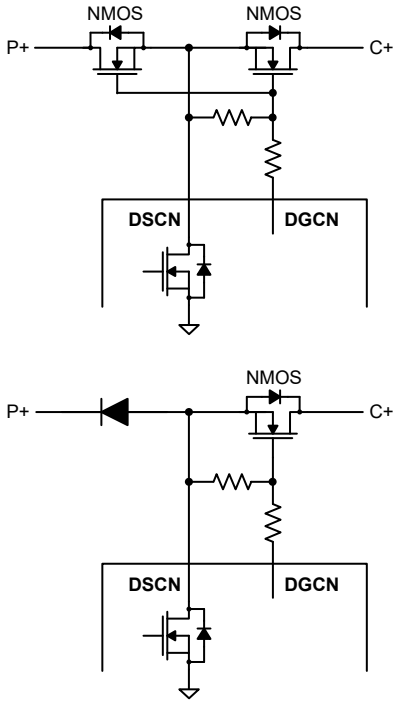




Application Information

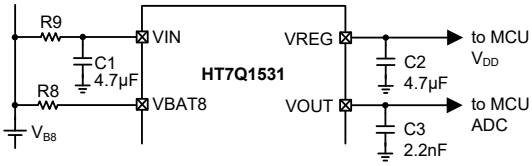
Charge NMOS Switch Configuration

Due to the internal pull down MOS switch between DSCN and GND, the recommended Charge NMOS switch configuration is back-to-back or single NMOS in series with a diode in order to avoid the DSCN pin draining current from battery.



VIN, VREG, VOUT Capacitors

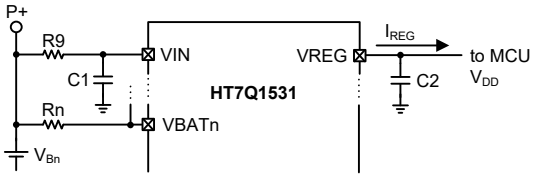
The VIN input capacitor C1 and VREG output capacitor C2 are 4.7μF for better input noise filtering and output load transient behavior. A recommended 2.2nF noise filtering capacitor should be connected between VOUT and GND terminals. Note that higher noise capacitance value of C3 will lower the acceptable scan frequency.



VIN Filter Recommendation

The input capacitor C1 for VIN is used for lowering the input voltage ripple while the battery is supplying a highly inductive load in PWM mode. The recommanded value of VIN input capacitor C1 is 4.7μF. The input resistor R9 of VIN is able to reduce the inrush current during battery assembly, and also it shares the heat on chip while VREG outputs a large current in normal operation mode. The recommanded value for VIN input resistor R9 differs from different battery cell number applications. The recommended resistance values of VIN input resistor R9 with different battery cell numbers and the corresponding VREG maximum output current are listed in the following table.

Battery Cell Number	VIN Recommended Resistor (R9)	VREG Maximum Output Current
3S	15Ω	50mA
4S	43Ω	50mA
5S	110Ω	40mA
6S	220Ω	35mA
7S	330Ω	30mA
8S	430Ω	30mA



It is necessary to select an appropriate package for VIN filter resistor (R9) in order to prevent it being damaged from overheated. The maximum power on R9 is easily calculated by:

$$P_{R9.MAX} = (I_{REG})^2 \times R9$$

where I_{REG} is the maximum VREG output current, R9 is the resistance value of VIN filter resistor (R9)

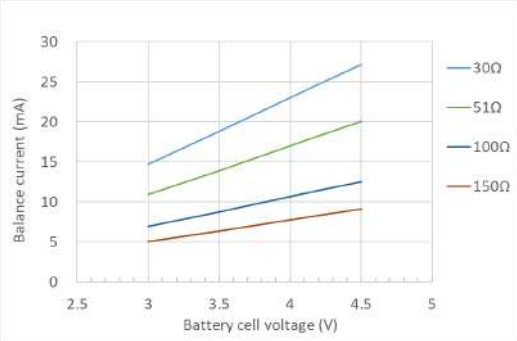
It is recommended to choose the resistor package that its maximum rated power is greater than twice the $P_{R9.MAX}$.

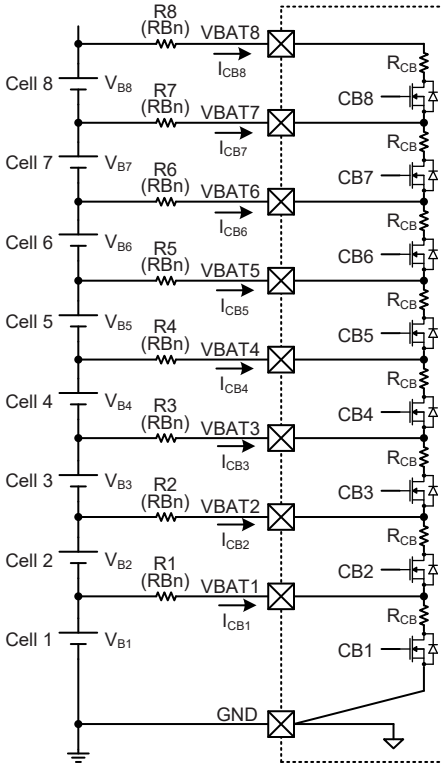
VBATn Protection and Balance Resistor Selection

The VBATn series resistors R1~R8 not only suppress inrush and noise spikes applied to I/O pins, they affect charge balance current as well. Larger resistance of R1~R8 provide better protection to VBATn and other I/O pins, but they lower the charge balance current instead. The charge balance current of each channel is configured by internal balance resistance and external series resistors. Because the balance current of Cell 1 flows out through the GND pin, the balance current of Cell 1 is greater than that of other cells. Considering inrush spike protection to I/O pins and noise reduction of voltage monitor, the recommended typical values of resistor R1~R8 are 100Ω, and the charge balancing current is 11mA while the voltage of battery cell is 4.2V. If larger balancing current is needed, the recommended minimum values of the R1~R8 resistors are 30Ω which

provide 25mA while the voltage of battery cell is 4.2V. To ensure the internal balance circuit works properly, the minimum battery cell voltage to start the balance function is 3V. The recommended VBATn series resistances and their related charge balancing current are listed in the following table.

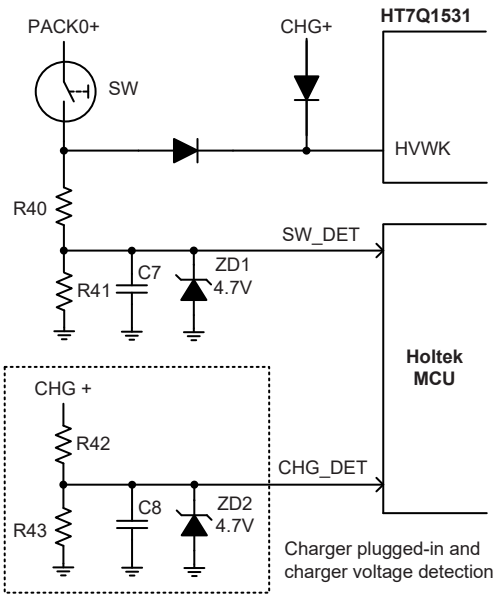
Resistance of R1~R8	Typical Balancing Current (@ V_{Bn}=4.2V)	Note
30Ω	25mA	Minimum value of resistors R1~R8
51Ω	18mA	—
100Ω	11mA	—
150Ω	8.4mA	—





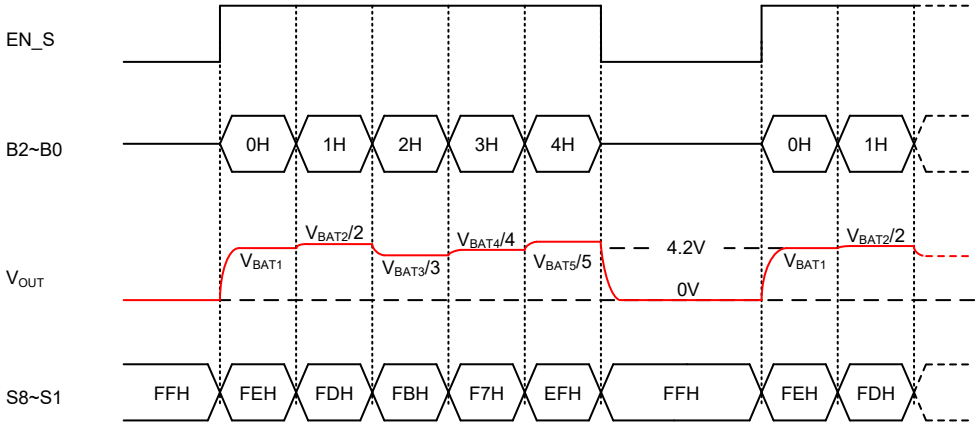
Charger and Switch Status Detection for MCU

The High-voltage wake-up (HVWK) function is capable of detecting charger plugged in or load switched on. The recommended HVWK external circuit is listed below. When a charger is plugged in or load switch is on, the voltage of HVWK is triggered to be larger than V_{WKTH} and set EXT_WK bit as "1". After the charger or switch is removed or turned off, the EXT_WK bit is reset to "0". An MCU can acquire the charger or switch status by reading the EXT_WK bit through the I^2C interface. Therefore, by the means of reading the EXT_WK bit status, additional charger or switch detection circuit for MCU are not necessary. The circuit below is a typical application for high-voltage wake-up function, charger plugged-in detection and charger voltage detection.

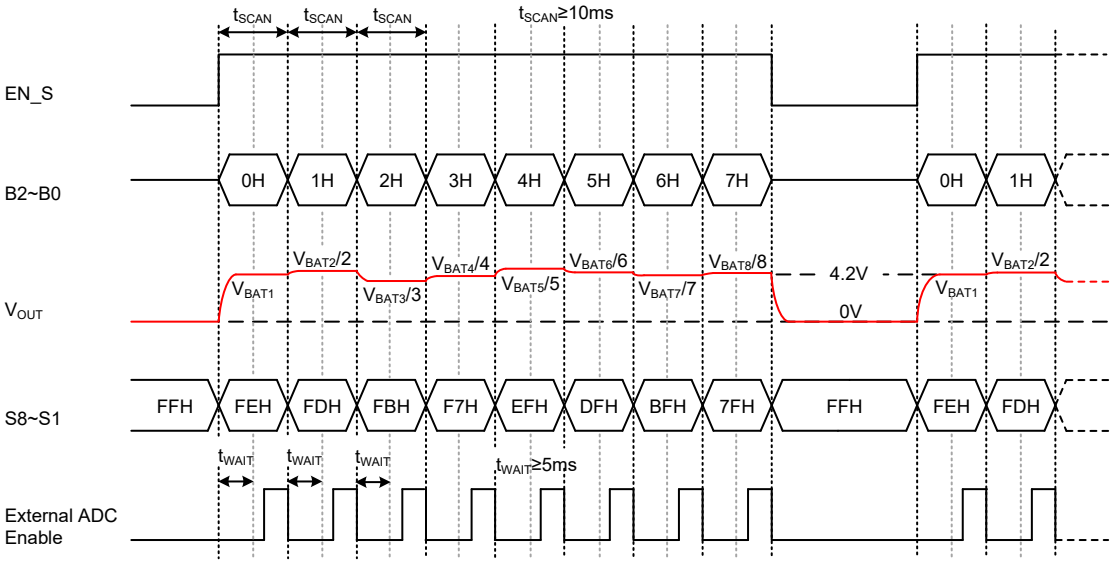


Cell Voltage Monitor Scan Frequency

The VOUT pin outputs accumulative cell voltage to external MCU ADC for monitoring battery voltage status. The timing diagrams of cell voltage monitor scanning for 5S and 8S applications are shown below. The VOUT pin starts to charge the VOUT capacitor from 0V to the selected cell voltage while the EN_S is set to "1". In order to ensure external MCU A/D conversion accuracy, the A/D conversion procedure has to wait before the VOUT capacitor is fully charged. The suggested minimum waiting time is 5ms after the EN_S is set to "1" or cell voltage monitor channel switched. It is recommended that the maximum scan frequency for accumulative cell voltage monitoring is less than 100Hz and that EN_S="0" when the voltage scanning procedure has finished for power saving purposes.



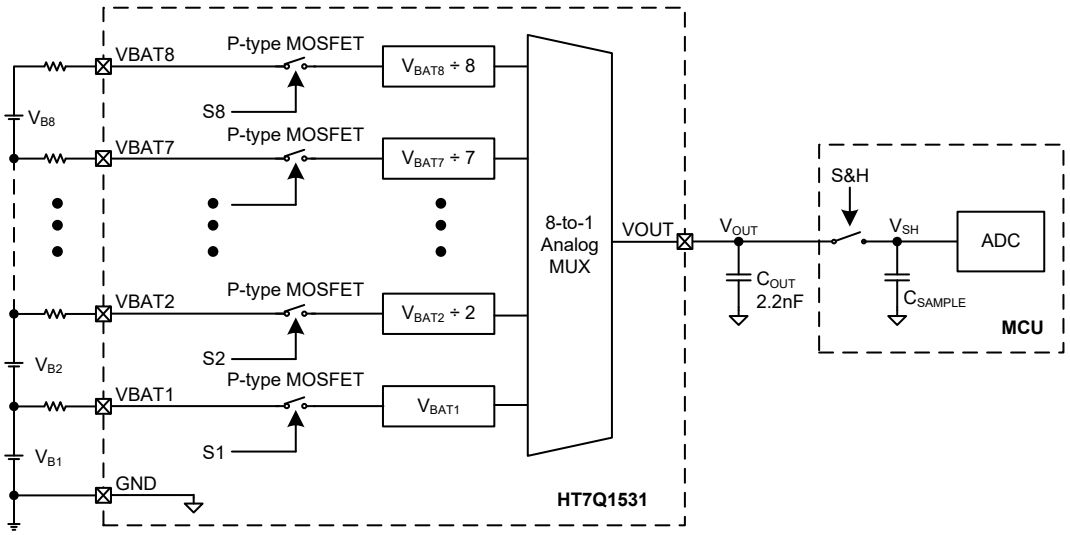
5S Battery Monitoring Timing



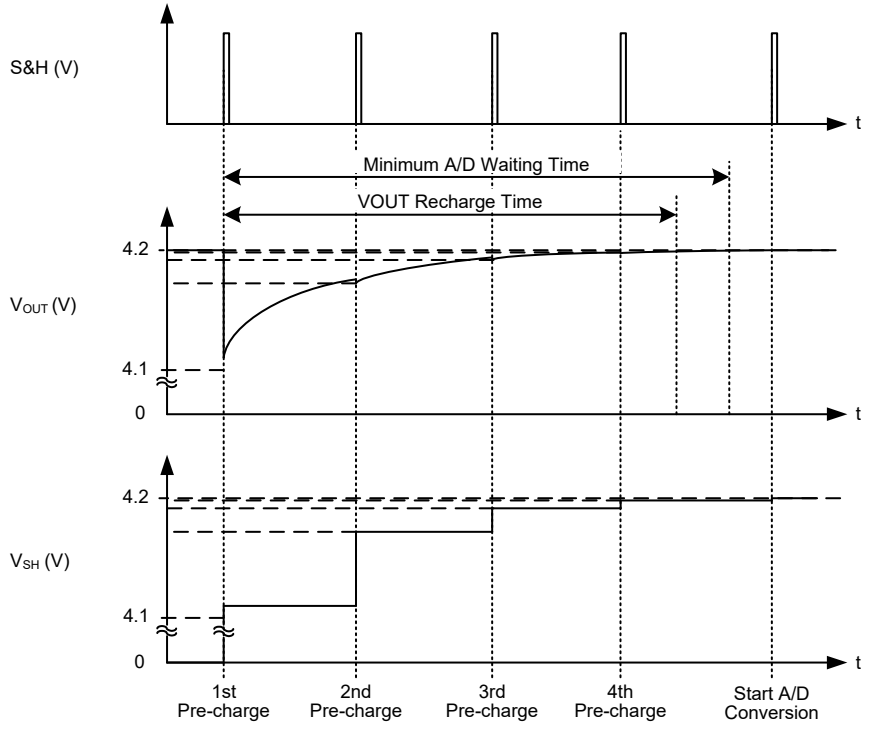
8S Battery Monitoring Timing

Acquiring Cell Voltage Monitor Output with External MCU ADC

The accumulative battery cell voltage is output through the VOUT pin to an external MCU for monitoring the battery voltage status. As shown in the following block diagram, the external MCU ADC samples the V_{OUT} voltage via an ADC sampling capacitor (C_{SAMPLE}), which is typically 5pF to 50pF. Due to the charge sharing effect, the voltage on the VOUT capacitor (C_{OUT}) drops while the ADC samples that with initially zero-voltage C_{SAMPLE}. A voltage-drop occurs on the C_{OUT} after the first ADC sampling, and then it needs a recharge time to recharge the C_{OUT}. Referring to the following timing diagram, a pre-charge procedure of C_{SAMPLE} during the VOUT recharge time is recommended to minimize the charge sharing effect by the means of performing several sampling without clearing the charges in the C_{SAMPLE}.



HT7Q1531 + MCU ADC Functional Block



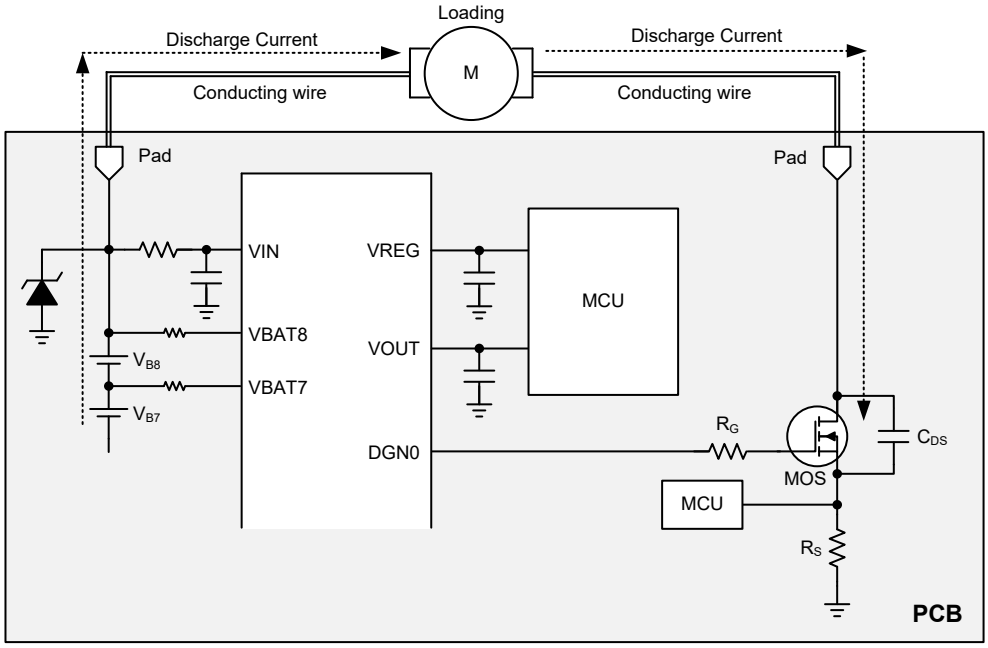
ADC Sampling Recommended Timing

For the best conversion accuracy, the A/D conversion has to wait before C_{OUT} recharge is complete. The recommended minimum waiting time from the first sampling to A/D conversion beginning is listed in the following table.

MCU ADC Sampling Capacitance (pF)	Recommended Minimum A/D Waiting Time (μs)
5	370
10	660
20	950
30	1120
40	1240
50	1340

ADC Recommended Waiting Time

Voltage Spike Suppression Method



Simplified Typical BMS System Discharge Path Diagram

Most battery-management systems would monitor charge and discharge current to prevent over-current damage. Due to the parasitic inductance on conducting wires and PCB layout connections, large voltage spike may occurs while the external MOS rapidly shuts down the charge or discharge current, and this spike may damage the device VBATn or VIN pins. Any voltage spike on the VBATn and VIN pins should not over the limitation in Absolute Maximum Ratings, which is 48V. Four recommended measures listed below would help to reduce the voltage spike.

1. Make the external conducting wire and PCB layout connections as short as possible where large charge or discharge current flows.
2. Adjust the slew rate of MOS switch with the gate resistor R_G. Turn off the MOS with slower slew rate for lower voltage spike, and the tradeoff is a slower protection response time.
3. Add a capacitor (C_{DS}) between drain and source node of the MOS switch as shown above. The recommended capacitance is 0.1μF to 0.22μF.
4. Add a Zener diode between the highest voltage potential node of battery cells and GND.

PCB Layout Considerations

The following component placement and layout guidelines are suggested for the sake of noise reduction and voltage spike suppression.

1. The VIN filter capacitor must be close to VIN pin.
2. The VREG regulation and noise filter capacitor must be close to VREG pin.
3. The tracks where large current would flow through should be wide and short to suppress the voltage spike at the time when external NMOS switch change its ON/OFF state.
4. Minimize VBA©T1~VBAT8 signal trace length to reduce parasitic inductance and capacitance and improve measure accuracy.

Thermal Considerations

The maximum power dissipation depends upon the thermal resistance of the IC package, PCB layout, rate of surrounding airflow and difference between the junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

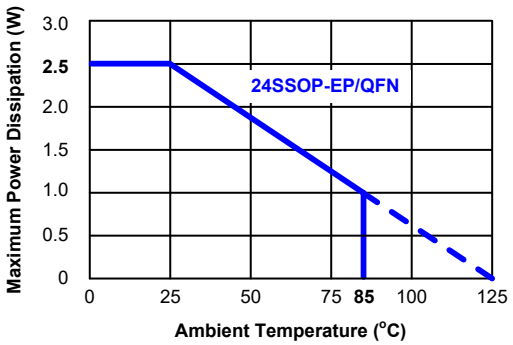
$$P_{D(MAX)} = (T_{J(MAX)} – Ta) / \theta_{JA} (W)$$

where $T_{J(MAX)}$ is the maximum junction temperature, Ta is the ambient temperature and θ_{JA} is the junction-to-ambient thermal resistance of IC package.

For maximum operating rating conditions, the maximum junction temperature is 125°C. However, it is recommended that the maximum junction temperature does not exceed 125°C during normal operation to maintain high reliability. The de-rating curve of the maximum power dissipation is show below:

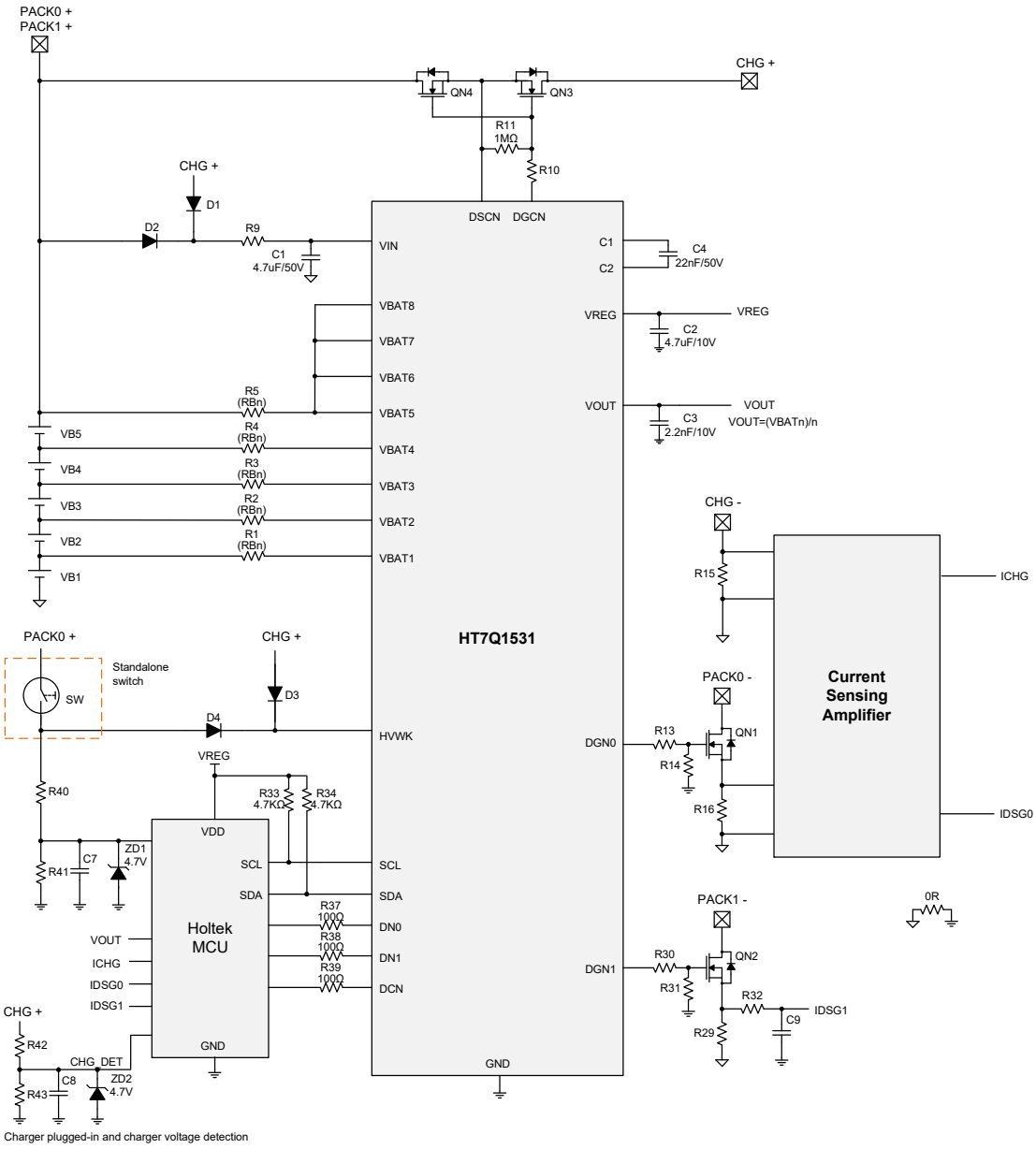
$$P_{D(MAX)} = (125°C-25°C) / (40°C/W) = 2.5W$$

For a fixed $T_{J(MAX)}$ of 125°C, the maximum power dissipation depends upon the operating ambient temperature and the package's thermal resistance, θ_{JA}. The de-rating curve below shows the effect of rising ambient temperature on the maximum recommended power dissipation.

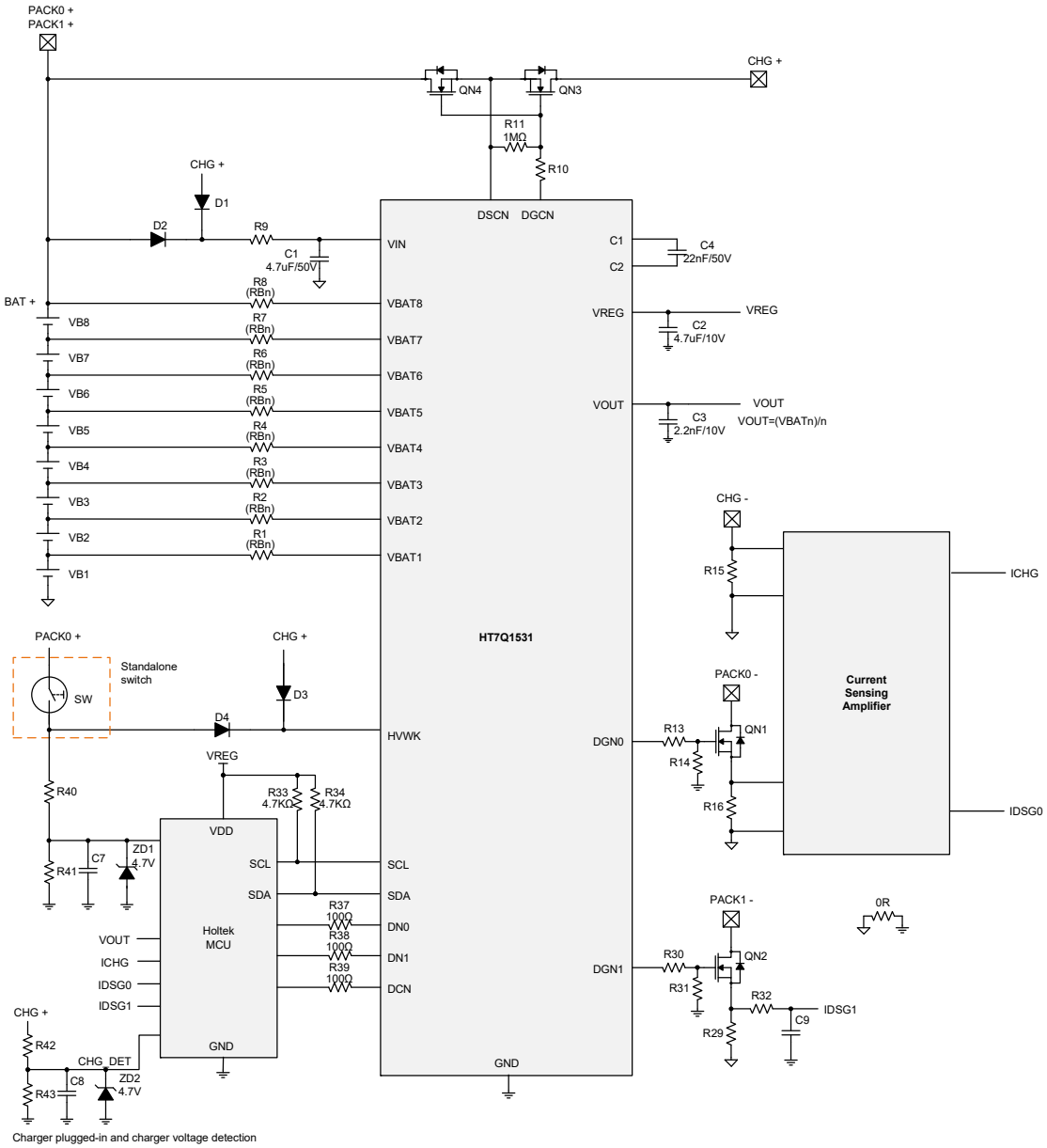


Application Circuits

HVWK Connected to Standalone Switch and Charger Input (5S)



HVWK Connected to Standalone Switch and Charger Input (8S)

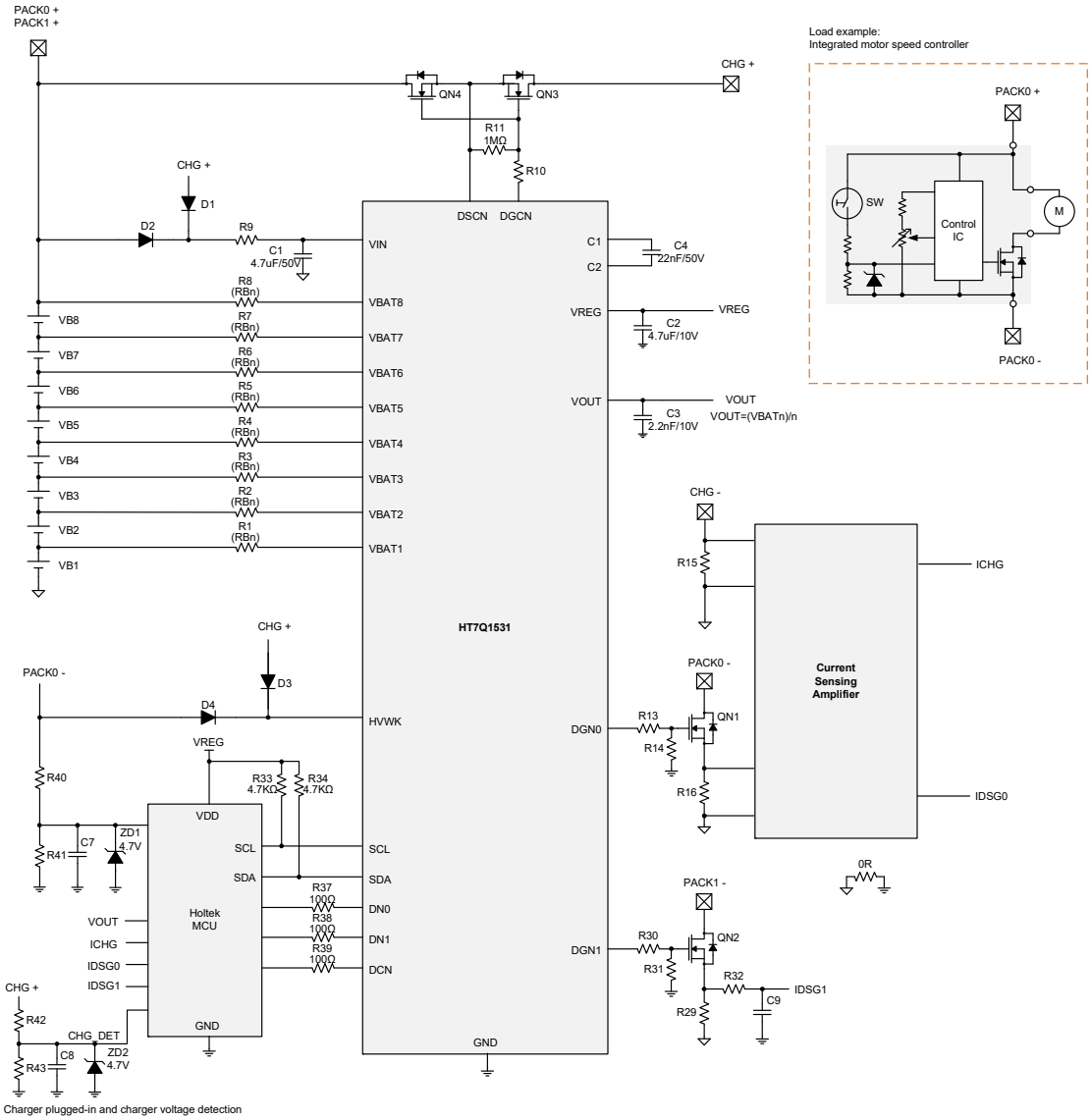


Note: 1. The resistance of R1~R8 can be adjusted to fit the desired balance current. The recommended resistance of R1~R8 are listed in the "VBATn Protection and Balancing Resistor Selection" section.

2. If less than 8 serial batteries are used, connect the unused VBATn to the highest voltage potential. Do not leave any VBATn pin floating in order to prevent damage to the device.

3. The VIN pin should not be floating to prevent abnormal operations.

HVWK Connected to Integrated Switch Control Unit and Charger Input



Charger plugged-in and charger voltage detection

Note: 1. The resistance of R1~R8 can be adjusted to fit the desired balance current. The recommended resistance of R1~R8 are listed in the "VBATn Protection and Balancing Resistor Selection" section.

2. If less than 8 serial batteries are used, connect the unused VBATn to the highest voltage potential. Do not leave any VBATn pin floating in order to prevent damage to the device.

3. The VIN pin should not be floating to prevent abnormal operations.

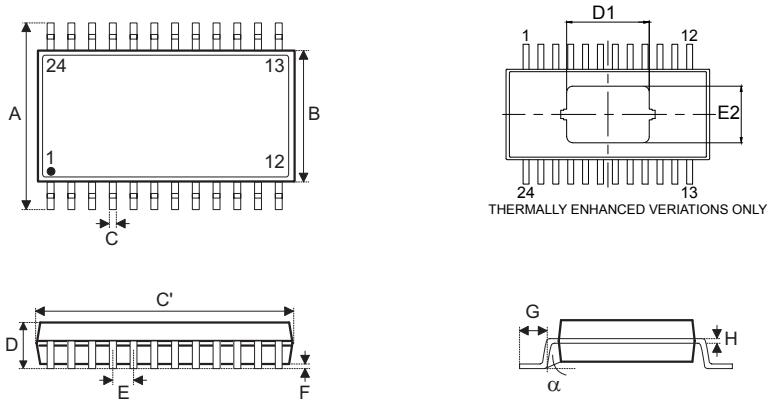
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

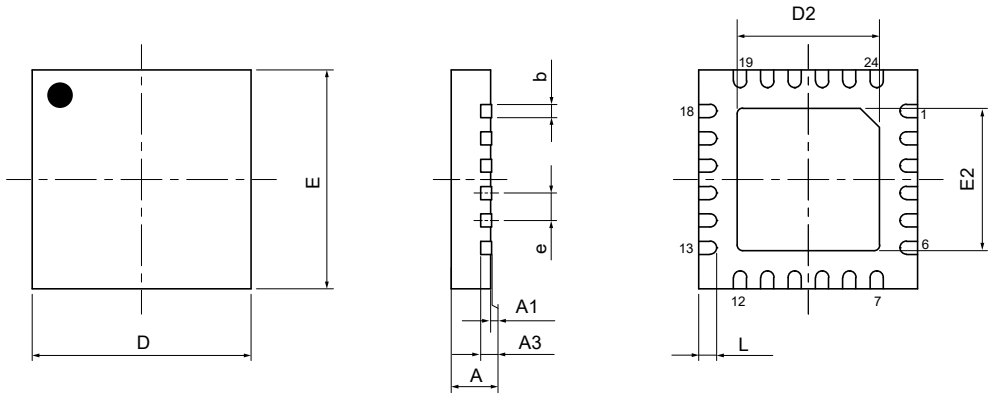
24-pin SSOP-EP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.008	—	0.012
C’	—	0.341 BSC	—
D	—	—	0.069
D1	0.119	—	0.146
E	—	0.025 BSC	—
E2	0.081	—	0.102
F	0.000	—	0.004
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions mm		
	Min.	Nom.	Max.
A	—	6.00 BSC	—
B	—	3.90 BSC	—
C	0.20	—	0.30
C’	—	8.66 BSC	—
D	—	—	1.75
D1	3.02	—	3.71
E	—	0.635 BSC	—
E2	2.06	—	2.59
F	0.00	—	0.10
G	0.41	—	1.27
H	0.10	—	0.25
α	0°	—	8°

SAW Type 24-pin QFN (4mm×4mm×0.75mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008 REF	—
b	0.007	0.010	0.012
D	—	0.157 BSC	—
E	—	0.157 BSC	—
e	—	0.020 BSC	—
D2	0.100	—	0.108
E2	0.100	—	0.108
L	0.014	0.016	0.018

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	—	0.203 REF	—
b	0.18	0.25	0.30
D	—	4.00 BSC	—
E	—	4.00 BSC	—
e	—	0.50 BSC	—
D2	2.55	—	2.75
E2	2.55	—	2.75
L	0.35	0.40	0.45