Features

- V_{IN} Input Range from 7.5V to 36V
- Accumulative Cell Voltage Monitor
- 8-to-1 Analog Multiplexer with divided ratio accuracy: 1/n ± 0.5%
- Reverse-current prevention switching scan frequency of 100Hz
- Requires fewer MCU A/D Converters (ADCs)
- 5V/30mA internal Voltage Regulator with ±1% accuracy
- Sleep Mode with 0.1μA ultra-low standby current
- Direct High Voltage Wake-up function
- Operating Temperature Range: -40°C to +85°C
- Package Types: 16-pin NSOPand 24-pin SSOP (150mil)

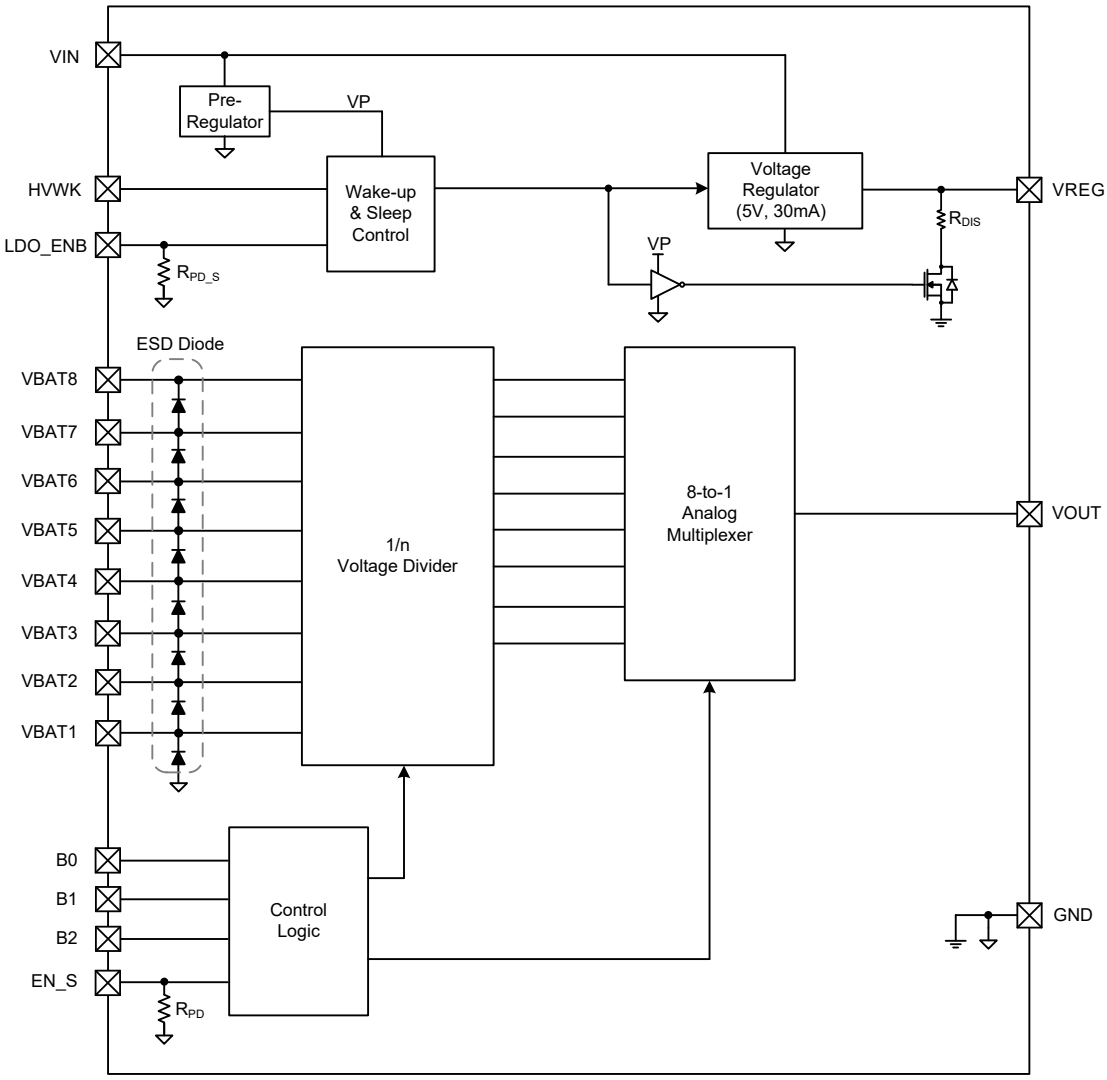
Applications

- Electric power tools
- Handheld vacuum cleaners

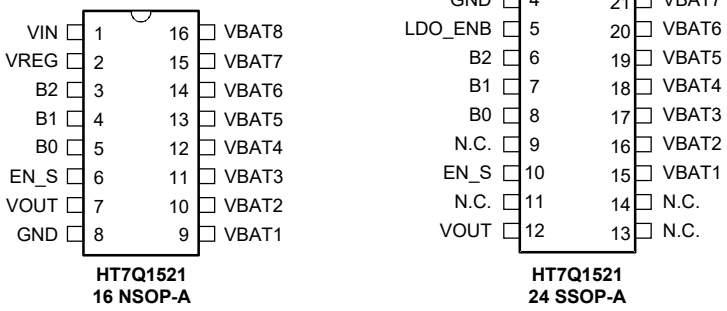
General Description

The HT7Q1521 is a high voltage analog-front-end IC for 3 to 8 cell Li-ion rechargeable battery protection. It consists of an accumulative cell voltage monitor and a high accuracy voltage regulator. The device is designed to monitor an accumulative voltage from 1 to N and outputs the divide-by-N voltage to the analog multiplexer with a ±0.5% divided ratio accuracy. The anti-reverse current switch is implemented to prevent a backflow current even if V_{OUT} is higher than V_{BATn}. Each divided accumulative cell voltage can be observed sequentially from VBAT1 to VBAT8 which benefits MCUs with a lower number of ADCs. There are 3 control bits, B0, B1 and B2, to select which terminal voltage outputs with a maximum 100Hz scanning frequency when C_{OUT}=2.2nF. The enable pin, EN_S, is used to close all switches and the output voltage is pulled down by an internal 1MΩ resistor. An integrated regulator provides a 5V supply to the MCU with a 30mA driving current capability and which has ±1% accuracy. The voltage regulator and cell voltage monitor are shut down with an ultra-low standby current of 0.1μA when the device is in the Sleep Mode. When the HVWK pin is triggered by a voltage greater than its threshold, the device will return to the normal operating state.

Functional Block Diagram



Pin Assignment



Pin Description

Pin No.		Pin Name	Type	Pin Description
16NSOP	24SSOP			
1	1	VIN	P	Input supply voltage. Connect to the top VBATn
2	3	VREG	O	Regulator 5V/30mA output. Connect a 4.7μF capacitor to GND
8	4	GND	G	Ground terminal
—	5	LDO_ENB	I	Sleep Mode enable pin. Chip enters Sleep Mode by applying LDO_ENB pin 5V
3	6	B2	I	8-to-1 analog multiplexer selection bit – MSB
4	7	B1	I	8-to-1 analog multiplexer selection bit
5	8	B0	I	8-to-1 analog multiplexer selection bit – LSB
6	10	EN_S	I	Enable terminal for the 8-to-1 analog multiplexer. Connected to 1MΩ internal pull low resistor
7	12	VOUT	O	8-to-1 analog multiplexer output. Connect a 2.2nF capacitor to GND.
9	15	VBAT1	I	Battery cell 1 positive terminal and battery cell 2 negative terminal
10	16	VBAT2	I	Battery cell 2 positive terminal and battery cell 3 negative terminal.
11	17	VBAT3	I	Battery cell 3 positive terminal and battery cell 4 negative terminal
12	18	VBAT4	I	Battery cell 4 positive terminal and battery cell 5 negative terminal
13	19	VBAT5	I	Battery cell 5 positive terminal and battery cell 6 negative terminal
14	20	VBAT6	I	Battery cell 6 positive terminal and battery cell 7 negative terminal
15	21	VBAT7	I	Battery cell 7 positive terminal and battery cell 8 negative terminal
16	22	VBAT8	I	Battery cell 8 positive terminal
—	24	HVWK	I	Sense and trigger pin of High voltage Wake-up function.
—	Others	N.C.	—	Not connected

Note: I: Input; O: Output; P: Power; G: Ground;

Absolute Maximum Ratings

Pin / Parameter		Value	Unit
VIN, HVWK		-0.3 to +48	V
VREG, OUT, B2, B1, B0, EN_S, LDO_ENB, VBAT1		-0.3 to +5.5	V
$\Delta[V_{BATi}\sim V_{BAT(i-1)}]$, i=8, 7, 6, 5, 4, 3, 2		-0.3 to +5.5	V
Operating Temperature Range		-40 to +85	°C
Maximum Junction Temperature		+125	°C
Storage Temperature Range		-60 to +150	°C
Lead Temperature (Soldering 10sec)		+260	°C
ESD Susceptibility	Human Body Model	±2000	V
	Machine Model	±200	V
Junction-to-Ambient Thermal Resistance, θ_{JA}	16NSOP (150mil)	100	°C/W
	24SSOP (150mil)	85	°C/W

Note: Absolute Maximum Ratings indicate limitations beyond which damage to the device may occur.

Recommended Operating Ratings

Pin / Parameter	Value	Unit
VIN	7.5 to 36	V
Ta	-40 to +85	°C

Note: Recommended Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specified performance limits.

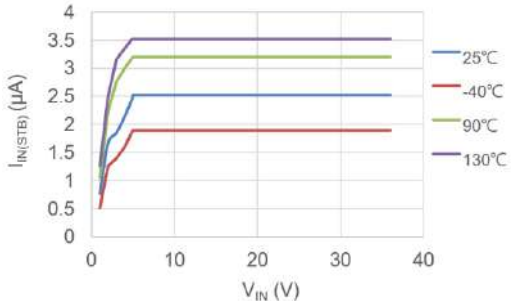
Electrical Characteristics

V_{IN}=36V, C_{REG}=4.7μF, C_{OUT}=2.2nF, Ta=25°C, unless otherwise specified

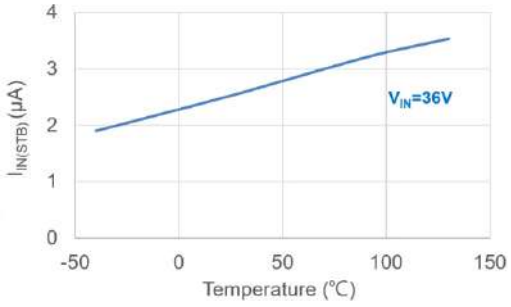
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply and Input						
V_{IN}	Supply Voltage	—	7.5	—	36.0	V
$I_{IN(SCAN)}$	Supply Current – Scan	EN_S=1, Scan B2~B0 with frequency 100Hz	—	2.5	4.0	μA
$I_{IN(STB)}$	Supply Current – Standby	B0=B1=B2=EN_S=0	—	2.5	4.0	μA
I_{SLP}	Standby Current in SLEEP Mode	V_{LDO_ENB}=5V, V_{HVWK}=0V	—	0.1	0.2	μA
t_{ENBDB}	LDO_ENB Pin Debounce Time	—	—	1.8	—	μs
Voltage Regulator						
V_{REG}	Regulator Output Voltage	I_{LOAD}=10mA	4.95	5.00	5.05	V
I_{REG}	Regulator Output Current	V_{IN}=7.5V, Ta=-40~85°C	30	—	—	mA
ΔV_{REG}	Load Regulation	I_{LOAD}=0~30mA	—	50	—	mV
$\Delta V_{REG}/(V_{REG}\times\Delta V_{IN})$	Line Regulation	V_{IN}=7.5V~36V, I_{LOAD}=10mA	—	0.02	—	%/V
$\Delta V_{REG}/(V_{REG}\times\Delta Ta)$	Temperature Coefficient	I_{LOAD}=1mA, Ta=-40~85°C	—	±100	—	ppm/°C
R_{DIS}	VREG Discharge Resistance	V_{LDO_ENB}=5V, V_{REG}=0.1V, I_{REG1} denotes VREG input current at V_{REG}=0.1V, $R_{DIS}=V_{REG}/I_{REG1}$	—	85	—	Ω
Input Logic						
f_{MAX}	B2~B0 Maximum Scan Frequency	C_{OUT}=2.2nF	100	—	—	Hz
V_{IH}	B2, B1, B0, EN_S, LDO_ENB Pins Input Logic High Threshold	V_{IN}=7.5V~36V	2.5	—	—	V
V_{IL}	B2, B1, B0, EN_S, LDO_ENB Pins Input Logic Low Threshold	V_{IN}=7.5V~36V	—	—	0.8	V

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R_{PD}	EN_S Pin Pull low Resistance	—	—	1	—	MΩ
R_{PD_S}	LDO_ENB Pin Pull Low Resistance	—	—	10	—	kΩ
I_{LEAK}	B2, B1 and B0 Pins Input Logic Leakage	V_{IN}=7.5V~36V	—	—	0.1	μA
High Voltage Wake-Up						
V_{WKTH}	HVWK Trigger Threshold Voltage	—	3.5	4.0	5.0	V
t_{WKDB1}	HVWK Trigger Debounce time	—	1	—	—	ms
I_{WK}	HVWK Input Current	V_{HVWK}=36V	—	50	—	μA
Accumulative Cell Voltage Monitor						
V_{Bi}	Cell Voltage Range	i=1~8	2.5	—	4.5	V
I_{Bi}	Cell Input Leakage Current	V_{BATi}=4.2V×i, i=1~8, EN_S=0, V_{IN}=V_{BAT8}	-0.1	—	0.1	μA
$I_{Bi(ACT)}$	Cell Input Current When Voltage Monitoring	V_{BATi}=4.2V×i, i=1~8, EN_S=1	19	24	35	μA
$I_{B1(REV)}$	VBAT1 Input Reverse Current	V_{BAT8}=36V, V_{BAT1}=2.5V, B2~B0=0b111, Measure I_{B1}	-0.1	—	0.1	μA
R	Divided Resistance	—	120	170	220	kΩ
$Ratio8_{(NORM)}$	VBAT8 Accumulative Cell Voltage Divided Ratio (Normalised)	V_{BAT8}=20V~36V, B2~B0=0b111, EN_S=1	0.995	1	1.005	—
		V_{BAT8}=20V~36V, B2~B0=0b111, EN_S=1, Ta=-40°C~85°C	0.99	1	1.01	—
$Ratio7_{(NORM)}$	VBAT7 Accumulative Cell Voltage Divided Ratio (Normalised)	V_{BAT7}=17.5V~31.5V, B2~B0=0b110, EN_S=1	0.995	1	1.005	—
		V_{BAT7}=17.5V~31.5V, B2~B0=0b110, EN_S=1, Ta=-40°C~85°C	0.99	1	1.01	—
$Ratio6_{(NORM)}$	VBAT6 Accumulative Cell Voltage Divided Ratio (Normalised)	V_{BAT6}=15V~27V, B2~B0=0b101, EN_S=1	0.995	1	1.005	—
		V_{BAT6}=15V~27V, B2~B0=0b101, EN_S=1, Ta=-40°C~85°C	0.99	1	1.01	—
$Ratio5_{(NORM)}$	VBAT5 Accumulative Cell Voltage Divided Ratio (Normalised)	V_{BAT5}=12.5V~22.5V, B2~B0=0b100, EN_S=1	0.995	1	1.005	—
		V_{BAT5}=12.5V~22.5V, B2~B0=0b100,EN_S=1, Ta=-40°C~85°C	0.99	1	1.01	—
$Ratio4_{(NORM)}$	VBAT4 Accumulative Cell Voltage Divided Ratio (Normalised)	V_{BAT4}=10V~18V, B2~B0=0b011, EN_S=1	0.995	1	1.005	—
		V_{BAT4}=10V~18V, B2~B0=0b011, EN_S=1, Ta=-40°C~85°C	0.99	1	1.01	—
$Ratio3_{(NORM)}$	VBAT3 Accumulative Cell Voltage Divided Ratio (Normalised)	V_{BAT3}=7.5V~13.5V, B2~B0=0b010, EN_S=1	0.995	1	1.005	—
		V_{BAT3}=7.5V~13.5V, B2~B0=0b010, EN_S=1, Ta=-40°C~85°C	0.99	1	1.01	—
$Ratio2_{(NORM)}$	VBAT2 Accumulative Cell voltage divided ratio (Normalised)	V_{BAT2}=5V~9V, B2~B0=0b001, EN_S=1	0.995	1	1.005	—
		V_{BAT2}=5V~9V, B2~B0=0b001, EN_S=1, Ta=-40°C~85°C	0.99	1	1.01	—
$Ratio1_{(NORM)}$	VBAT1 Accumulative Cell Voltage Divided Ratio (Normalised)	V_{BAT1}=2.5V~4.5V, B2~B0=0b000, EN_S=1	0.995	1	1.005	—
		V_{BAT1}=2.5V~4.5V, B2~B0=0b000, EN_S=1, Ta=-40°C~85°C	0.99	1	1.01	—

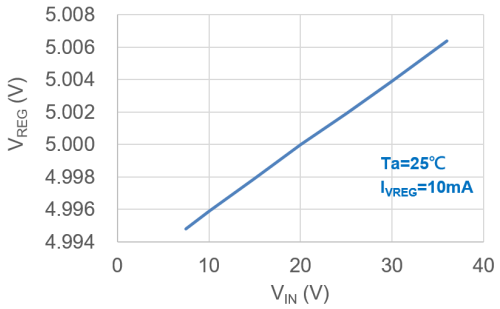
Typical Performance Characteristics



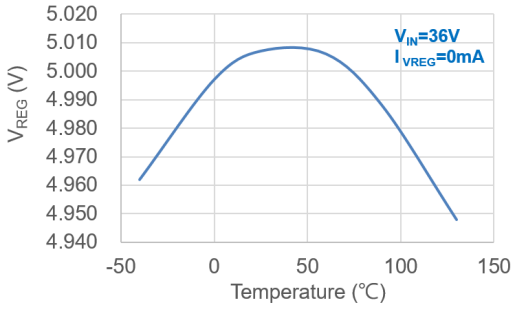
$I_{IN(STB)}$ vs. V_{IN}



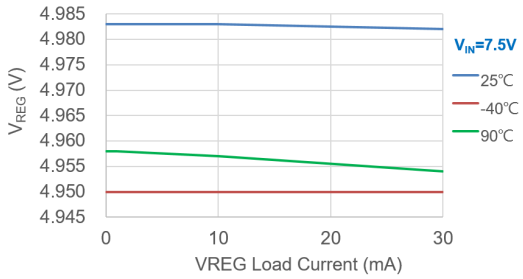
$I_{IN(STB)}$ vs. Temperature



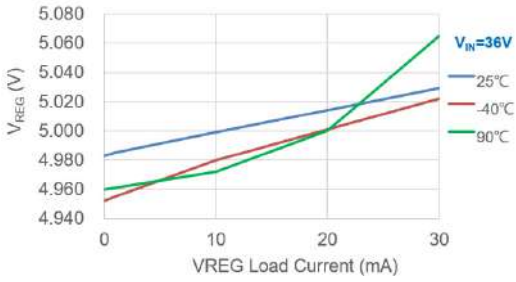
V_{REG} vs. V_{IN}



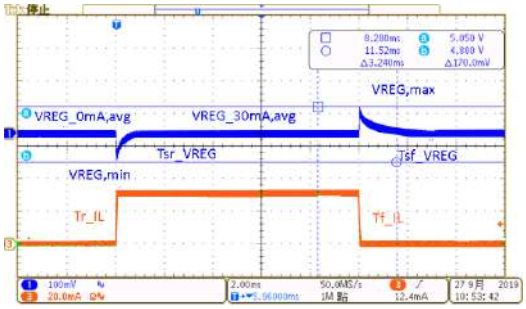
V_{REG} vs. Temperature



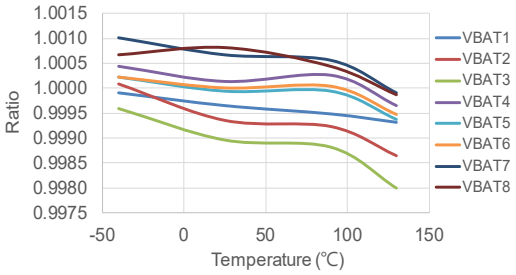
V_{REG} vs. Load Current



V_{REG} vs. Load Current

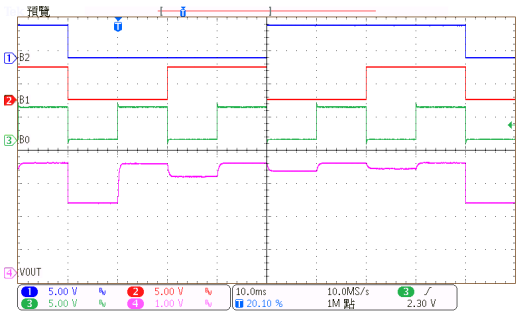


VREG Load Transient (0mA⇄30mA)

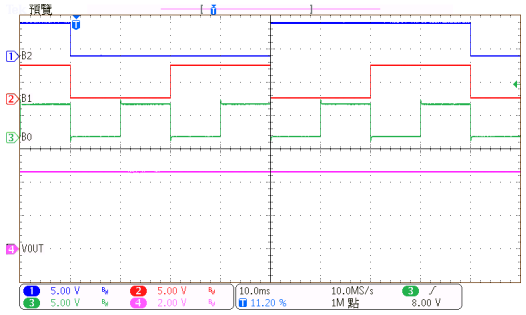


(Averaged values from 3 samples)

Cell Voltage Divided Ratio vs. Temperature

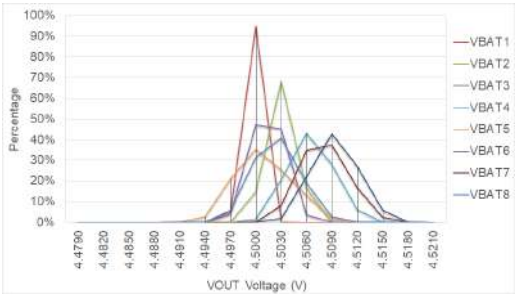


Cell voltage from 1 to 8:
2.5V, 4.5V, 2.5V, 4.5V, 2.5V, 4.5V, 2.5V, 4.5V



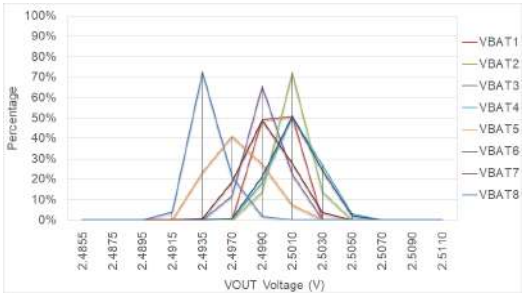
Cell voltage from 1 to 8: all equal to 4.2V

V_{OUT} Scanning Waveform (Scan from Cell 1 to Cell 8 and repeat)



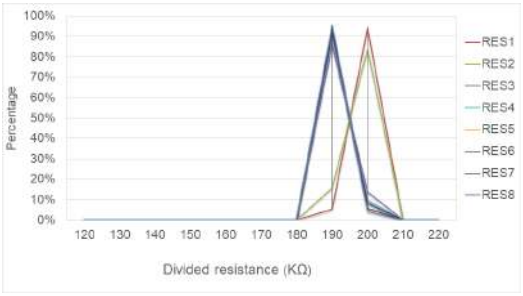
$VOUT_{MIN}$=4.479V, $VOUT_{MAX}$=4.521V

Wafer Level V_{OUT} Voltage Statistics Distribution (V_{Bi}=4.5V)



$VOUT_{MIN}$=2.4855V, $VOUT_{MAX}$=2.5110V

Wafer Level V_{OUT} Voltage Statistics Distribution (V_{Bi}=2.5V)



R_{MIN}=120kΩ, R_{MAX}=220kΩ

Wafer Level Divided Resistance Statistics Distribution

Functional Description

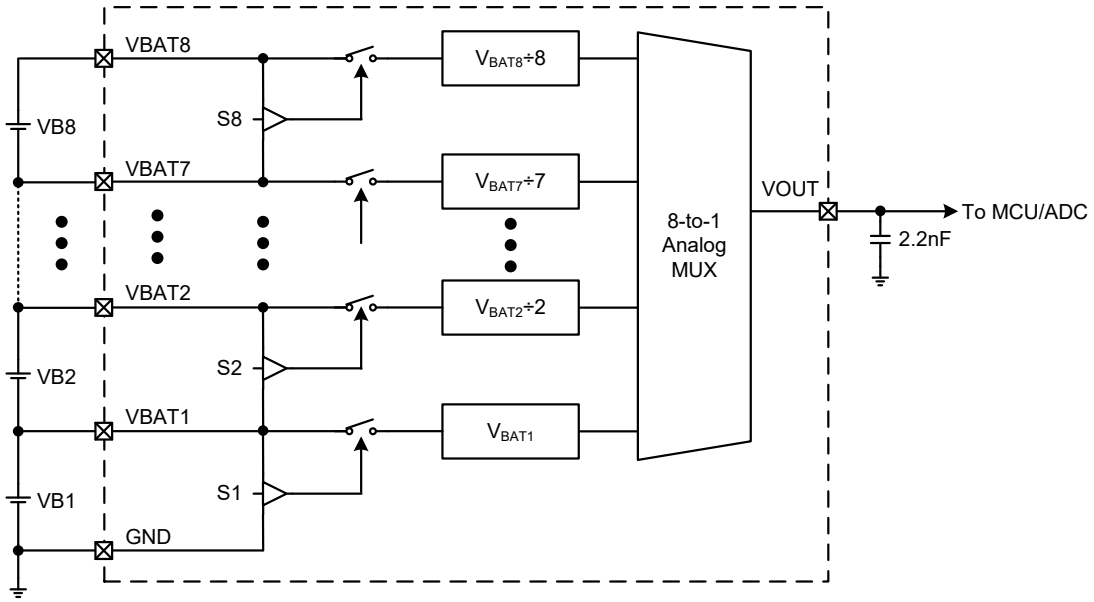
Accumulative Cell Voltage Monitor

The accumulative cell voltage monitor consists of high voltage switches, voltage dividers and an 8-to-1 analog multiplexer as shown in the following diagram. The high voltage switches are implemented using an anti-reverse current topology which provides isolation between the output voltage and the unselected VBATn.

B2, B1 and B0 are used to control the p-type switches S1~S8 only if EN_S="1". The control truth table is shown below. This produces an accumulative cell voltage, VBATn, divided by "n" on VOUT. This accurate ±0.5% voltage divided ratio is designed to minimize any mismatch errors.

EN_S	B2	B1	B0	S8	S7	S6	S5	S4	S3	S2	S1	V_{OUT} (V)
0	X	X	X	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1	V_{BAT1}×1/1
1	0	0	1	0	0	0	0	0	0	1	0	V_{BAT2}×1/2
1	0	1	0	0	0	0	0	0	1	0	0	V_{BAT3}×1/3
1	0	1	1	0	0	0	0	1	0	0	0	V_{BAT4}×1/4
1	1	0	0	0	0	0	1	0	0	0	0	V_{BAT5}×1/5
1	1	0	1	0	0	1	0	0	0	0	0	V_{BAT6}×1/6
1	1	1	0	0	1	0	0	0	0	0	0	V_{BAT7}×1/7
1	1	1	1	1	0	0	0	0	0	0	0	V_{BAT8}×1/8
Power on states				0	0	0	0	0	0	0	0	0

Accumulative Cell Voltage Monitor Truth Table



Accumulative Cell Voltage Monitor Functional Block

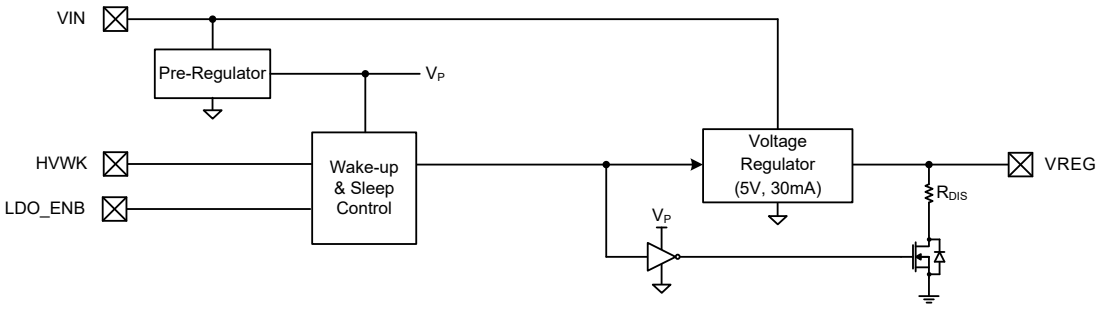
Sleep Mode

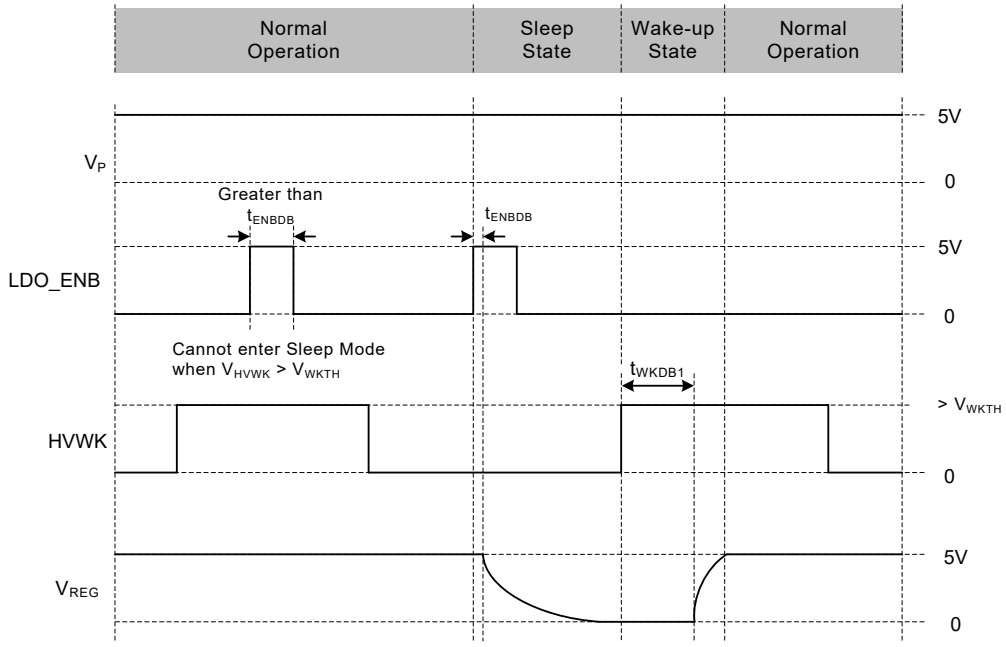
When a voltage of 5V and duration of more than 1.8μs signal is applied on LDO_ENB pin, the chip enters Sleep Mode. During Sleep Mode, VREG and VOUT are shut down to 0V and the capacitor of VREG is discharged through internal discharge resistor. Pre-regulator and high voltage wake-up circuit are the only blocks that are still working in Sleep Mode and operates with an ultra-low standby current of 0.1μA (typical).

When the voltage applied on HVWK pin is greater than V_{WKTH} (typical value is 4.0V), the chip cannot enter Sleep Mode, even though the voltage of LDO_ENB pin is 5V.

Wake up from Sleep Mode

The HVWK pin can be used for detecting charger plugged-in, switch turned on, or load connected events. When the device is under the Sleep Mode, if the HVWK pin is triggered by a pulse with requiring at least 4.0V voltage and 1ms width, the output of VREG will resume and the whole chip is ready for normal operation. The reference timing diagram of entering the Sleep Mode and waked up is listed below.





Application Information

VIN, VREG, VOUT Capacitors

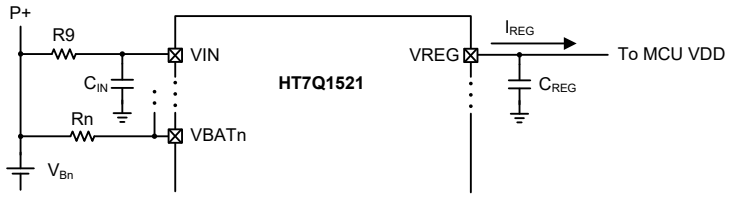
The VIN input capacitor C_{IN} and VREG output capacitor C_{REG} are 4.7μF for better input noise filtering and output load transient behavior. A recommended 2.2nF noise filtering capacitor should be connected between VOUT and GND terminals. Note that higher noise capacitance value of C_{OUT} will lower the acceptable scan frequency.

VIN and VBATn Spike Suppression Resistors

The appropriate VIN and VBATn spike suppression resistors corresponded to R9 and Rn lower the voltage spike and inrush current applied on any I/O pins, which can improve the stability of V_{REG} that provides the power source to the external MCUs. Especially when there are spike filter capacitors connected from P+ or C+ to GND, the VBATn spike suppression resistors (Rn) are necessary. The recommended resistance values of VIN and VBATn resistor varies with the number of battery cells, which are listed in the following table.

Battery Cell Number	VIN Recommended Resistor (R9)	VBATn Recommended Resistor (Rn)
3S	18Ω	100Ω
4S	100Ω	51Ω
5S	180Ω	51Ω
6S	270Ω	51Ω
7S	360Ω	51Ω
8S	430Ω	51Ω

Recommended Resistance of Spike Suppression Resistors



It is necessary to select an appropriate package for VIN spike suppression resistor (R9) in order to prevent it being damaged from overheated. The maximum power on R9 is easily calculated by:

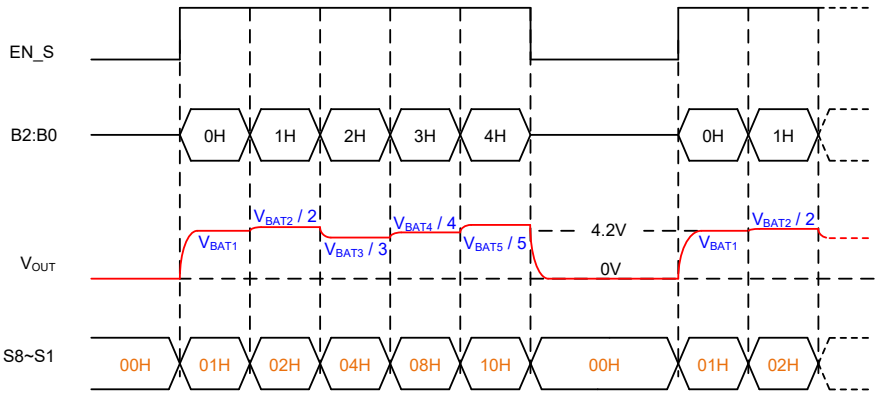
$$P_{R9.MAX}=(I_{REG})^2\times R9$$

where I_{REG} is the maximum VREG output current, R9 is the resistance value of VIN spike suppression resistor (R9).

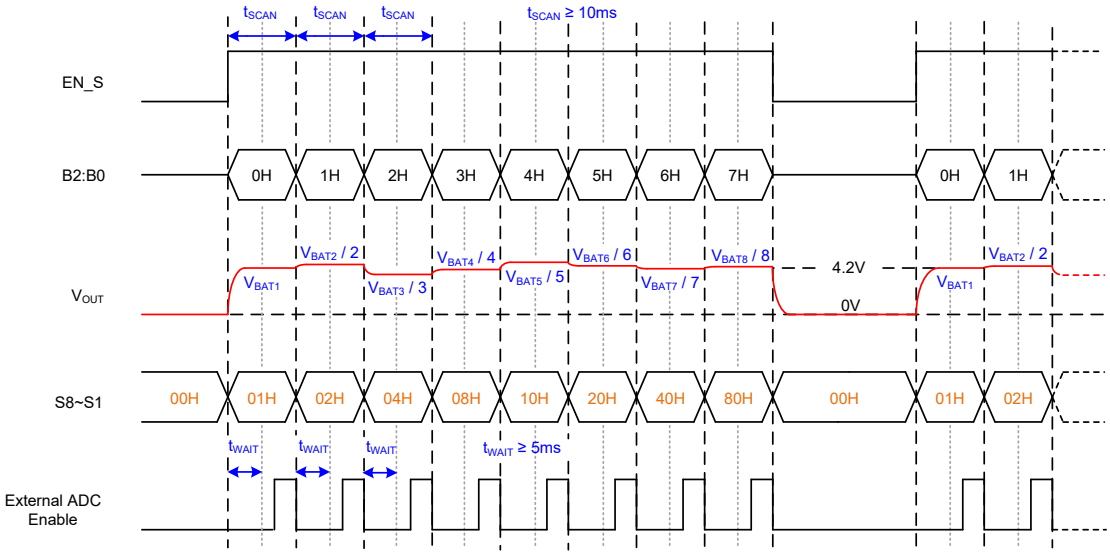
It is recommended to choose the resistor package that its maximum rated power is greater than twice the $P_{R9.MAX}$.

Cell Voltage Monitor Scan Frequency

The HT7Q1521 can output accumulative cell voltage to external MCU ADC for monitoring battery voltage status. The following figures show the timing diagrams of cell voltage monitor scanning for 5S and 8S applications. The HT7Q1521 starts to charge the VOUT capacitor from 0V to the selected cell voltage while the EN_S receives an 'L' to 'H' signal. In order to ensure external MCU A/D conversion accuracy, the A/D conversion procedure has to wait before the HT7Q1521 VOUT capacitor is fully charged. The suggested minimum waiting time is 5ms after the EN_S from 'L' to 'H' or cell voltage monitor channel switched. It is recommended that the maximum scan frequency for accumulative cell voltage monitoring is less than 100Hz and that EN_S="0" when the voltage scanning procedure has finished for power saving purposes.



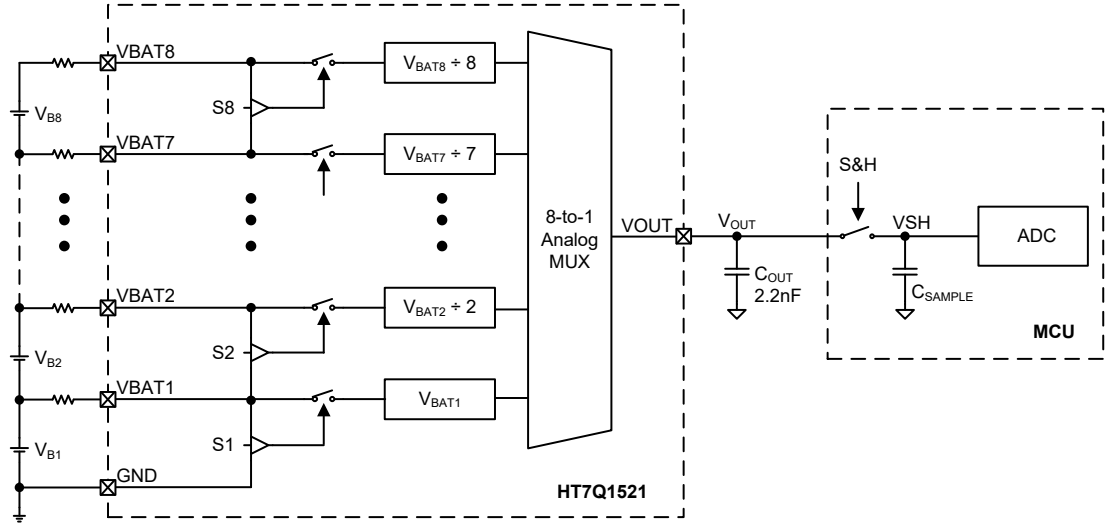
5S Battery Monitoring Timing



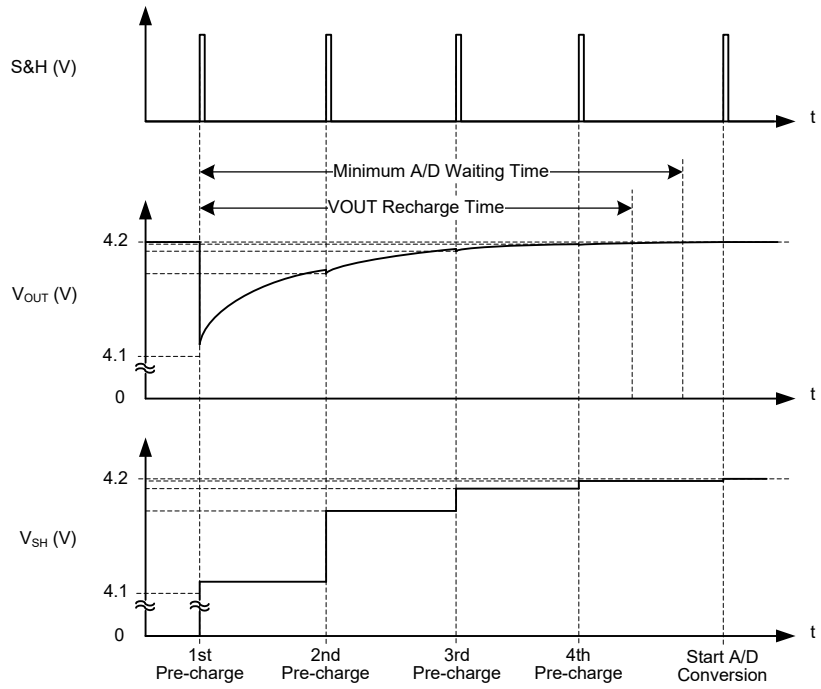
8S Battery Monitoring Timing

Acquiring Cell Voltage Monitor Output with External MCU ADC

The HT7Q1521 can output battery cell voltage to an external MCU for monitoring the battery voltage status when it is in charging or discharging state. As shown in the following figure, the external MCU ADC samples the V_{OUT} voltage via an ADC sampling capacitor (C_{SAMPLE}), which is typically 5pF to 50pF. Due to the charge sharing effect, the voltage on the VOUT capacitor (C_{OUT}) drops while the ADC samples that with initially zero-voltage C_{SAMPLE}. A voltage-drop occurs on the C_{OUT} after the first ADC sampling, and then it needs a recharge time to recharge the C_{OUT}. Referring to the following timing figure, a pre-charge procedure of C_{SAMPLE} during the VOUT recharge time is recommended to minimize the charge sharing effect by the means of performing several sampling without clearing the charges in the C_{SAMPLE}.



HT7Q1521 + MCU ADC Functional Block



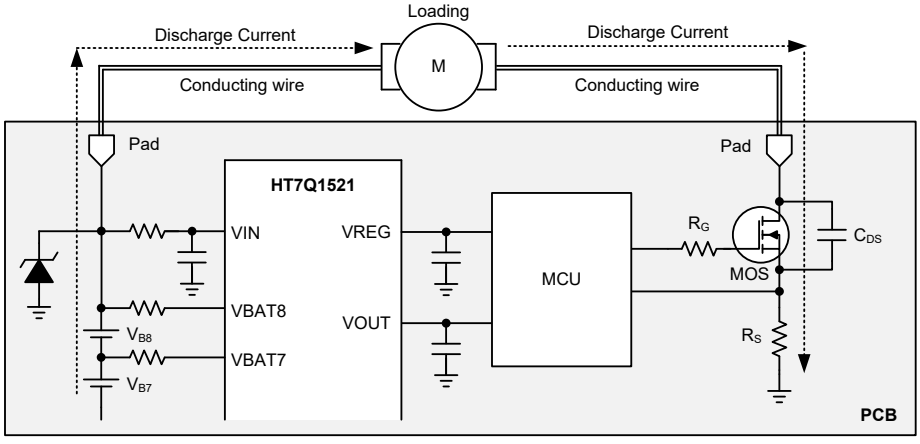
ADC Sampling Recommended Timing

For the best conversion accuracy, the A/D conversion has to wait before C_{OUT} recharge is complete. The recommended minimum waiting time from the first sampling to A/D conversion beginning is listed in the following table.

MCU ADC Sampling Capacitance (pF)	Recommended Minimum A/D Waiting Time (μs)
5	370
10	660
20	950
30	1120
40	1240
50	1340

ADC Sampling Recommended Waiting Time

Voltage Spike Suppression Method



Simplified Typical BMS System Discharge Path Diagram

Most battery-management systems would monitor charge and discharge current to prevent over-current damage. Due to the parasitic inductance on conducting wires and PCB layout connections, large voltage spike may occurs while the MCU controlled MOS rapidly shuts down the charge or discharge current, and this spike may damage the device VBATn or VIN pins. Any voltage spike on the VBATn and VIN pins should not over the limitation in Absolute Maximum Ratings, which is 48V. Four recommended measures listed below would help to reduce the voltage spike.

1. Make the external conducting wire and PCB layout connections as short as possible where large charge or discharge current flows.
2. Adjust the slew rate of MOS switch with the gate resistor R_G. Turn off the MOS with slower slew rate for lower voltage spike, and the tradeoff is a slower protection response time.
3. Add a capacitor (C_{DS}) between drain and source node of the MOS switch as shown above. The recommended capacitance is 0.1μF to 0.22μF.
4. Add a 39V Zener diode between the highest voltage potential node of battery cells and GND.

PCB Layout Considerations

The following component placement and layout guidelines are suggested for the sake of noise reduction and voltage spike suppression.

1. The VIN filter capacitor and resistor must be close to VIN pin. [Region (A)]
2. The VREG regulation and noise filter capacitor must be close to VREG pin. [Region (B)]
3. The VOUT noise filter capacitor must be close to VOUT pin. [Region (C)]
4. Placing a ground line between VIN and VREG lines would improve the ability of resisting surge.
5. The tracks where large current would flow through should be wide and short to suppress the voltage spike at the time when MOS switch change its ON/OFF state.
6. The power ground and signal ground should be connected at final output pad (B-) for less noise disturbance.

Thermal Considerations

The maximum power dissipation depends upon the thermal resistance of the IC package, PCB layout, rate of surrounding airflow and difference between the junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)}\text{-}Ta)/\theta_{JA}\ (W)$$

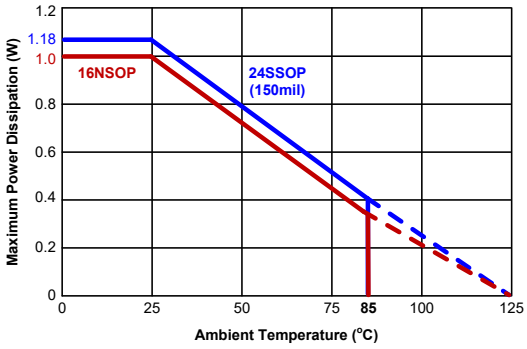
where $T_{J(MAX)}$ is the maximum junction temperature, Ta is the ambient temperature and θ_{JA} is the junction-to-ambient thermal resistance of IC package.

For maximum operating rating conditions, the maximum junction temperature is 125°C. However, it is recommended that the maximum junction temperature does not exceed 125°C during normal operation to maintain high reliability. The de-rating curve of the maximum power dissipation is show below:

$P_{D(MAX)}$ = (125°C-25°C)/(100°C/W) = 1.0W (16NSOP)

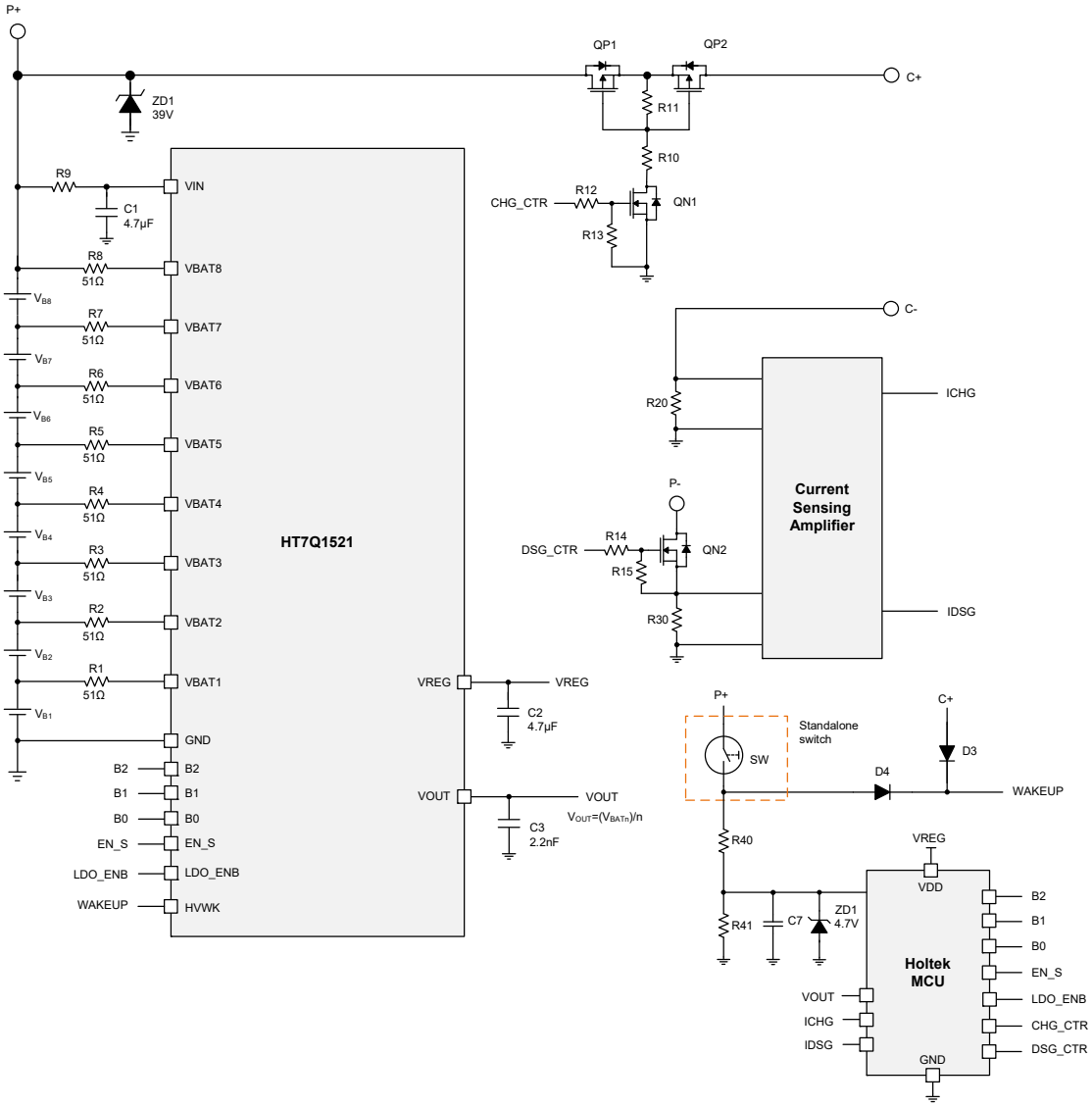
$P_{D(MAX)}$ = (125°C-25°C)/(85°C/W) = 1.18W (24SSOP)

For a fixed $T_{J(MAX)}$ of 125°C, the maximum power dissipation depends upon the operating ambient temperature and the package's thermal resistance, θ_{JA}. The de-rating curve below shows the effect of rising ambient temperature on the maximum recommended power dissipation.

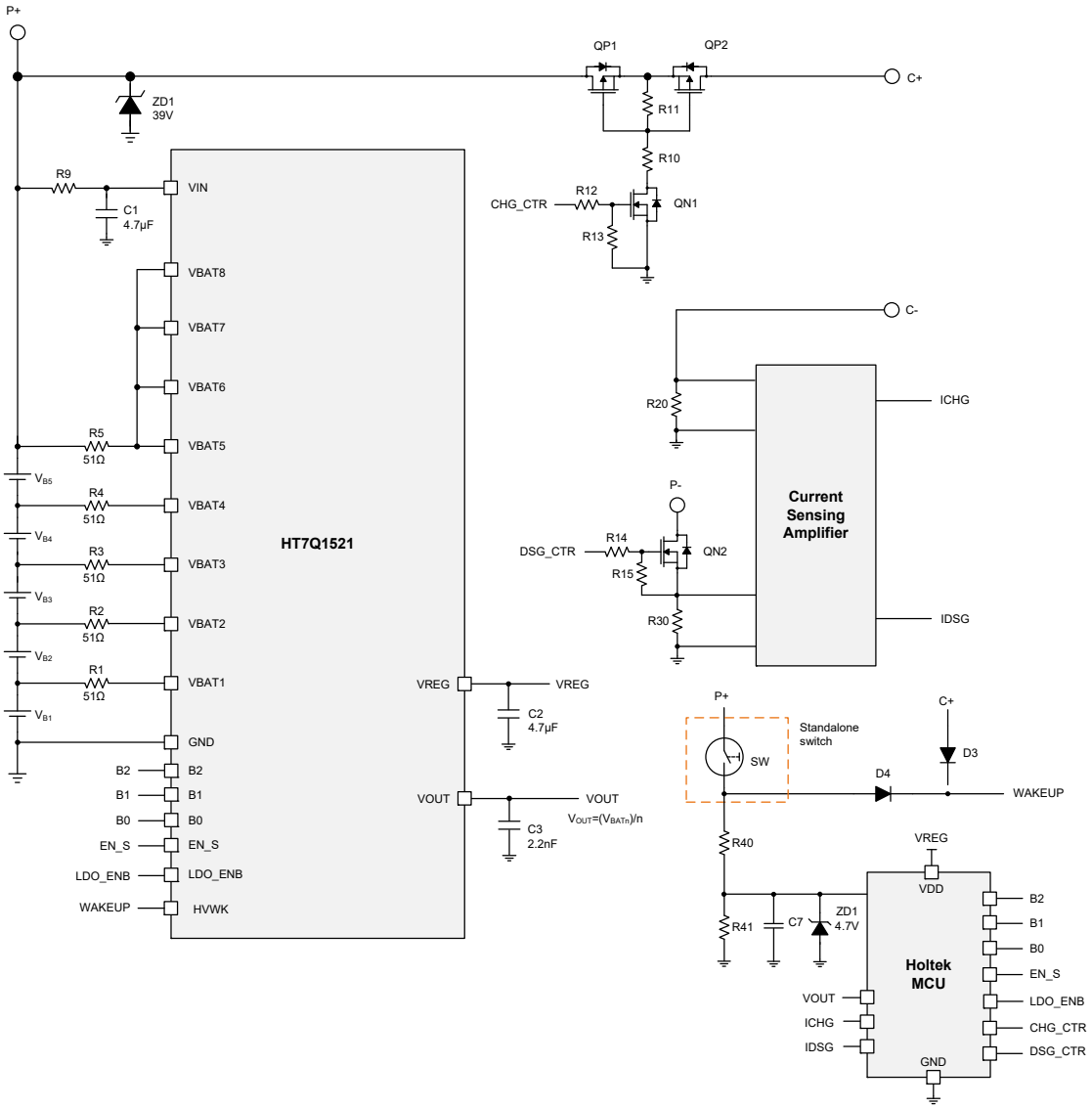


Typical Application Circuits

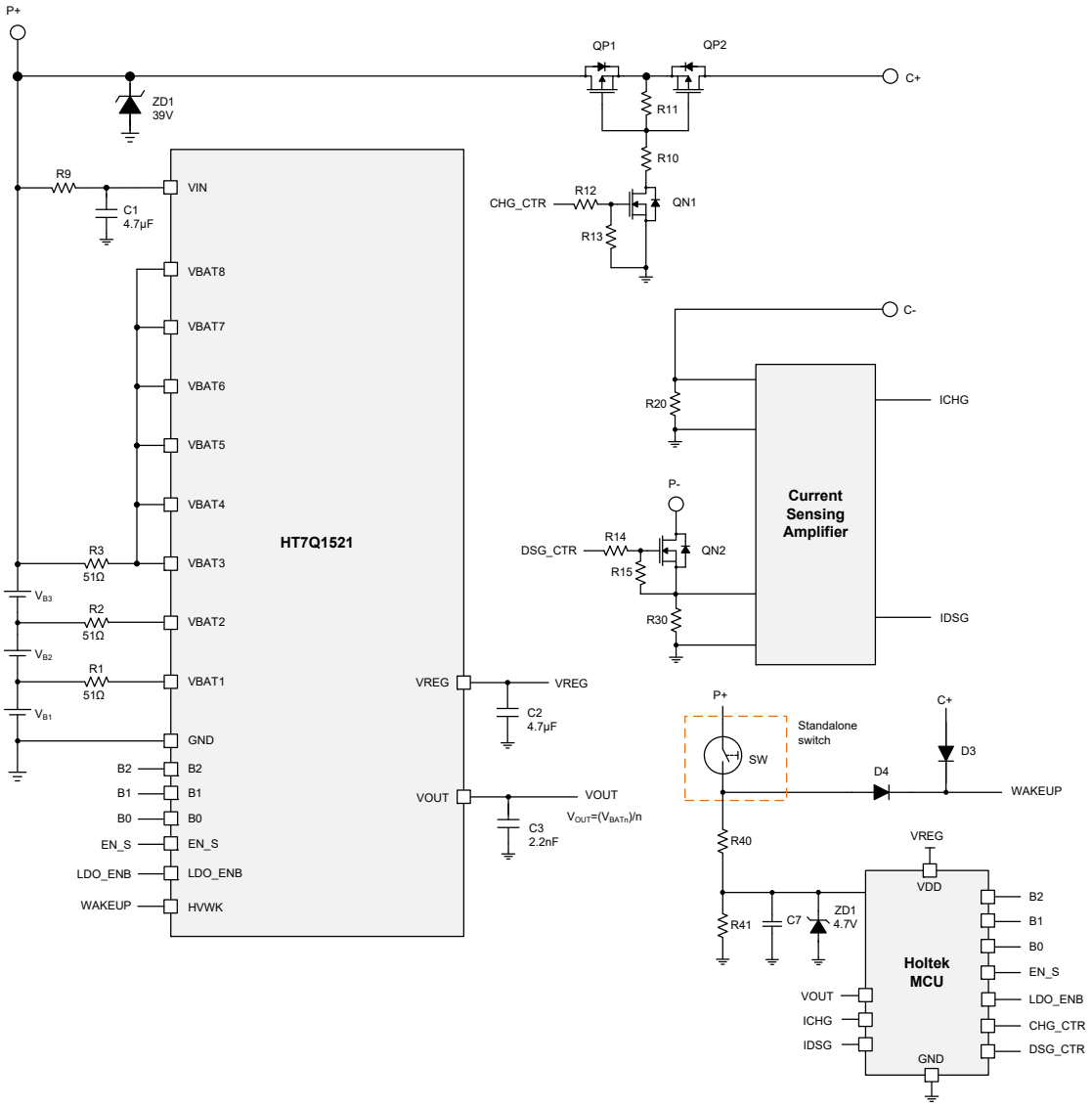
8S Battery Monitoring Typical Application Circuit



5S Battery Monitoring Typical Application Circuit



3S Battery Monitoring Typical Application Circuit



Note: 1. If less than 8 serial batteries are used, connect the unused VBATn to the highest voltage potential. Do not leave any VBATn floating in order to prevent damage to the device.

2. The resistance selection of R9, R1, R2, and R3 are listed in section “VIN and VBATn Spike Suppression Resistors”.

3.VIN pin should not be floating to prevent abnormal operations.

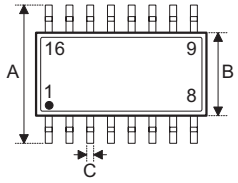
Package Information

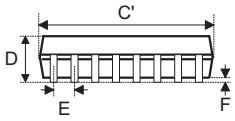
Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

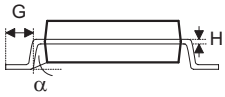
Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

16-pin NSOP (150mil) Outline Dimensions



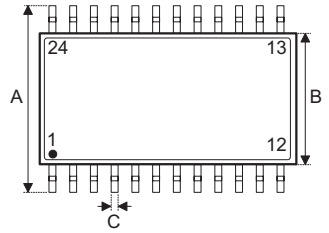


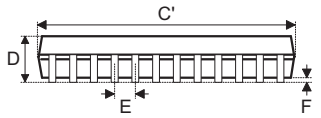


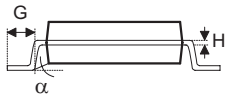
Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.012	—	0.020
C'	—	0.390 BSC	—
D	—	—	0.069
E	—	0.050 BSC	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.000 BSC	—
B	—	3.900 BSC	—
C	0.31	—	0.51
C'	—	9.900 BSC	—
D	—	—	1.75
E	—	1.270 BSC	—
F	0.10	—	0.25
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°

24-pin SSOP (150mil) Outline Dimensions







Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.008	—	0.012
C'	—	0.341 BSC	—
D	—	—	0.069
E	—	0.025 BSC	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.00 BSC	—
B	—	3.90 BSC	—
C	0.20	—	0.30
C'	—	8.66 BSC	—
D	—	—	1.75
E	—	0.635 BSC	—
F	0.10	—	0.25
G	0.41	—	1.27
H	0.10	—	0.25
α	0°	—	8°