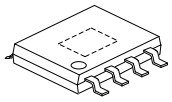
L1806 **CMOS IC**

3A, ULTRA LOW DROPOUT (0.23V@3A) LINEAR REGULATOR



HSOP-8

DFN3030-10

■ DESCRIPTION

The UTC **L1806** is a typical LDO with the features of very low dropout voltage as low as 0.23V at output current 3A.

For normal operation, two supply voltages are necessary. One called control voltage from other equipment can shutdown the output voltage and it should pull and hold the voltage of EN pin less than 0.5V. Another one is the main supply voltage whose purpose is for main power conversion, to keep the power dissipation low, and to make the dropout voltage lower.

Internally, in the UTC **L1806**, there're many functions which can be seen in the block figure to prevent the IC from being damaged. Internal Power-On-Reset (POR) circuit can control the two supply voltages to prevent fault operations of the circuit; the thermal shutdown circuit is able to protect the device from over thermal operation, and a current limit function will keep the device work safely under current over-loads.

The UTC **L1806** can be used as an ideal to provide well supply voltage in the applications, such as front-side-bus termination on motherboard, NB applications, front side bus V_{TT} (1.2V/3A) and note book PC applications.

■ FEATURES

* Low Dropout V_D=0.23V(typ.)@ I_{OUT}=3A
* Low ESR Output Capacitor
* V_{REF}=0.8V
* Fast Transient Response
* Output Voltage Adjustable through External Resistors
* POR(Power-On-Reset) controlling V_{CNTL} and V_{IN}
* With internal Soft-Start
* Internal Current Limit Protection
* Internal Under Voltage Protection
* Hysteretic Thermal Shutdown
* With Power-OK Output (with a Delay Time)
* Low Shutdown Quiescent Current (<30 uA)
* Shutdown/Enable Control Function

■ ORDERING INFORMATION

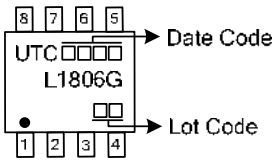
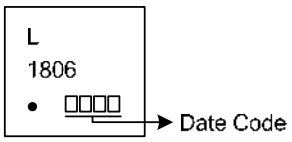
Ordering Number		Package	Packing
Lead Free	Halogen Free		
L1806L-SH2-R	L1806G-SH2-R	HSOP-8	Tape Reel
L1806L-K10-3030-R	L1806G-K10-3030-R	DFN3030-10	Tape Reel

L1806G-SH2-R

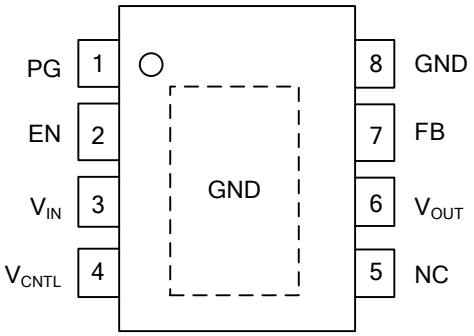
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) SH2: HSOP-8, K10-3030: DFN3030-10
(3) G: Halogen Free and Lead Free, L: Lead Free

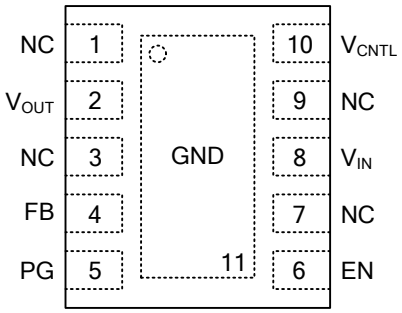
■ MARKING

HSOP-8	DFN3030-10
	

■ PIN CONFIGURATION



HSOP-8

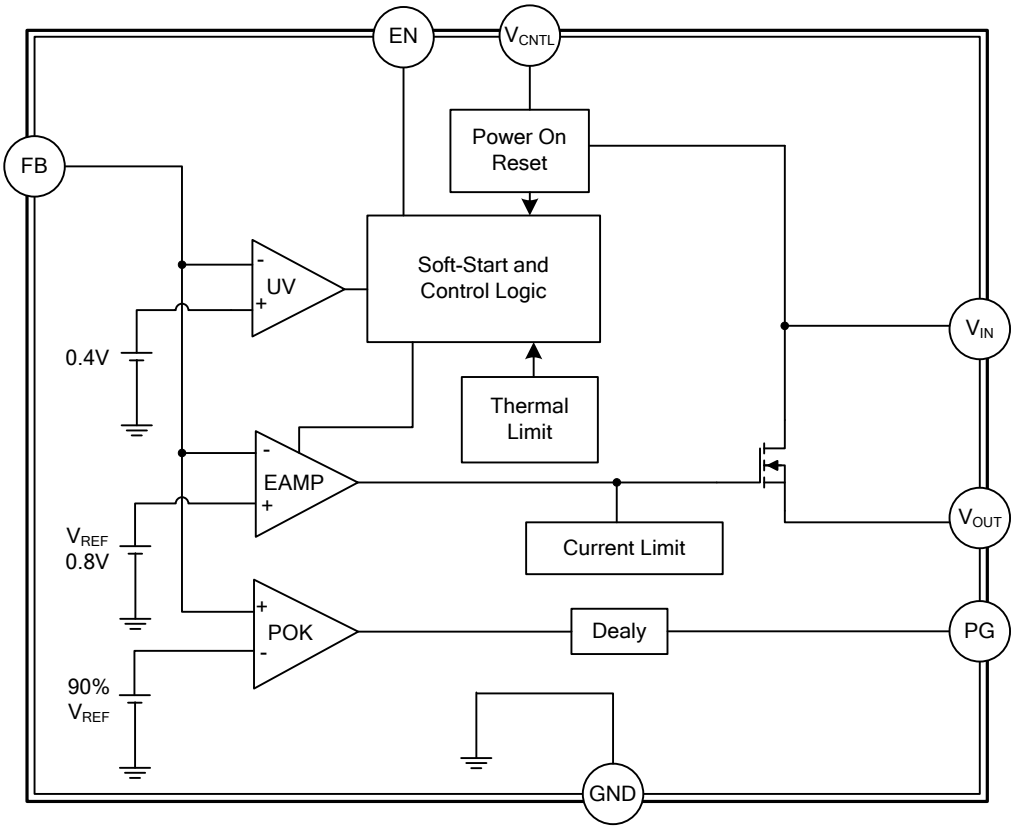


Top View
DFN3030-10

■ PIN DESCRIPTION

PIN NO.		PIN NAME	DESCRIPTION
HSOP-8	DFN3030-10		
1	5	PG	Power Good.Output open drain to indicate the status of V_{OUT} via monitoring the FB pin. This pin is pulled low when the voltage is outside the limits, during thermal shutdown and if either V_{CNTL} or V_{IN} go below their thresholds.
2	6	EN	Enable Pin. Driving this pin low will disable the part. When left floating an internal current source will pull this pin high and enable it.
3	8	V_{IN}	Power Input Pin for current supply. Connect a decoupling capacitor (≥10μF) as close as possible to the pin for noise filtering
4	10	V_{CNTL}	BIAS supply for the controller, recommended 5V. Connect a decoupling capacitor (≥1μF) as close as possible to the pin for noise filtering.
5	1, 3, 7,9	NC	No Connection
6	2	V_{OUT}	Power output pin
7	4	FB	Feedback to set the output voltage via an external resistor divider between V_{OUT} and GND
8	11	GND	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (V_{CNTL} to GND)	V_{CNTL}	-0.3 ~ +7	V
Supply Voltage (V_{IN} to GND)	V_{IN}	-0.3 ~ + 4.0	V
EN and FB to GND	$V_{I/O}$	-0.3 ~ V_{CNTL}+0.3	V
PG to GND	V_{PG}	-0.3 ~ +7	V
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage	Control	V_{CNTL}	3~ 5.5	V
Supply Voltage	Input	V_{IN}	1.2~ 3.65	V
Output Voltage	V_{CNTL}=3.3±5%	V_{OUT}	0.8 ~ 1.2	V
	V_{CNTL}=5.0±5%		+0.8 ~ V_{IN}-0.2	V
Output Current		I_{OUT}	0 ~ 4	A

■ THERMAL RESISTANCES CHARACTERISTICS

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	HSOP-8	θ_{JA}	90 (Note 1)	°C/W
	DFN3030-10		72 (Note 2)	°C/W

Notes: 1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of HSOP-8 is soldered directly on the PCB.
2. The PCB area is 4 times larger than that of IC's

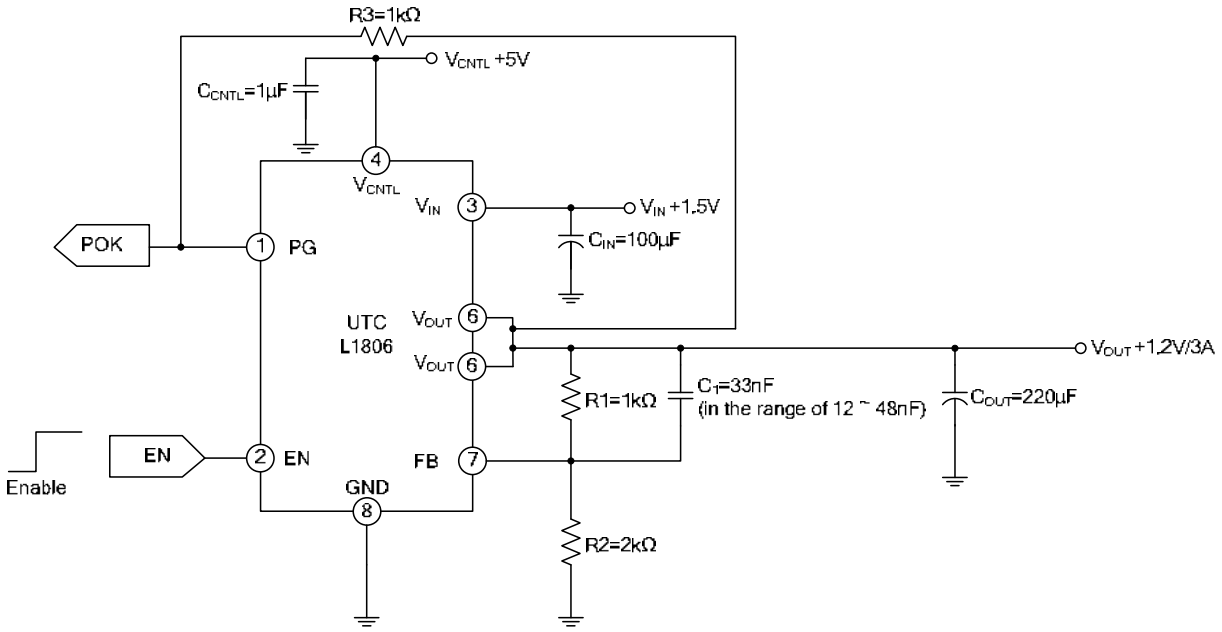
■ ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_{CNTL} = 5V, V_{IN} = 1.5V, V_{OUT} = 1.2V, unless otherwise specified)

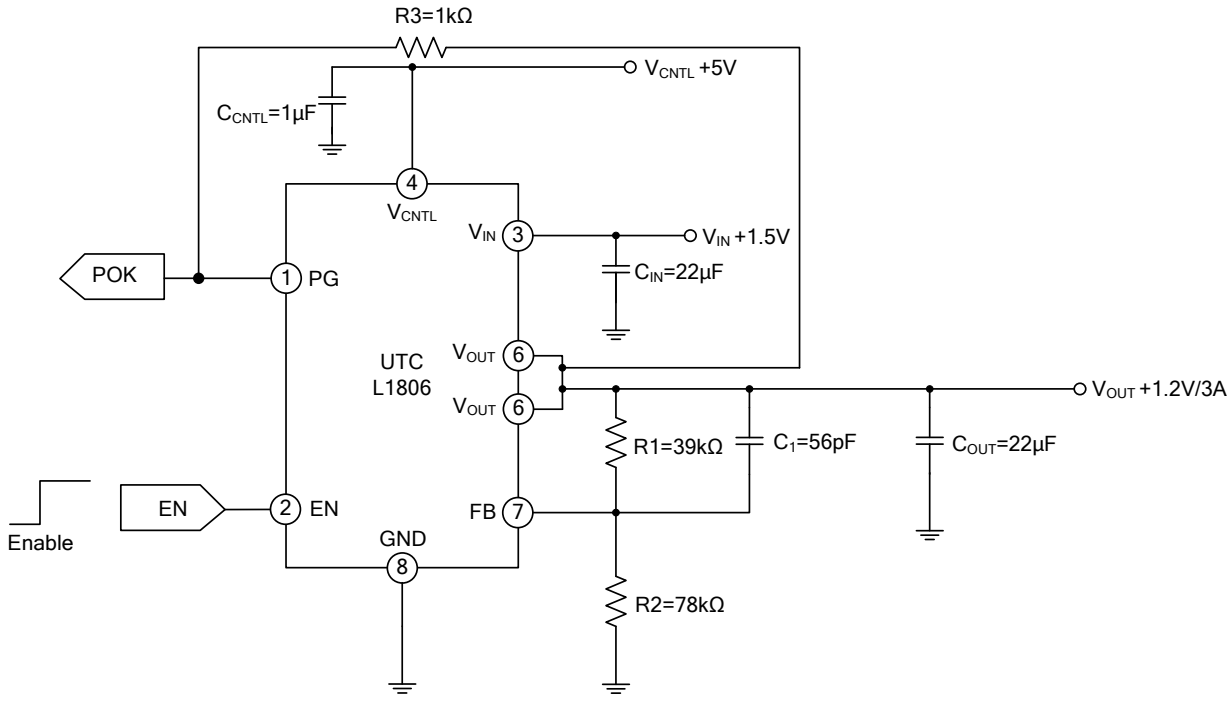
PARAMETER		SYMBOL	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{CNTL} Nominal Supply Current		I_{CNTL}	EN = V_{CNTL}				1	1.5	mA
V_{CNTL} Shutdown Current		I_{SD}	EN = GND				15	30	μA
PG Threshold	V_{CNTL}	V_{THR}	V_{CNTL} Rising			2.5	2.7	2.9	V
	V_{IN}		V_{IN} Rising			0.8	0.9	1.0	V
PG Hysteresis	V_{CNTL}	V_{HYS}					0.4		V
	V_{IN}						0.5		V
Reference Voltage		V_{REF}	FB =V_{OUT}				0.8		V
Output Voltage Accuracy			I_{OUT}=0A~3A, T_J= -25 ~125°C			-1.5		+1.5	%
Line Regulation		$\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$	I_{OUT}=10mA,V_{CNTL}=3~5V			-0.15		+0.15	%/V
Load Regulation		$\frac{\Delta V_{OUT}}{V_{OUT}}$	I_{OUT}=0A~3A				0.06	0.25	%
Current Limit		I_{LIMIT}	V_{CNTL}=5V, T_J= 25°C			4	5.7	7	A
Dropout Voltage		V_D	V_{CNTL}=5V I_{OUT}=3A	V_{OUT}=2.5V	T_J= 25°C		0.26	0.31	V
				V_{OUT}=1.8V	T_J= 25°C		0.24	0.29	
				V_{OUT}=1.2V	T_J= 25°C		0.23	0.28	
Over Temperature Shutdown		OTS	T_J Rising				150		°C
Over Temperature Hysteresis		OTH					30		°C
Under-Voltage Threshold			V_{FB} Falling				0.4		V
EN Logic High Threshold Voltage			V_{EN} Rising			0.5	0.8	1.1	V
EN Hysteresis							100		mV
EN Pin Pull-Up Current			EN=GND				5		μA
PG Threshold Voltage for Power OK		V_{PG}	V_{FB} Rising			90%	92%	94%	V_{REF}
PG Threshold Voltage for Power Not OK		V_{PNOK}	V_{FB} Falling				81%		V_{REF}
PG Low Voltage			PG sinks 5mA				0.25	0.4	V

■ TYPICAL APPLICATION CIRCUIT

1. Using an Output Capacitor with ESR≥18mΩ



2. Using an MLCC as the Output Capacitor



V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C1 (pF)
1.05	43	137.6	47
1.5	27	30.86	82
1.8	15	12	150

■ APPLICATION INFORMATION

1. Power Sequencing

When there's no main voltage applied at V_{IN}, it is suggested not to apply a voltage to V_{OUT} for a long time. Because the internal parasitic diode (between V_{OUT} to V_{IN}) will conduct and dissipate power, there's no protection.

2. Output Capacitor

A proper output capacitor to maintain stability and improve transient response over temperature and current is necessary. Proper ESR (equivalent series resistance) and capacitance of the output capacitor should be selected properly for stability of the normal operation and good load transient response.

Many kinds of capacitors can be used as an output capacitor, such as ultra-low-ESR capacitors (like ceramic chip capacitors), low-ESR bulk capacitors (like solid Tantalum, POSCap, and Aluminum electrolytic capacitors). And also the value of the output capacitors' can be increased without limit.

In the applications with large stepping load current, the low-ESR bulk capacitors are normally recommended.

Decoupling ceramic capacitors are recommended to be placed at the load and ground pins very closely and also the impedance of the layout must be minimized.

3. Input Capacitor

In order to prevent the input rail from dropping, the proper input capacitor to supply current surge during stepping load transients is required. Because the limited slew rate of the surge currents, more parasitic inductance needs more input capacitance.

Ultra-low-ESR capacitors (>100mF, ESR<300mW) is recommended for the input capacitor.

4. Feedback Network

The following figure shows the feedback network between V_{OUT} GND and FB pins. Working with the internal error amplifier, the feedback network can provide proper frequency response for the UTC **L1806**.