HT32F50343
Datasheet

32-Bit Arm® Cortex®-M0+ 5V USB Microcontroller, 64 KB Flash and 12 KB SRAM with 1 MSPS ADC, USB, PDMA, DIV, UART, SPI, I²C, GPTM, PWM, SCTM, BFTM, SLED, CRC, RTC and WDT

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1 General Description

The Holtek HT32F50343 device is a high performance, low power consumption 32-bit microcontroller based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The device operates at a frequency of up to 60 MHz with a Flash accelerator to obtain maximum efficiency. It provides 64 KB of embedded Flash memory for code/data storage and 12 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as Hardware Divider DIV, PDMA, ADC, I^2C, UART, SPI, SLED, GPTM, PWM, SCTM, BFTM, CRC-16/32, RTC, WDT, USB2.0, SW-DP (Serial Wire Debug Port), etc., are also implemented in the device. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the device is suitable for use in a wide range of applications, especially in areas such as gaming application controllers, keyboards and mice, consumer products, handheld equipment, LED lighting applications and so on.

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 60 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O ports, hardware multiplier and low latency interrupt respond time.

On-chip Memory

- 64 KB on-chip Flash memory for instruction/data and options storage
- 12 KB on-chip SRAM
- Supports multiple boot modes

The Arm® Cortex®-M0+ processor accesses and debug accesses share the single external interface to external AHB peripherals. The processor accesses take priority over debug accesses. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the HT32F50343 device, including code, SRAM, peripheral and other pre-defined regions.

Flash Memory Controller – FMC

- 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions for the embedded on-chip Flash Memory. The word programming/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor:
  - Power On Reset / Power Down Reset – POR / PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by external signals, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- External 32.768 kHz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to ±2 % accuracy at 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control Unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), an HSE clock monitor, clock pre-scalers, clock multiplexers, APB clock divider and gating circuitry. The AHB, APB and Cortex®-M0+ clocks are derived from the system clock (CK_SYS) which can come from the HSI, HSE, LSI or LSE. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source.

Power Management Control Unit – PWRCU

- Flexible power supply: V_{DD} power supply (2.5 V ~ 5.5 V), V_{DDIO} for I/Os (1.8 V ~ 5.5 V)
- Integrated 1.5 V LDO regulator for CPU core, peripherals and memories power supply
- Three power domains: V_{DD}, V_{DDIO} and 1.5 V
- Three power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in the device provides many types of power saving modes such as Sleep, Deep-Sleep1 and Deep-Sleep2 mode. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

Real Time Clock – RTC

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real Time Clock, RTC, circuitry includes the APB interface, a 24-bit up-counter, a control register, a prescaler, a compare register and a status register. The RTC circuits are located in the V_{DD15} power domain. The RTC counter is used as a wakeup timer to generate a system resume or interrupt signal from the MCU power saving mode.

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 12 external analog input channels

A 12-bit multi-channel Analog to Digital Converter is integrated in the device. There are multiplexed channels, which include 12 external channels on which the external analog signal can be supplied and 1 internal channels. If the input voltage is required to remain within a specific threshold window, the Analog Watchdog function will monitor and detect the signals. An interrupt will then be generated to inform the device that the input voltage is higher or lower than the preset thresholds. There are three conversion modes to convert an analog signal to digital data. The A/D conversion can be operated in one shot, continuous and discontinuous conversion mode.

I/O Ports – GPIO

- Up to 51 GPIOs
- Port A, B, C, D are mapped as 16 external interrupts – EXTI
- Almost all I/O pins have configurable output driving current

There are up to 51 General Purpose I/O pins, GPIO, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC6, PC10 ~ PC15 and PD0 ~ PD5 for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

General-Purpose Timer – GPTM

- 16-bit up/down auto-reload counter
- Up to 4 independent channels for each timer
- 16-bit programmable prescaler that allows division of the counter clock frequency by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General-Purpose Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

Pulse-Width-Modulation Timer – PWM

- 16-bit up/down auto-reload counter
- Up to 8 independent channels for each timer
- 16-bit programmable prescaler that allows division of the counter clock frequency by any factor between 1 and 65536
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned counting Modes
- Single Pulse Mode Output

The Pulse-Width-Modulation Timer consists of one 16-bit up/down-counter, four 16-bit Compare Registers (CRs), one 16-bit Counter-Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer and output waveform generation such as single pulse generation or PWM output.

Single Channel Timer – SCTM

- 16-bit auto-reload up-counter
- One channel for each timer
- 16-bit programmable prescaler that allows division of the counter clock frequency by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned counting Mode
- Single Pulse Mode Output

The Single Channel Timer consists of one 16-bit up-counter, one 16-bit Capture/Compare Register (CCR), one 16-bit Counter Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as single pulse generation or PWM outputs.

Basic Function Timer – BFTM

- 32-bit compare match up-counter – no I/O control
- One shot mode – counter stops counting when compare match occurs
- Repetitive mode – counter restarts when compare match occurs

The Basic Function Timer is a simple 32-bit up-counting counter designed to measure time intervals and generate one shots or generate repetitive interrupts. The BFTM can operate in two functional modes, repetitive and one shot modes. In the repetitive mode, the counter will restart at each compare match event. The BFTM also supports a one shot mode which will force the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-bit down-counter with 3-bit prescaler
- Provides reset to the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect a system lock-up due to software trapped in a deadlock. It includes a 12-bit down-counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter before it reaches a delta value. It means that the counter reload must occur when the Watchdog timer value has a value within a limited window using a specific method. The Watchdog Timer counter can be stopped when the processor is in the debug mode. The register write protection function can be enabled to prevent an unexpected change in the Watchdog Timer configuration.

Inter-integrated Circuit – I²C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode using address mask function

The I²C module is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I²C bus is a bidirectional data line between the master and slave devices and is used for data transmission and reception. The I²C also has an arbitration detect function and clock synchronization function to prevent the situations where more than one master attempts to transmit data to the I²C bus at the same time.

Serial Peripheral Interface– SPI

- Supports both master and slave modes
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, among which are serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamlined data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to (f_{PCLK}/16) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and

serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Serial LED Interface – SLED

- 4 output channels with output enable and polarity control
- 4 × 32-bit FIFO with trigger level selection
- Configurable transfer speed and frame reset length
- Configurable T0H and T1H duty cycle

The SLED is an individually addressable RGB LED strip controller which can control four LED strips synchronously, simply converting the RGB data for hundreds of LEDs on per strip into T0 and T1 code outputs.

Cyclic Redundancy Check – CRC

- Support CRC16 polynomial: 0x8005,
  $X^{16} + X^{15} + X^2 + 1$
- Support CCITT CRC16 polynomial: 0x1021,
  $X^{16} + X^{12} + X^5 + 1$
- Support IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
  $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data

The CRC calculation unit is an error detection technique test algorithm and is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means the data stream contains a data error.

Peripheral Direct Memory Access – PDMA

- 6 channels with trigger source grouping
- 8-bit, 16-bit and 32-bit width data transfer
- Supports linear address, circular address and fixed address modes
- 4-level programmable channel priority
- Auto reload mode

- Supports trigger source:
  ADC, SPI, UART, I²C, GPTM, PWM, SLED and software request

The Peripheral Direct Memory Access circuitry, PDMA, moves data between the peripherals and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt service routine execution. It improves system performance as the software does not need to connect each data movement operation.

Hardware Divider – DIV

- Signed/unsigned 32-bit divider
- Calculate in 8 clock cycles, load in 1 clock cycle
- Division by zero error Flag

The divider is the truncated division and needs a software triggered start signal by using the control register "START" bit. After 8 clock cycles, the divider calculate complete flag will be set to 1, and if the divisor register data is zero, the division by zero error flag will be set to 1.

Universal Serial Bus Device Controller – USB

- Complies with USB 2.0 Full-Speed (12 Mbps) specification
- Fully integrated USB full-speed transceiver
- 1 control endpoint (EP0) for control transfer
- 3 single-buffered endpoints for bulk and interrupt transfer
- 4 double-buffered endpoints for bulk, interrupt and isochronous transfer
- 1,024 bytes EP_SRAM used as the endpoint data buffers

The USB device controller is compliant with the USB 2.0 full-speed specification. There is one control endpoint known as Endpoint 0 and seven configurable endpoints. A 1024-byte SRAM is used as the endpoint buffers. Each endpoint buffer size is programmable using corresponding registers, thus providing maximum flexibility for various applications. The integrated USB full-speed transceiver helps to minimize overall system complexity and cost. The USB also contains suspend and resume features to meet low-power consumption requirement.

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watch points

Package and Operation Temperature

- 32/46-pin QFN and 48/64-pin LQFP packages
- Operation temperature range: -40 °C to + 85 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F50343
Main Flash (KB)		63
Option Bytes Flash (KB)		1
SRAM (KB)		12
Timers	GPTM	1
	PWM	3
	SCTM	2
	BFTM	2
	WDT	1
	RTC	1
Communication	USB	1
	SPI	2
	UART	2
	I^2C	2
	SLED	2
PDMA		6 Channels
Hardware Divider		1
CRC-16/32		1
EXTI		16
12-bit ADC		1
Number of channels		12 Channels
GPIO		Up to 51
CPU frequency		Up to 60 MHz
Operating voltage		2.5 V ~ 5.5 V
Operating temperature		-40 °C ~ 85 °C
Package		32/46-pin QFN and 48/64-pin LQFP

Block Diagram

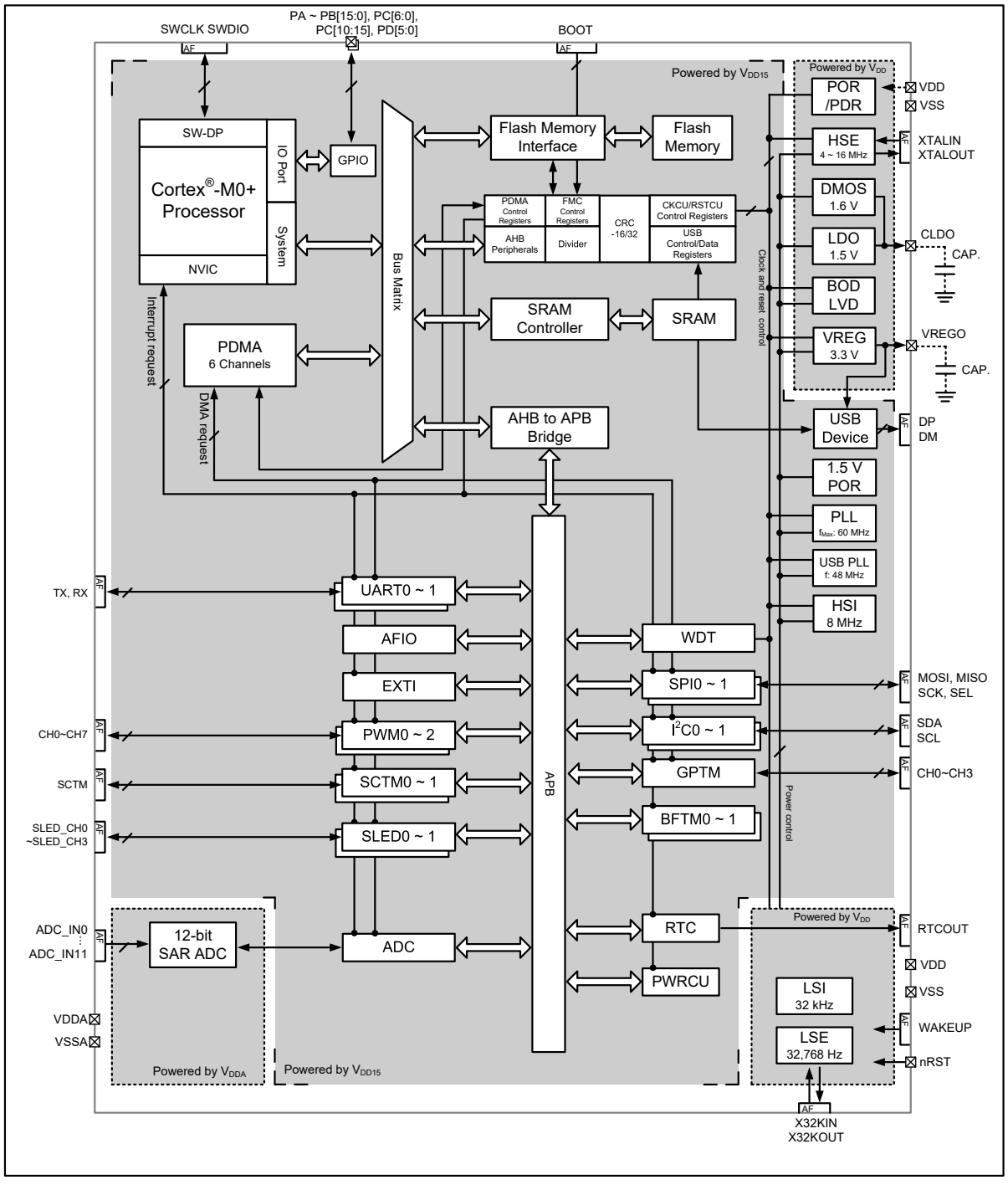


Figure 1. Block Diagram

Memory Map

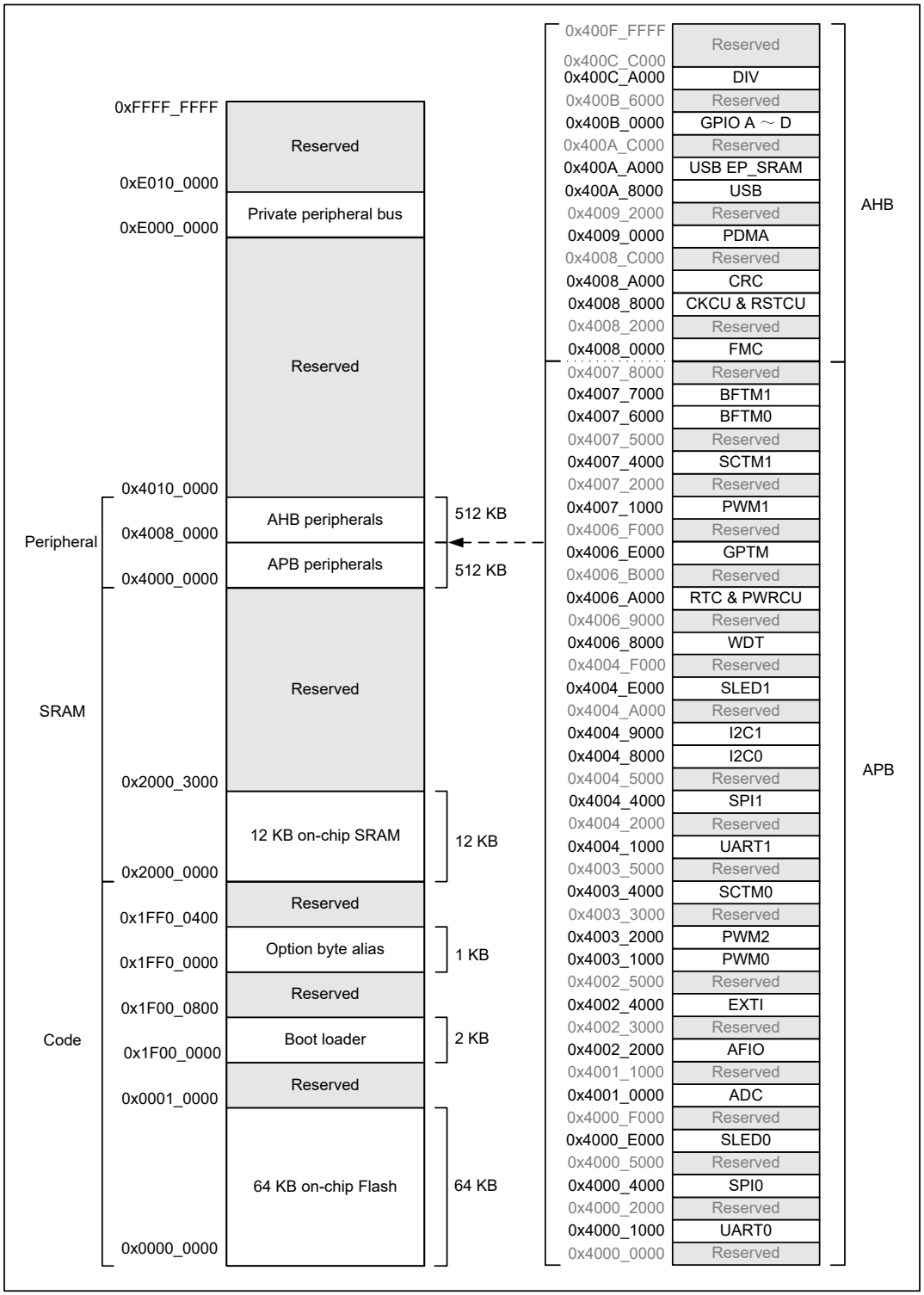


Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	Reserved	APB
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI0	
0x4000_5000	0x4000_DFFF	Reserved	
0x4000_E000	0x4000_EFFF	SLED0	
0x4000_F000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4003_0FFF	Reserved	
0x4003_1000	0x4003_1FFF	PWM0	
0x4003_2000	0x4003_2FFF	PWM2	
0x4003_3000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4004_0FFF	Reserved	
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_3FFF	Reserved	
0x4004_4000	0x4004_4FFF	SPI1	
0x4004_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^2C0	
0x4004_9000	0x4004_9FFF	I^2C1	
0x4004_A000	0x4004_DFFF	Reserved	
0x4004_E000	0x4004_EFFF	SLED1	
0x4004_F000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC & PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_0FFF	Reserved	
0x4007_1000	0x4007_1FFF	PWM1	
0x4007_2000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	

Start Address	End Address	Peripheral	Bus
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU & RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x4008_FFFF	Reserved	
0x4009_0000	0x4009_1FFF	PDMA Control Registers	
0x4009_2000	0x400A_7FFF	Reserved	
0x400A_8000	0x400A_9FFF	USB Control Registers	
0x400A_A000	0x400A_BFFF	USB EP_SRAM	
0x400A_C000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIO A	
0x400B_2000	0x400B_3FFF	GPIO B	
0x400B_4000	0x400B_5FFF	GPIO C	
0x400B_6000	0x400B_7FFF	GPIO D	
0x400B_8000	0x400C_9FFF	Reserved	
0x400C_A000	0x400C_BFFF	DIV	
0x400C_C000	0x400F_FFFF	Reserved	

Clock Structure

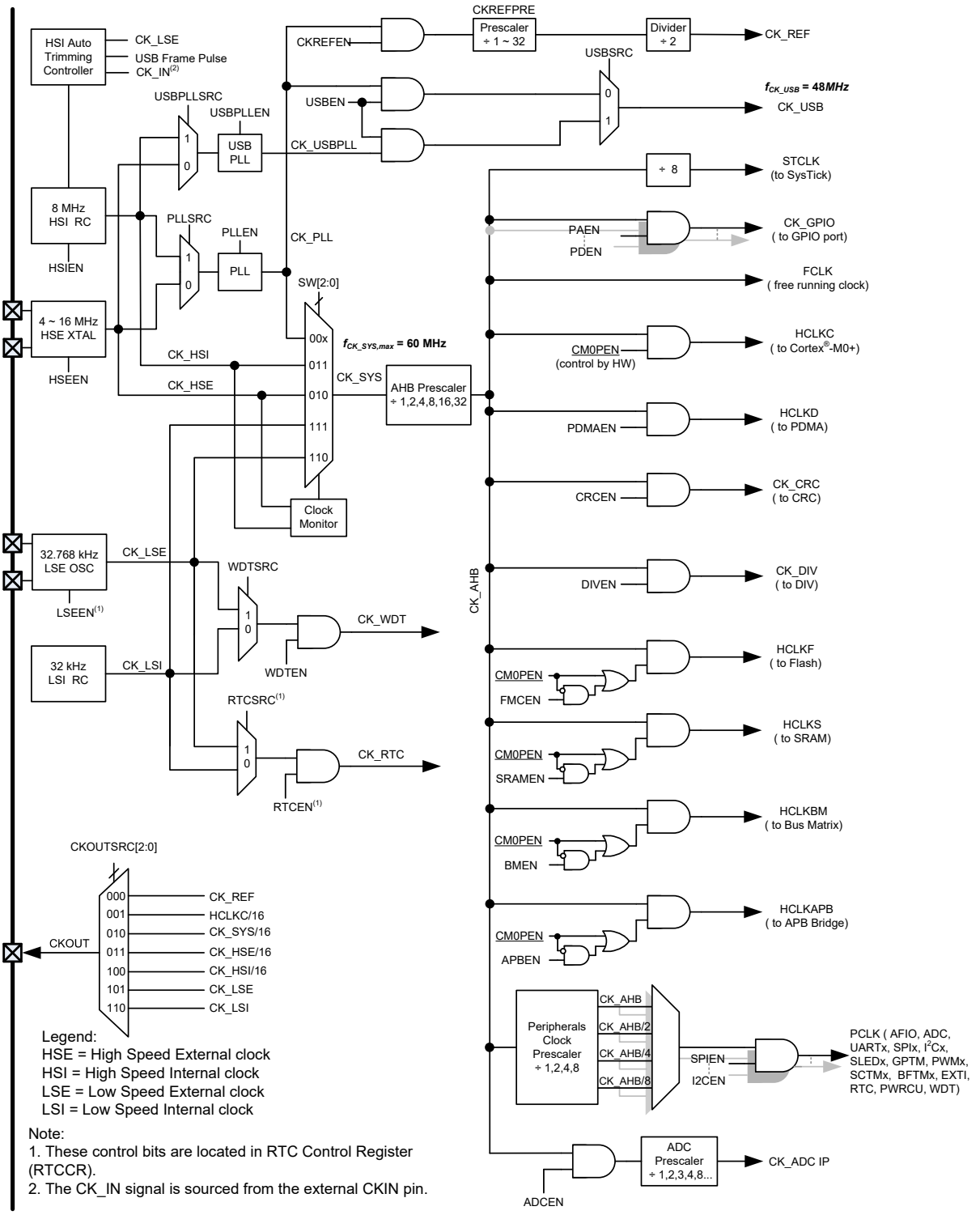


Figure 3. Clock Structure

4 Pin Assignment

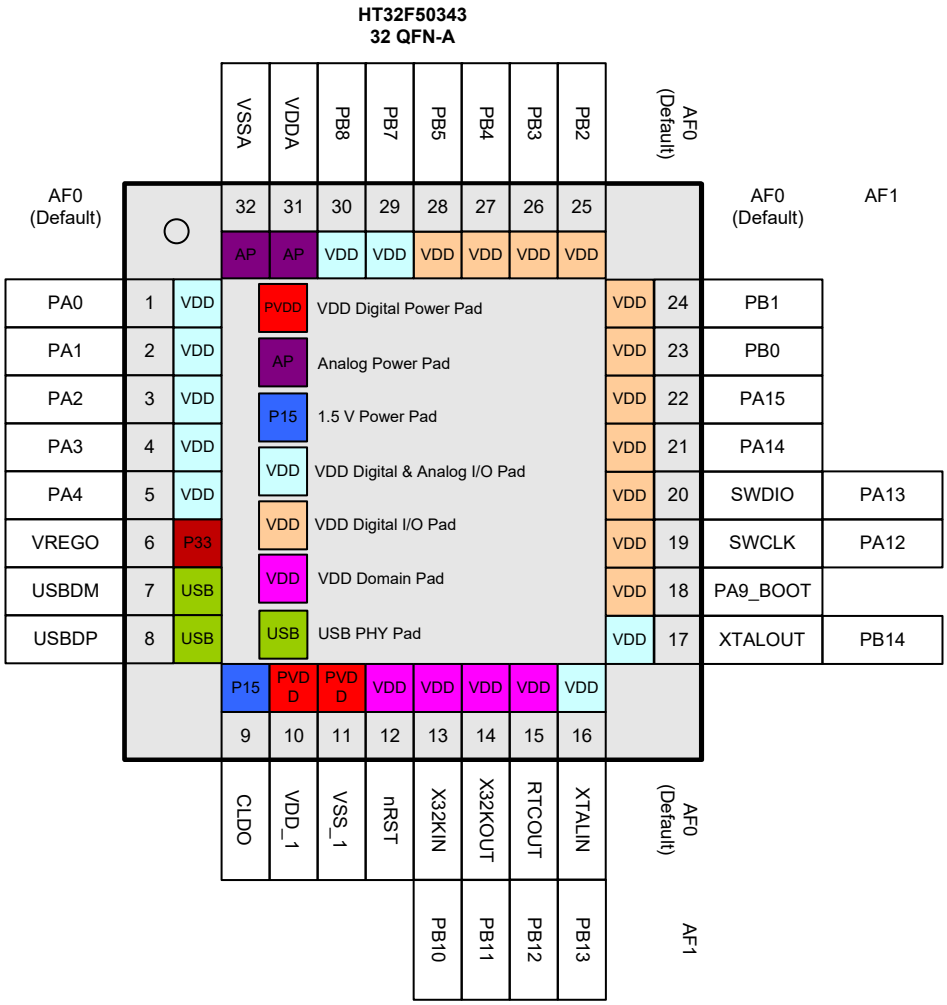


Figure 4. 32-pin QFN Pin Assignment

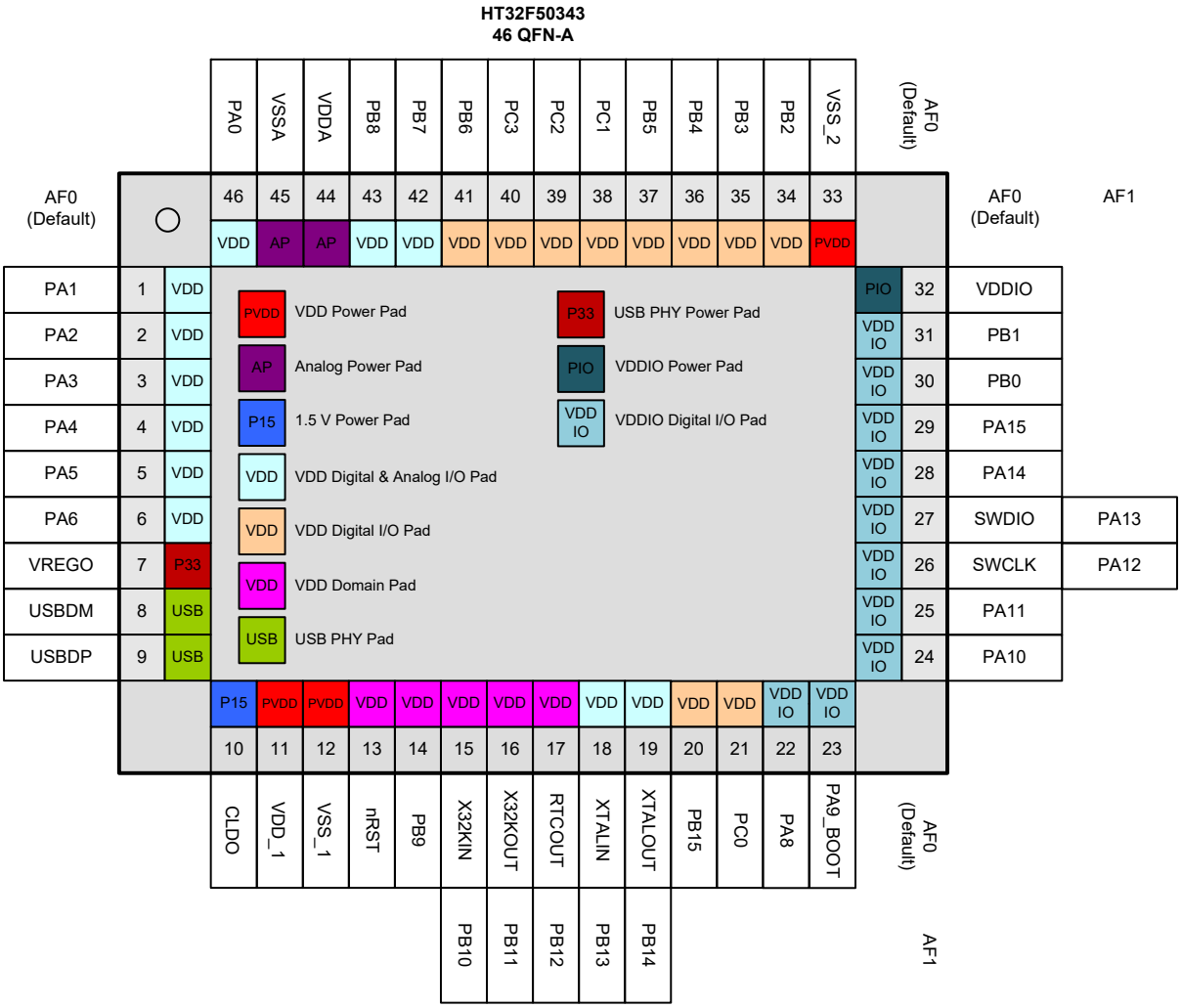


Figure 5. 46-pin QFN Pin Assignment

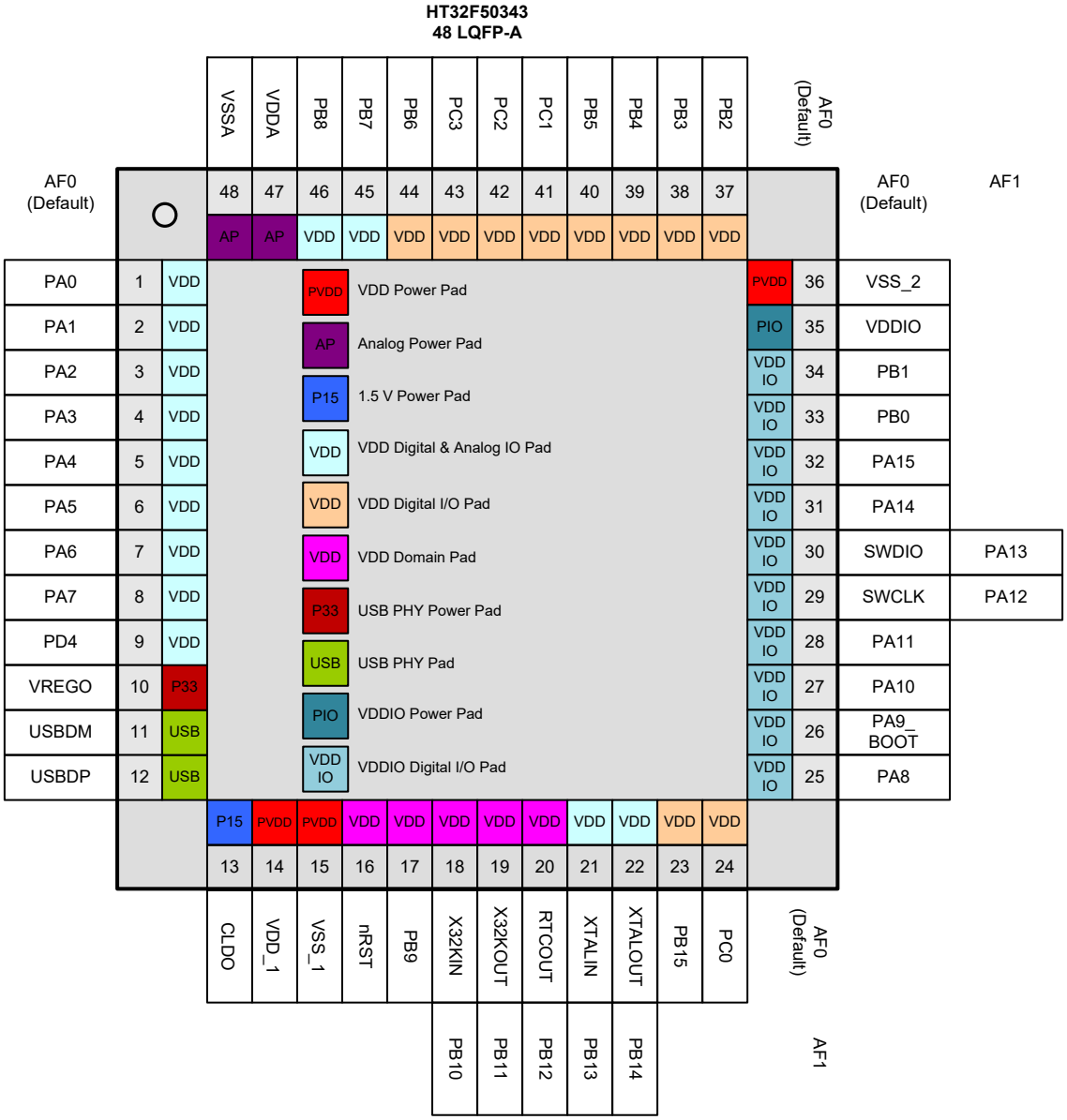


Figure 6. 48-pin LQFP Pin Assignment

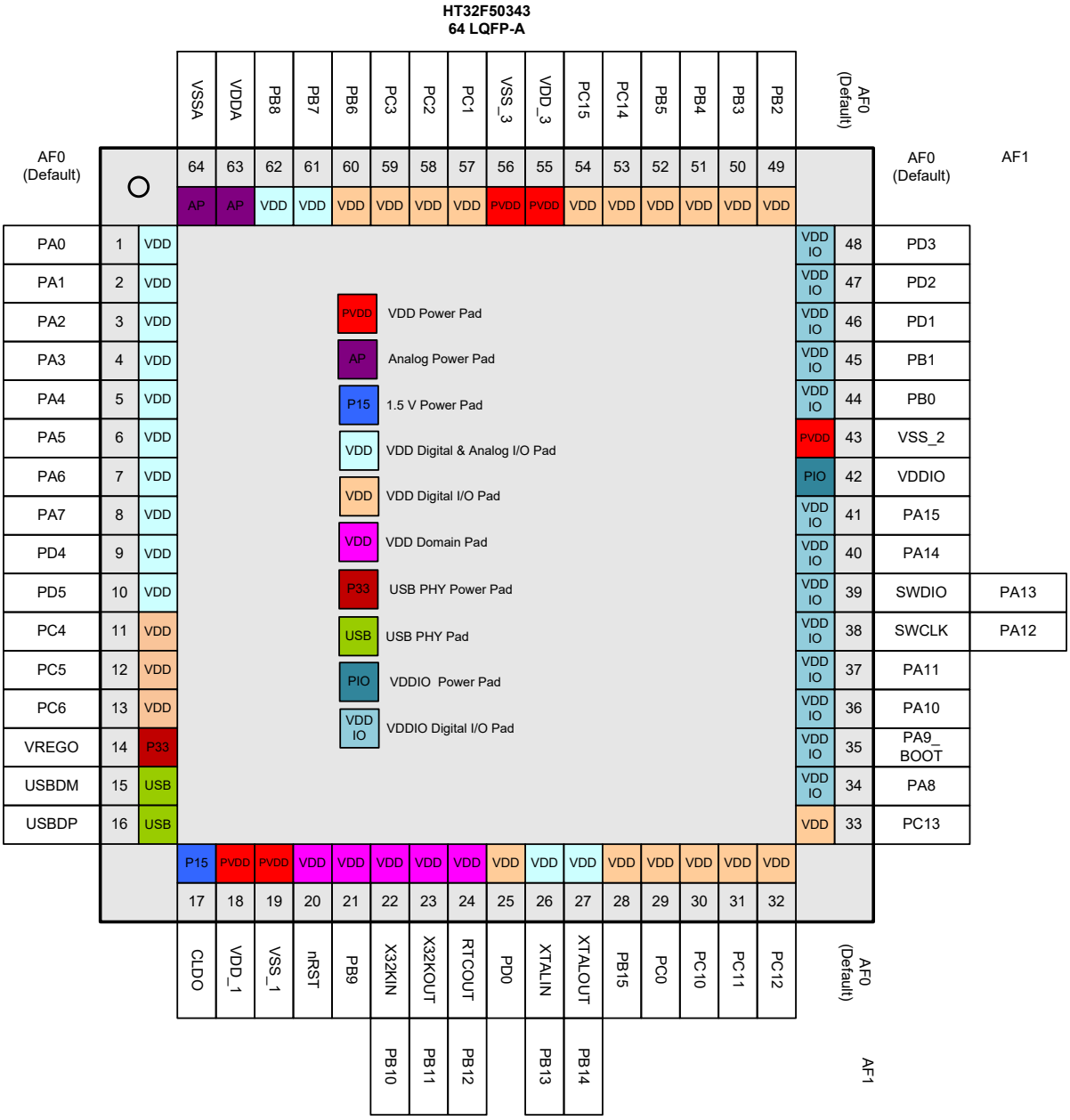


Figure 7. 64-pin LQFP Pin Assignment

Table 3. Pin Assignment for 32/46-pin QFN and 48/64-pin LQFP Packages

Package				Alternate Function Mapping															
				AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64 LQFP	48 LQFP	46 QFN	32 QFN	System Default	GPIO	ADC	N/A	GPTM	SPI	UART	I²C	N/A	N/A	N/A	N/A	N/A	SCTM / PWM	SLED	System Other
1	1	46	1	PA0		ADC_IN2		GT_CH0	SPI1_SCK	UR1_TX	I2C0_SCL						PWM1_CH0	SLED1_CH0	
2	2	1	2	PA1		ADC_IN3		GT_CH1	SPI1_MOSI	UR1_RX	I2C0_SDA						PWM1_CH1	SLED1_CH1	
3	3	2	3	PA2		ADC_IN4		GT_CH2	SPI1_MISO	UR0_TX							PWM1_CH2	SLED1_CH2	
4	4	3	4	PA3		ADC_IN5		GT_CH3	SPI1_SEL	UR0_RX							PWM1_CH3	SLED1_CH3	
5	5	4	5	PA4		ADC_IN6		GT_CH0	SPI0_SCK	UR1_TX	I2C1_SCL						PWM1_CH4	SLED0_CH0	
6	6	5		PA5		ADC_IN7		GT_CH1	SPI0_MOSI	UR1_RX	I2C1_SDA						PWM1_CH5	SLED0_CH1	
7	7	6		PA6		ADC_IN8		GT_CH2	SPI0_MISO								PWM1_CH6	SLED0_CH2	
8	8			PA7		ADC_IN9		GT_CH3	SPI0_SEL								PWM1_CH7	SLED0_CH3	
9	9			PD4		ADC_IN10				UR1_TX							SCTM0		
10				PD5		ADC_IN11				UR1_RX							SCTM1		
11				PC4				GT_CH0	SPI1_SEL	UR0_TX	I2C1_SCL						SCTM0	SLED1_CH0	
12				PC5				GT_CH1	SPI1_SCK	UR0_RX	I2C1_SDA						SCTM1	SLED1_CH1	
13				PC6				GT_CH2	SPI1_MOSI									SLED1_CH2	
14	10	7	6	VREGO															
15	11	8	7	USBDM															
16	12	9	8	USBDP															
17	13	10	9	CLDO															
18	14	11	10	VDD_1															
19	15	12	11	VSS_1															
20	16	13	12	nRST															
21	17	14		PB9													SCTM1		WAKEUP1
22	18	15	13	X32KIN	PB10			GT_CH0	SPI1_SEL	UR1_TX							SCTM0	SLED0_CH0	
23	19	16	14	X32KOUT	PB11			GT_CH1	SPI1_SCK	UR1_RX							SCTM1	SLED0_CH1	
24	20	17	15	RTCOUT	PB12				SPI0_MISO	UR0_RX							SCTM0		WAKEUP0
25				PD0													SCTM1		
26	21	18	16	XTALIN	PB13					UR0_TX							PWM0_CH0	SLED0_CH2	
27	22	19	17	XTALOUT	PB14					UR0_RX							PWM0_CH1	SLED0_CH3	
28	23	20		PB15					SPI0_SEL		I2C1_SCL						PWM0_CH2		
29	24	21		PC0					SPI0_SCK		I2C1_SDA						PWM0_CH3		
30				PC10				GT_CH0	SPI1_SEL								PWM0_CH4		
31				PC11				GT_CH1	SPI1_SCK								PWM0_CH5		
32				PC12				GT_CH2	SPI1_MOSI	UR1_TX	I2C0_SCL						PWM0_CH6		
33				PC13				GT_CH3	SPI1_MISO	UR1_RX	I2C0_SDA						PWM0_CH7		
34	25	22		PA8						UR1_TX							SCTM0	SLED1_CH0	
35	26	23	18	PA9_BOOT					SPI0_MOSI								SCTM1	SLED1_CH1	CKOUT
36	27	24		PA10					SPI0_MOSI	UR1_RX							PWM0_CH4	SLED1_CH2	

Package				Alternate Function Mapping															
				AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64 LQFP	48 LQFP	46 QFN	32 QFN	System Default	GPIO	ADC	N/A	GPTM	SPI	UART	I²C	N/A	N/A	N/A	N/A	N/A	SCTM / PWM	SLED	System Other
37	28	25		PA11					SPI0_ MISO								PWM0_ CH5	SLED1_ CH3	
38	29	26	19	SWCLK	PA12														
39	30	27	20	SWDIO	PA13														
40	31	28	21	PA14					SPI1_ SEL		I2C1_ SCL						PWM0_ CH2	SLED0_ CH2	
41	32	29	22	PA15					SPI1_ SCK		I2C1_ SDA						PWM0_ CH3	SLED0_ CH3	
42	35	32		VDDIO															
43	36	33		VSS_2															
44	33	30	23	PB0					SPI1_ MOSI	UR0_ TX	I2C0_ SCL						PWM0_ CH0	SLED0_ CH0	
45	34	31	24	PB1					SPI1_ MISO	UR0_ RX	I2C0_ SDA						PWM0_ CH1	SLED0_ CH1	
46				PD1													SCTM0		
47				PD2													PWM0_ CH6		
48				PD3													PWM0_ CH7		
49	37	34	25	PB2					SPI0_ SEL	UR1_ TX							SCTM0	SLED0_ CH2	CKIN
50	38	35	26	PB3					SPI0_ SCK	UR1_ RX							SCTM1	SLED0_ CH3	
51	39	36	27	PB4					SPI0_ MOSI	UR1_ TX							PWM2_ CH2	SLED1_ CH2	
52	40	37	28	PB5				GT_CH2	SPI0_ MISO	UR1_ RX							PWM2_ CH3	SLED1_ CH3	
53				PC14							I2C0_ SCL						SCTM0		
54				PC15							I2C0_ SDA						SCTM1		
55				VDD_3															
56				VSS_3															
57	41	38		PC1					SPI1_ SEL	UR1_ TX							PWM2_ CH4		
58	42	39		PC2					SPI1_ SCK								PWM2_ CH5		
59	43	40		PC3					SPI1_ MOSI	UR1_ RX							PWM2_ CH6		
60	44	41		PB6				GT_CH3	SPI1_ MISO	UR0_ TX							PWM2_ CH7		
61	45	42	29	PB7		ADC_ IN0			SPI0_ MISO	UR0_ TX	I2C1_ SCL						PWM2_ CH0	SLED1_ CH0	
62	46	43	30	PB8		ADC_ IN1			SPI0_ SEL	UR0_ RX	I2C1_ SDA						PWM2_ CH1	SLED1_ CH1	
63	47	44	31	VDDA															
64	48	45	32	VSSA															

Table 4. Pin Description

Pin Number				Pin Name	Type[1]	I/O Structure[2]	Output Driving	Description
64 LQFP	48 LQFP	46 QFN	32 QFN					Default Function (AF0)
1	1	46	1	PA0	AI/O	5V	4/8/12/16 mA	PA0
2	2	1	2	PA1	AI/O	5V	4/8/12/16 mA	PA1
3	3	2	3	PA2	AI/O	5V	4/8/12/16 mA	PA2
4	4	3	4	PA3	AI/O	5V	4/8/12/16 mA	PA3
5	5	4	5	PA4	AI/O	5V	4/8/12/16 mA	PA4
6	6	5		PA5	AI/O	5V	4/8/12/16 mA	PA5
7	7	6		PA6	AI/O	5V	4/8/12/16 mA	PA6
8	8			PA7	AI/O	5V	4/8/12/16 mA	PA7
9	9			PD4	AI/O	5V	4/8/12/16 mA	PD4
10				PD5	AI/O	5V	4/8/12/16 mA	PD5
11				PC4	I/O	5V	4/8/12/16 mA	PC4
12				PC5	I/O	5V	4/8/12/16 mA	PC5
13				PC6	I/O	5V	4/8/12/16 mA	PC6
14	10	7	6	VREGO	P	—	—	On-chip USB voltage regulator 3.3 V output If using the internal USB voltage regulator, it must be connected a 2.2 μF capacitor as close as possible between this pin and VSS_1.
15	11	8	7	USBDM	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
16	12	9	8	USBDP	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
17	13	10	9	CLDO	P	—	—	Core power LDO 1.5 V output It must be connected a 2.2 μF capacitor as close as possible between this pin and VSS_1.
18	14	11	10	VDD_1	P	—	—	Voltage for VDD domain digital I/O
19	15	12	11	VSS_1	P	—	—	Ground reference for digital I/O
20	16	13	12	nRST[3]	I	5V_PU	—	External reset pin
21	17	14		PB9[3]	I/O (V_{DD})	5V	4/8/12/16 mA	PB9
22	18	15	13	PB10[3]	AI/O (V_{DD})	5V	4/8/12/16 mA	X32KIN
23	19	16	14	PB11[3]	AI/O (V_{DD})	5V	4/8/12/16 mA	X32KOUT
24	20	17	15	PB12[3]	I/O (V_{DD})	5V	4/8/12/16 mA	RTCOUT
25				PD0	I/O	5V	4/8/12/16 mA	PD0
26	21	18	16	PB13	AI/O	5V	4/8/12/16 mA	XTALIN
27	22	19	17	PB14	AI/O	5V	4/8/12/16 mA	XTALOUT
28	23	20		PB15	I/O	5V	4/8/12/16 mA	PB15
29	24	21		PC0	I/O	5V	4/8/12/16 mA	PC0
30				PC10	I/O	5V	4/8/12/16 mA	PC10
31				PC11	I/O	5V	4/8/12/16 mA	PC11
32				PC12	I/O	5V	4/8/12/16 mA	PC12
33				PC13	I/O	5V	4/8/12/16 mA	PC13
34	25	22		PA8	I/O (V_{DDIO})	5V	4/8/12/16 mA	PA8

Pin Number				Pin Name	Type[1]	I/O Structure[2]	Output Driving	Description
64 LQFP	48 LQFP	46 QFN	32 QFN					Default Function (AF0)
35	26	23	18	PA9	I/O (V_{DDIO})	5V_PU	4/8/12/16 mA	PA9_BOOT
36	27	24		PA10	I/O (V_{DDIO})	5V	4/8/12/16 mA	PA10
37	28	25		PA11	I/O (V_{DDIO})	5V	4/8/12/16 mA	PA11
38	29	26	19	PA12	I/O (V_{DDIO})	5V_PU	4/8/12/16 mA	SWCLK
39	30	27	20	PA13	I/O (V_{DDIO})	5V_PU	4/8/12/16 mA	SWDIO
40	31	28	21	PA14	I/O (V_{DDIO})	5V	4/8/12/16 mA	PA14
41	32	29	22	PA15	I/O (V_{DDIO})	5V	4/8/12/16 mA	PA15
42	35	32		VDDIO	P	—	—	Voltage for digital VDDIO domain I/O
43	36	33		VSS_2	P	—	—	Ground reference for digital I/O
44	33	30	23	PB0	I/O (V_{DDIO})	5V	4/8/12/16 mA	PB0
45	34	31	24	PB1	I/O (V_{DDIO})	5V	4/8/12/16 mA	PB1
46				PD1	I/O (V_{DDIO})	5V	4/8/12/16 mA	PD1
47				PD2	I/O (V_{DDIO})	5V	4/8/12/16 mA	PD2
48				PD3	I/O (V_{DDIO})	5V	4/8/12/16 mA	PD3
49	37	34	25	PB2	I/O	5V	4/8/12/16 mA	PB2
50	38	35	26	PB3	I/O	5V	4/8/12/16 mA	PB3
51	39	36	27	PB4	I/O	5V	4/8/12/16 mA	PB4
52	40	37	28	PB5	I/O	5V	4/8/12/16 mA	PB5
53				PC14	I/O	5V	4/8/12/16 mA	PC14
54				PC15	I/O	5V	4/8/12/16 mA	PC15
55				VDD_3	P	—	—	Voltage for VDD domain digital I/O
56				VSS_3	P	—	—	Ground reference for digital I/O
57	41	38		PC1	I/O	5V	4/8/12/16 mA	PC1
58	42	39		PC2	I/O	5V	4/8/12/16 mA	PC2
59	43	40		PC3	I/O	5V	4/8/12/16 mA	PC3
60	44	41		PB6	I/O	5V	4/8/12/16 mA	PB6
61	45	42	29	PB7	AI/O	5V	4/8/12/16 mA	PB7
62	46	43	30	PB8	AI/O	5V	4/8/12/16 mA	PB8
63	47	44	31	VDDA	P	—	—	Analog voltage for ADC
64	48	45	32	VSSA	P	—	—	Ground reference for the ADC

Note: 1. I = input, O = output, A = Analog port, P = Power Supply, V_{DD} = V_{DD} Power.
2. 5V = 5 V operation I/O type, PU = Pull-up.
3. These pins are located at the V_{DD} power domain.
4. In the Boot loader mode, only the USB interface can be used for communication.

5 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	External Main Supply Voltage	V_{SS} - 0.3	V_{SS} + 5.5	V
V_{DDIO}	External I/O Supply Voltage	V_{SS} - 0.3	V_{SS} + 5.5	V
V_{DDA}	External Analog Supply Voltage	V_{SSA} - 0.3	V_{SSA} + 5.5	V
V_{IN}	Input Voltage on I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
T_A	Ambient Operating Temperature Range	-40	+85	°C
T_{STG}	Storage Temperature Range	-55	+150	°C
T_J	Maximum Junction Temperature	—	+125	°C
P_D	Total Power Dissipation	—	500	mW
V_{ESD}	Electrostatic Discharge Voltage – Human Body Mode	-4000	+4000	V

Recommended DC Operating Conditions

Table 6. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	—	2.5	5.0	5.5	V
V_{DDIO}	I/O Operating Voltage	—	1.8	5.0	5.5	V
V_{DDA}	Analog Operating Voltage	—	2.5	5.0	5.5	V

On-Chip LDO Voltage Regulator Characteristics

Table 7. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	V_{DD} ≥ 2.5 V Regulator input @ I_{LDO} = 35 mA and voltage variant = ±5 %, After trimming	1.425	1.5	1.57	V
I_{LDO}	Output Current	V_{DD} = 2.5 V Regulator input @ V_{LDO} = 1.5 V	—	30	35	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	μF

On-Chip USB Voltage Regulator Characteristics

Table 8. USB Voltage Regulator Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{IN}	Operation Voltage Input Range	—		2.5	—	5.5	V
V_{VREGO}	On-chip USB Regulator Output Voltage after Trimming	V_{IN} ≥ 3.6 V	3.3 V VREGVS [1:0] = 00	3.069	3.3	3.531	V
		V_{IN} ≥ 3.4 V	3.0 V VREGVS [1:0] = 01	2.79	3.0	3.21	
		V_{IN} ≥ 4.5 V	4.0 V VREGVS [1:0] = 10	3.72	4.0	4.28	
		V_{IN} ≥ 2.5 V	1.8 V VREGVS [1:0] = 11	1.656	1.8	1.944	
I_{VREGO}	Output Current (Regulator Normal Mode)	V_{IN} = 3.6 V Regulator input @ V_{VREGO} = 3.3 V		—	30	50	mA
$V_{VREGOLR}$	Output Load Regulation (Regulator Normal Mode)	V_{IN} = 3.6 V Regulator input @ V_{VREGO} = 3.3 V		—	0.1	1	mV/mA
C_{VREGO}	External Capacitor Value for internal USB Regulator Output (1)	V_{IN} = 5.5 V Regulator input @ V_{VREGO} = 3.3 V; I_{VREGO} ≤ 50 mA		1	2.2	—	μF
I_{STATIC}	Static Current (Regulator Normal Mode)	V_{IN} = 5.5 V @ V_{VREGO} = 3.3 V, T_A = -40 °C ~ 85 °C I_{VREGO} ≤ 50 mA		—	30	50	μA
I_{PWD}	Regulator Power Down Current	V_{IN} = 5.5 V Regulator input		—	—	0.01	μA
t_{SETUP}	Regulator Set Up Time	V_{IN} = 5.5 V, C_{VREGO} = 2.2 μF T_A = -40 °C ~ 85 °C		—	—	500	μs

Note: 1. The Multi-layer Ceramic Capacitor (MLCC) is used for the external capacitor of the power regulator.

2. Owing to the on-chip USB voltage regulator output is internally connected to the USB driver, therefore, the on-chip USB voltage regulator has to be set to 3.3 V voltage output for the full USB electrical characteristics when the MCU USB functionality is active.

3. The reference voltage of the on-chip USB voltage regulator is from the on-chip 1.5 V LDO Bandgap reference.

Power Consumption

Table 9. Power Consumption Characteristics

Symbol	Parameter	f_{HCLK}	Conditions		Typ.	Max @ T_A		Unit
						25 °C	85 °C	
I_{DD}	Run Mode	60 MHz	V_{DD} = 5.0 V HSI = 8 MHz PLL = 60 MHz	All peripherals enabled	17.5	20.0	—	mA
				All peripherals disabled	7.6	8.7	—	
		40 MHz	V_{DD} = 5.0 V HSI = 8 MHz PLL = 40 MHz	All peripherals enabled	13.9	15.9	—	
				All peripherals disabled	7.2	8.3	—	
		20 MHz	V_{DD} = 5.0 V HSI = 8 MHz PLL = 20 MHz	All peripherals enabled	7.1	8.1	—	
				All peripherals disabled	3.4	3.9	—	
		8 MHz	V_{DD} = 5.0 V HSI = 8 MHz PLL = off	All peripherals enabled	3.6	4.1	—	
				All peripherals disabled	1.5	1.7	—	
		32 kHz	V_{DD} = 5.0 V LSI = 32 kHz LDO in low power mode	All peripherals enabled	32.0	42.4	—	µA
				All peripherals disabled	27.2	36.0	—	
	Sleep Mode	60 MHz	V_{DD} = 5.0 V HSI = 8 MHz PLL = 60 MHz MCU core sleep	All peripherals enabled	12.6	14.4	—	mA
				All peripherals disabled	1.9	2.2	—	
		40 MHz	V_{DD} = 5.0 V HSI = 8 MHz PLL = 40 MHz MCU core sleep	All peripherals enabled	8.6	9.9	—	
				All peripherals disabled	1.4	1.6	—	
		20 MHz	V_{DD} = 5.0 V HSI = 8 MHz PLL = 20 MHz MCU core sleep	All peripherals enabled	5.0	5.7	—	
				All peripherals disabled	1.0	1.2	—	
		8 MHz	V_{DD} = 5.0 V HSI = 8 MHz PLL = off MCU core sleep	All peripherals enabled	2.7	3.1	—	
				All peripherals disabled	0.5	0.6	—	
	Deep-Sleep 1 Mode	—	V_{DD} = 5.0 V, All clock off (HSI/HSE/PLL/LSE), LDO in low power mode, LSI on, RTC on		22.6	34.6	—	µA
	Deep-Sleep 2 Mode	—	V_{DD} = 5.0 V, All clock off (HSI/HSE/PLL/LSE), LDO off, DMOS on, LSI on, RTC on		6.7	10.2	—	µA

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
3. RTC means real time clock.
4. Code = while (1) { 208 NOP } executed in Flash.

Reset and Supply Monitor Characteristics

Table 10. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{POR}	Power On Reset Threshold (Rising Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	2.22	2.35	2.48	V
V_{PDR}	Power Down Reset Threshold (Falling Voltage on V_{DD})		2.12	2.2	2.33	V
$V_{PORHYST}$	POR Hysteresis	—	—	150	—	mV
t_{POR}	Reset Delay Time	V_{DD} = 5.0 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.
3. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO will be turned off.

Table 11. LVD / BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown Out Detection	T_A = -40 °C ~ 85 °C After factory-trimmed, V_{DD} Falling edge		2.37	2.45	2.53	V
V_{LVD}	Voltage of Low Voltage Detection	T_A = -40 °C ~ 85 °C, V_{DD} Falling edge	LVDS = 000	2.57	2.65	2.73	V
			LVDS = 001	2.77	2.85	2.93	V
			LVDS = 010	2.97	3.05	3.13	V
			LVDS = 011	3.17	3.25	3.33	V
			LVDS = 100	3.37	3.45	3.53	V
			LVDS = 101	4.15	4.25	4.35	V
			LVDS = 110	4.35	4.45	4.55	V
			LVDS = 111	4.55	4.65	4.75	V
$V_{LVDHTST}$	LVD Hysteresis	V_{DD} = 5.0 V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 5.0 V	—	—	—	5	μs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 5.0 V	—	—	—	—	ms
I_{DDLVD}	Operation Current (3)	V_{DD} = 5.0 V	—	—	10	20	μA

Note: 1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.
3. Bandgap current is not included.
4. LVDS field is in the PWRCU LVDCSR register

External Clock Characteristics

Table 12. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{HSE}	HSE Frequency	V_{DD} = 2.5 V ~ 5.0 V	4	—	16	MHz

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C_{LHSE}	Load Capacitance	V_{DD} = 5.0 V, R_{ESR} = 100 Ω @ 16 MHz	—	—	12	pF
R_{FHSE}	Internal Feedback Resistor between XTALIN and XTALOUT pins	V_{DD} = 5.0 V	—	0.5	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 5.0 V, C_L = 12 pF @ 16 MHz, HSEDR = 0	—	—	110	Ω
		V_{DD} = 2.5 V, C_L = 12 pF @ 16 MHz, HSEDR = 1				
D_{HSE}	HSE Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	V_{DD} = 5.0 V, R_{ESR} = 100 Ω, C_L = 12 pF @ 8 MHz, HSEDR = 0	—	0.85	—	mA
		V_{DD} = 5.0 V, R_{ESR} = 25 Ω, C_L = 12 pF @ 16 MHz, HSEDR = 1	—	3.0	—	
I_{PWDHSE}	HSE Oscillator Power Down Current	V_{DD} = 5.0 V	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	V_{DD} = 5.0 V	—	—	4	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE clock in the PCB layout.

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace length as short as possible to reduce any parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep any high frequency signal lines away from the crystal area to prevent the crosstalk adverse effects.

Table 13. Low Speed External Clock (LSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{CK_LSE}	LSE Frequency	V_{DD} = 2.5 V ~ 5.5 V	—	32.768	—	kHz
R_F	Internal feedback resistor	—	—	10	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 5.0 V	30	—	TBD	kΩ
C_L	Recommended load capacitances	V_{DD} = 5.0 V	6	—	TBD	pF
I_{DDLSE}	Oscillator Supply Current (High Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, C_L ≥ 7 pF, V_{DD} = 2.5 V ~ 5.5 V, T_A = -40 °C ~ +85 °C	—	4.0	5.6	μA
	Oscillator Supply Current (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, C_L < 7 pF, V_{DD} = 2.5 V ~ 5.5 V, T_A = -40 °C ~ +85 °C	—	3.6	4.5	μA
	Power Down Current	—	—	—	0.01	μA
t_{SULSE}	LSE Oscillator Startup Time (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, V_{DD} = 2.5 V ~ 5.5 V	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the LSE clock in the PCB layout.

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace length as short as possible to reduce any parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep any high frequency signal lines away from the crystal area to prevent the crosstalk adverse effects.

Internal Clock Characteristics

Table 14. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{HSI}	HSI Frequency	V_{DD} = 5 V @ 25 °C	—	8	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V_{DD} = 5.0 V, T_A = 25 °C	-2	—	2	%
		V_{DD} = 2.5 V ~ 5.5 V, T_A = -40 °C ~ 85 °C	-3	—	3	%
Duty	Duty Cycle	f_{HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	Oscillator Supply Current	f_{HSI} = 8 MHz @ V_{DD} = 2.5 V ~ 5.5 V	—	—	140	μA
	Power Down Current		—	—	0.01	μA
t_{SUHSI}	HSI Oscillator Startup time	f_{HSI} = 8 MHz	—	—	20	μs

Table 15. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	T_A = -40 °C ~ 85 °C	2.5	—	5.5	V
f_{LSI}	LSI Frequency	V_{DD} = 5.0 V, T_A = -40 °C ~ 85 °C	21	32	43	kHz
ACC_{LSI}	LSI Frequency Accuracy	V_{DD} = 5.0 V, with factory-trimmed	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 5.0 V	—	0.5	0.8	μA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 5.0 V	—	—	100	μs

Memory Characteristics

Table 16. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program/ Erase Cycles before failure (Endurance)	T_A = -40 °C ~ 85 °C	10	—	—	K cycles
t_{RET}	Data Retention Time	T_A = -40 °C ~ 85 °C	10	—	—	Years
t_{PROG}	Word Programming Time	T_A = -40 °C ~ 85 °C	20	—	—	μs
t_{ERASE}	Page Erase Time	T_A = -40 °C ~ 85 °C	2	—	—	ms
t_{MERASE}	Mass Erase Time	T_A = -40 °C ~ 85 °C	10	—	—	ms

I/O Port Characteristics

Table 17. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	5.0 V I/O	V_I = V_{SS}, On-chip pull-up resister disabled	—	—	3	μA
		Reset pin		—	—	3	μA
I_{IH}	High Level Input Current	5.0 V I/O	V_I = V_{DD}, On-chip pull-down resister disabled	—	—	3	μA
		Reset pin		—	—	3	μA
V_{IL}	Low Level Input Voltage	5.0 V I/O		- 0.5	—	V_{DD} × 0.35	V
		Reset pin		- 0.5	—	V_{DD} × 0.35	V
V_{IH}	High Level Input Voltage	5.0 V I/O		V_{DD} × 0.65	—	V_{DD} + 0.5	V
		Reset pin		V_{DD} × 0.65	—	V_{DD} + 0.5	V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	5.0 V I/O	—	0.12 × V_{DD}	—	mV
		Reset pin	—	0.12 × V_{DD}	—	mV
I_{OL}	Low Level Output Current (GPIO Sink Current)	5.0 V I/O 4 mA drive, V_{OL} = 0.6 V	4	—	—	mA
		5.0 V I/O 8 mA drive, V_{OL} = 0.6 V	8	—	—	mA
		5.0 V I/O 12 mA drive, V_{OL} = 0.6 V	12	—	—	mA
		5.0 V I/O 16 mA drive, V_{OL} = 0.6 V	16	—	—	mA
I_{OH}	High Level Output Current (GPIO Source Current)	5.0 V I/O 4 mA drive, V_{OH} = V_{DD} - 0.6 V	—	4	—	mA
		5.0 V I/O 8 mA drive, V_{OH} = V_{DD} - 0.6 V	—	8	—	mA
		5.0 V I/O 12 mA drive, V_{OH} = V_{DD} - 0.6 V	—	12	—	mA
		5.0 V I/O 16 mA drive, V_{OH} = V_{DD} - 0.6 V	—	16	—	mA
V_{OL}	Low Level Output Voltage	5.0 V 4 mA drive I/O, I_{OL} = 4 mA	—	—	0.6	V
		5.0 V 8 mA drive I/O, I_{OL} = 8 mA	—	—	0.6	V
		5.0 V 12 mA drive I/O, I_{OL} = 12 mA	—	—	0.6	V
		5.0 V 16 mA drive I/O, I_{OL} = 16 mA	—	—	0.6	V
V_{OH}	High Level Output Voltage	5.0 V 4 mA drive I/O, I_{OH} = 4 mA	V_{DD} - 0.6	—	—	V
		5.0 V 8 mA drive I/O, I_{OH} = 8 mA	V_{DD} - 0.6	—	—	V
		5.0 V 12 mA drive I/O, I_{OH} = 12 mA	V_{DD} - 0.6	—	—	V
		5.0 V 16 mA drive I/O, I_{OH} = 16 mA	V_{DD} - 0.6	—	—	V
R_{PU}	Internal Pull-up Resistor	V_{DD} = 5.0 V	—	50	—	kΩ
		V_{DD} = 3.3 V	—	76	—	
R_{PD}	Internal Pull-down Resistor	V_{DD} = 5.0 V	—	50	—	kΩ
		V_{DD} = 3.3 V	—	76	—	

ADC Characteristics

Table 18. ADC Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—	2.5	5.0	5.5	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference Voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	Current Consumption	V_{DDA} = 5.0 V, 1 Msps	—	1.4	1.5	mA
I_{ADC_DN}	Power Down Current Consumption	V_{DDA} = 5.0 V	—	—	0.1	μA
f_{ADC}	A/D Converter Clock Frequency	—	0.7	—	16	MHz

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_S	Sampling Rate	—	0.05	—	1	MHz
t_{DL}	Data Latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & Hold Time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter Conversion Time	—	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C_I	Input Sampling Capacitance	No pin/pad capacitance included	—	4	—	pF
t_{SU}	Startup Time	—	—	—	1	μs
N	Resolution	—	—	12	—	bits
INL	Integral Non-linearity Error	f_S = 750 kHz, V_{DDA} = 5.0 V	—	±2	±5	LSB
DNL	Differential Non-linearity Error	f_S = 750 kHz, V_{DDA} = 5.0 V	—	±1	—	LSB
E_O	Offset Error	—	—	—	±10	LSB
E_G	Gain Error	—	—	—	±10	LSB

Note: 1. Guaranteed by design, not tested in production.

2. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.

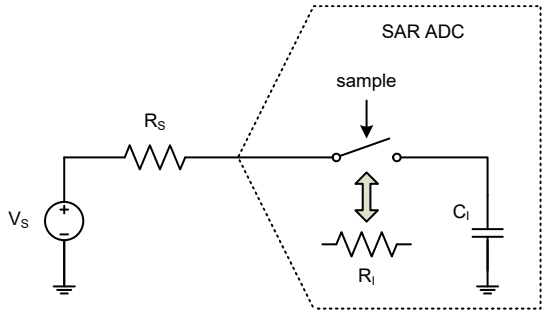


Figure 8. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0 V and V_{REF}) are sampled consecutively. In this situation a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

GPTM / PWM / SCTM Characteristics

Table 19. GPTM/PWM/SCTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for GPTM, PWM and SCTM	—	—	—	f_{PCLK}	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	$1/f_{TM}$
f_{EXT}	External Signal Frequency on Channel 1 ~ 4	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	bits

I²C Characteristics

Table 20. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL and SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL and SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time (5)	0	—	0	—	0	—	ns
	SDA Data Hold Time (6)	100	—	100	—	100	—	ns
$t_{VD(SDA)}$	SDA Data Valid Time	—	1.6	—	0.475	—	0.25	μs
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Guaranteed by design, not tested in production.
2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast plus mode, the peripheral clock frequency must be higher than 20 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 0 and SEQFILTER = 00.
6. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 1 and SEQFILTER = 00.

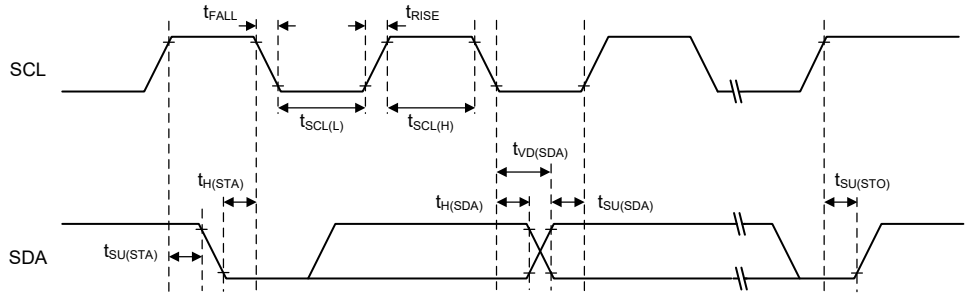


Figure 9. I²C Timing Diagram

SPI Characteristics

Table 21. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK}	SPI Master Output SCK Clock Frequency	Master mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High and Low Time	—	$t_{SCK}/2$ - 2	—	$t_{SCK}/2$ + 1	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
f_{SCK}	SPI Slave Input SCK Clock Frequency	Slave mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	3 t_{PCLK}	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	2 t_{PCLK}	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	3 t_{PCLK}	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

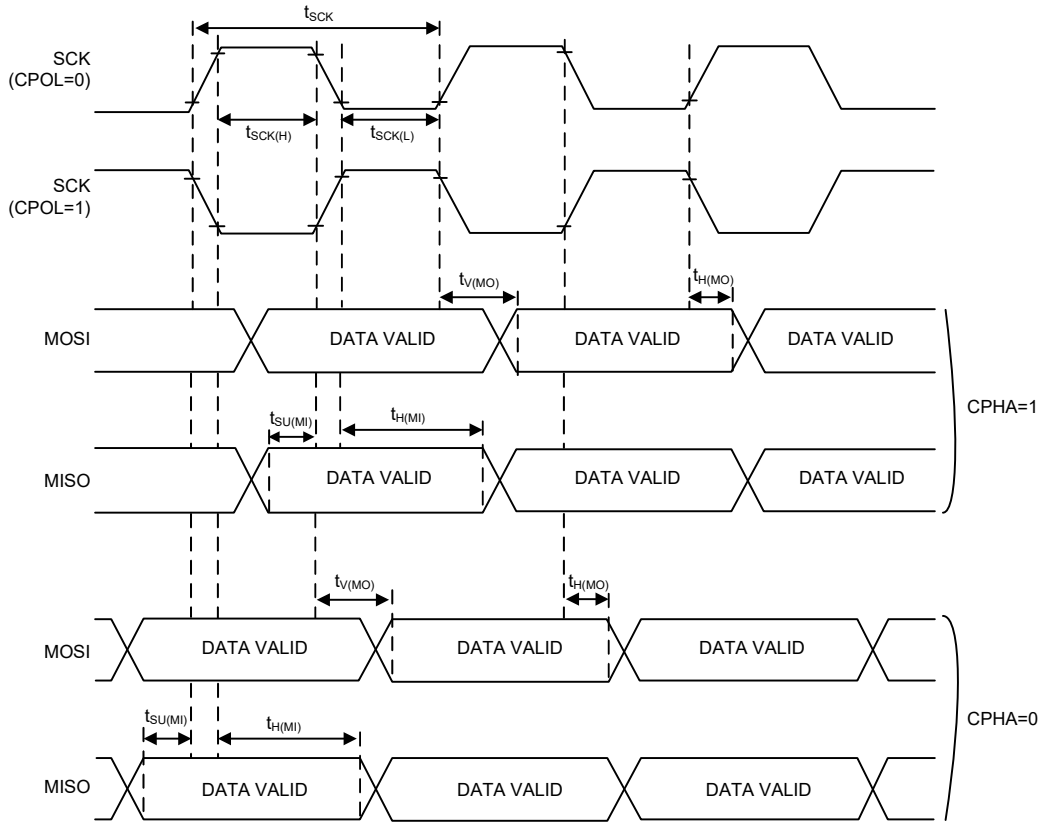


Figure 10. SPI Timing Diagram – SPI Master Mode

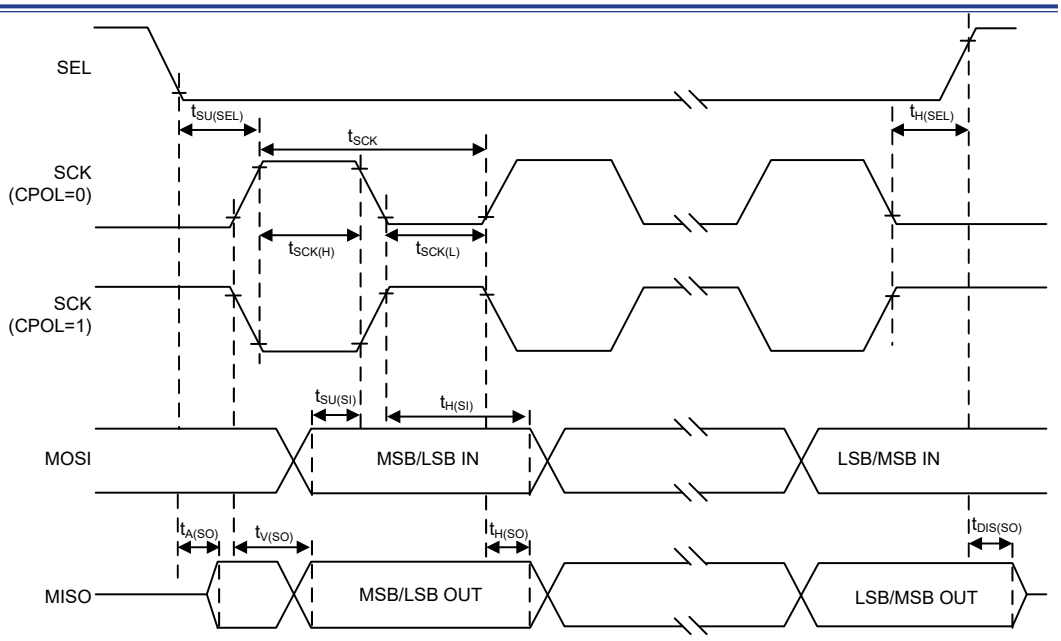


Figure 11. SPI Timing Diagram – SPI Slave Mode with CPHA = 1

USB Characteristics

The USB interface is USB-IF certified - Full Speed.

Table 22. USB DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{USB}	USB Driver Operating Voltage	—	3.0	—	3.6	V
V_{DI}	Differential Input Sensitivity	|USBDP – USBDM|	0.2	—	—	V
V_{CM}	Common Mode Voltage Range	—	0.8	—	2.5	V
V_{SE}	Single-ended Receiver Threshold	—	0.8	—	2.0	V
V_{OL}	Pad Output Low Voltage	1.5 kΩ R_L to V_{REGO}	0	—	0.3	V
V_{OH}	Pad Output High Voltage		2.8	—	3.6	V
V_{CRS}	Differential Output Signal Cross-point Voltage		1.3	—	2.0	V
Z_{DRV}	Driver Output Resistance	—	—	10	—	Ω
C_{IN}	Transceiver Pad Capacitance	—	—	—	20	pF

Note: 1. Guaranteed by design, not tested in production.
2. Owing to the on-chip USB voltage regulator output is internally connected to the USB driver, the on-chip USB voltage regulator has to be set to 3.3 V voltage output for the full USB electrical characteristics when the MCU USB functionality is active.
3. R_L is the resistor load and is internally connected to the USB driver USBDP.

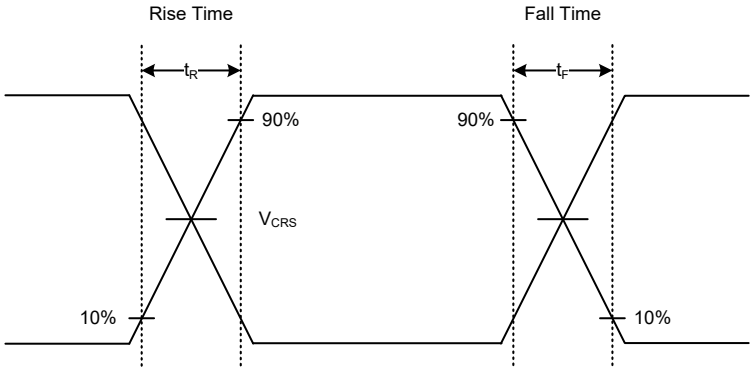


Figure 12. USB Signal Rise Time, Fall Time and Cross-point Voltage (V_{CRS}) Definitions

Table 23. USB AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_R	Rise time	C_L = 50 pF	4	—	20	ns
t_F	Fall time	C_L = 50 pF	4	—	20	ns
$t_{R/F}$	Rise time / Fall time matching	$t_{R/F} = t_R / t_F$	90	—	110	%

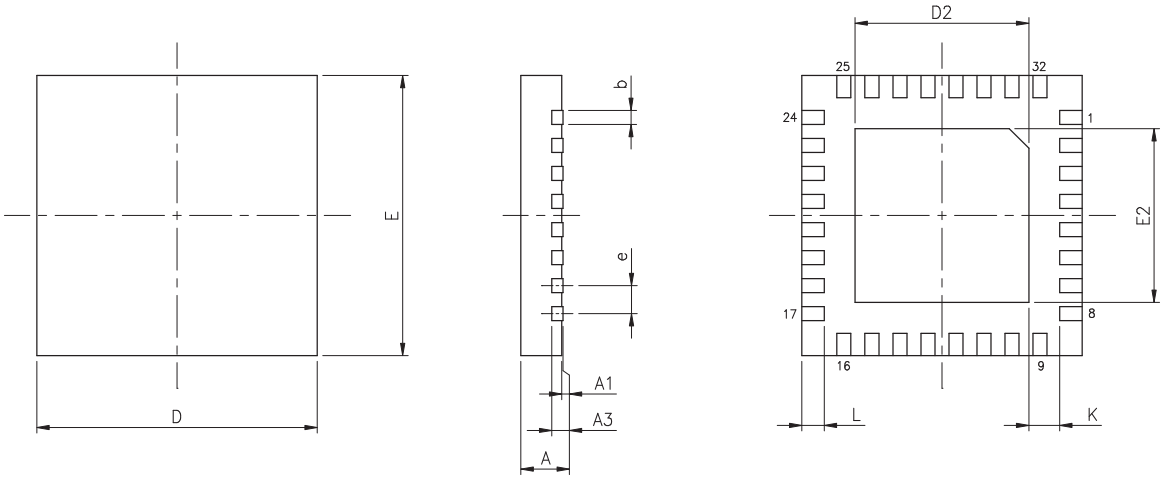
6 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

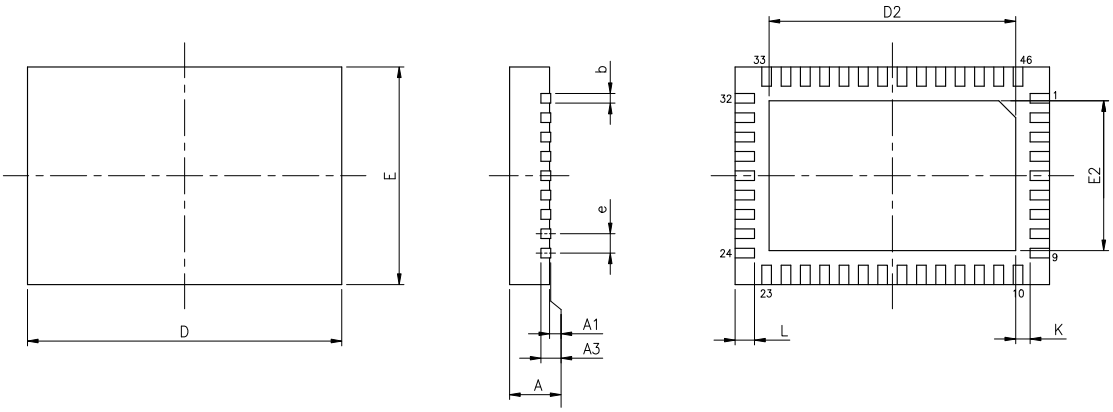
SAW Type 32-pin QFN (4mm × 4mm × 0.75mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.006	0.008	0.010
D	—	0.157 BSC	—
E	—	0.157 BSC	—
e	—	0.016 BSC	—
D2	0.104	0.106	0.108
E2	0.104	0.106	0.108
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	—	0.203 BSC	—
b	0.15	0.20	0.25
D	—	4.00 BSC	—
E	—	4.00 BSC	—
e	—	0.40 BSC	—
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
L	0.35	0.40	0.45
K	0.20	—	—

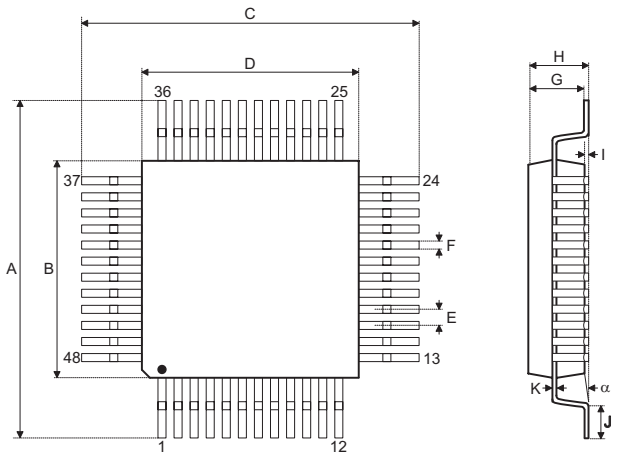
SAW Type 46-pin QFN (6.5mm × 4.5mm × 0.75mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.006	0.008	0.010
D	—	0.256 BSC	—
E	—	0.177 BSC	—
e	—	0.016 BSC	—
D2	0.199	0.201	0.203
E2	0.120	0.122	0.124
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	—	0.203 BSC	—
b	0.15	0.20	0.25
D	—	6.50 BSC	—
E	—	4.50 BSC	—
e	—	0.40 BSC	—
D2	5.05	5.10	5.15
E2	3.05	3.10	3.15
L	0.35	0.40	0.45
K	0.20	—	—

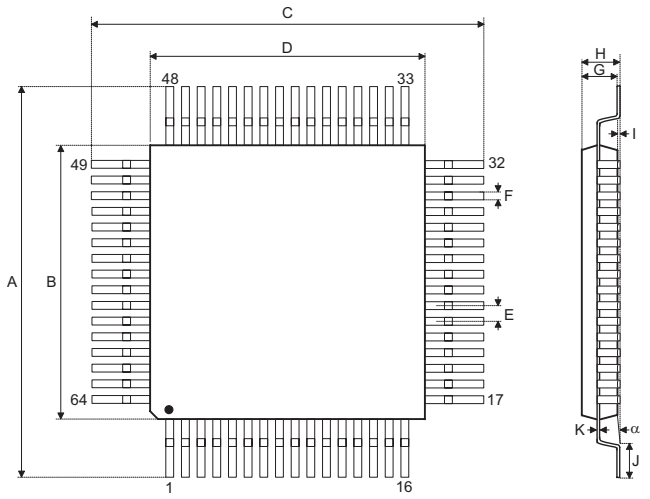
48-pin LQFP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.020 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.0 BSC	—
B	—	7.0 BSC	—
C	—	9.0 BSC	—
D	—	7.0 BSC	—
E	—	0.5 BSC	—
F	0.17	0.22	0.27
G	1.35	1.4	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

64-pin LQFP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.016 BSC	—
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.40 BSC	—
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

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