Features

- V_{IN} Input Range from 7.5V to 36V
- Accumulative Cell Voltage Monitor: 8-to-1 Analog Multiplexer with divided ratio accuracy: 1/n ± 0.5%
- Reverse-current prevention switching scan frequency of 100Hz
- Requires fewer MCU ADCs
- 5V/30mA internal Voltage Regulator with ±1% accuracy
- Operating Temperature Range: -40°C to +85°C
- Package Type: 16-pin NSOP

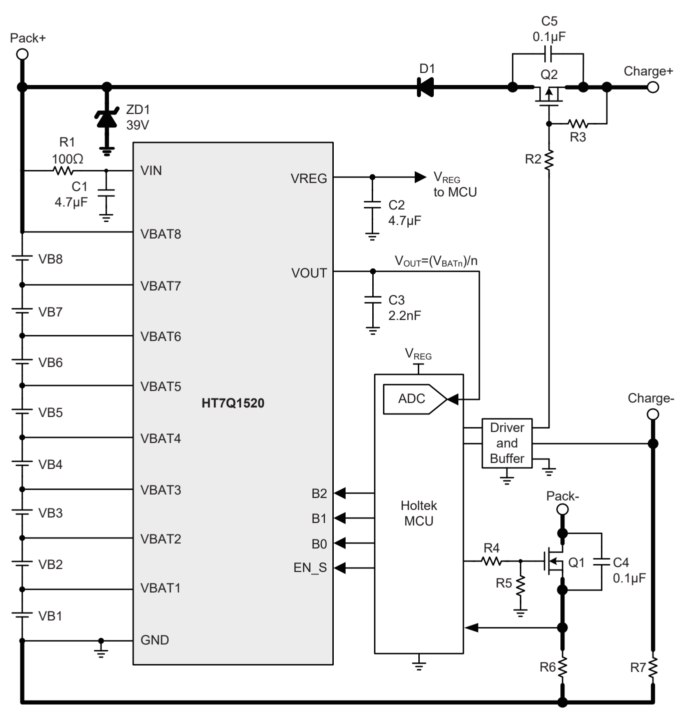
Applications

- Electric power tools
- Handheld vacuum cleaners

General Description

The HT7Q1520 is a high voltage analog-front-end IC for 3 to 8 cell Li-ion rechargeable battery protection. It consists of an accumulative cell voltage monitor and a high accuracy voltage regulator. The device is designed to monitor an accumulative voltage from 1 to N and outputs the divide-by-N voltage to the analog multiplexer with a ±0.5% divided ratio accuracy. The anti-reverse current switch is implemented to prevent a backflow current even if V_{OUT} is higher than V_{BATn}. Each divided accumulative cell voltage can be observed sequentially on pin VBATn which will benefit MCUs with a lower number of ADCs. There are 3 control bits, B0, B1 and B2, to select which terminal voltage outputs with a maximum 100Hz scanning frequency when C_{OUT}=2.2nF. The enable pin, EN_S, is used to close all switches and the output voltage is pulled down by an internal 1MΩ resistor. An integrated regulator provides a 5V supply to the MCU with a 30mA driving current capability and which has ±1% precision. The voltage regulator is always active even if the EN_S pin is cleared to a logic low level.

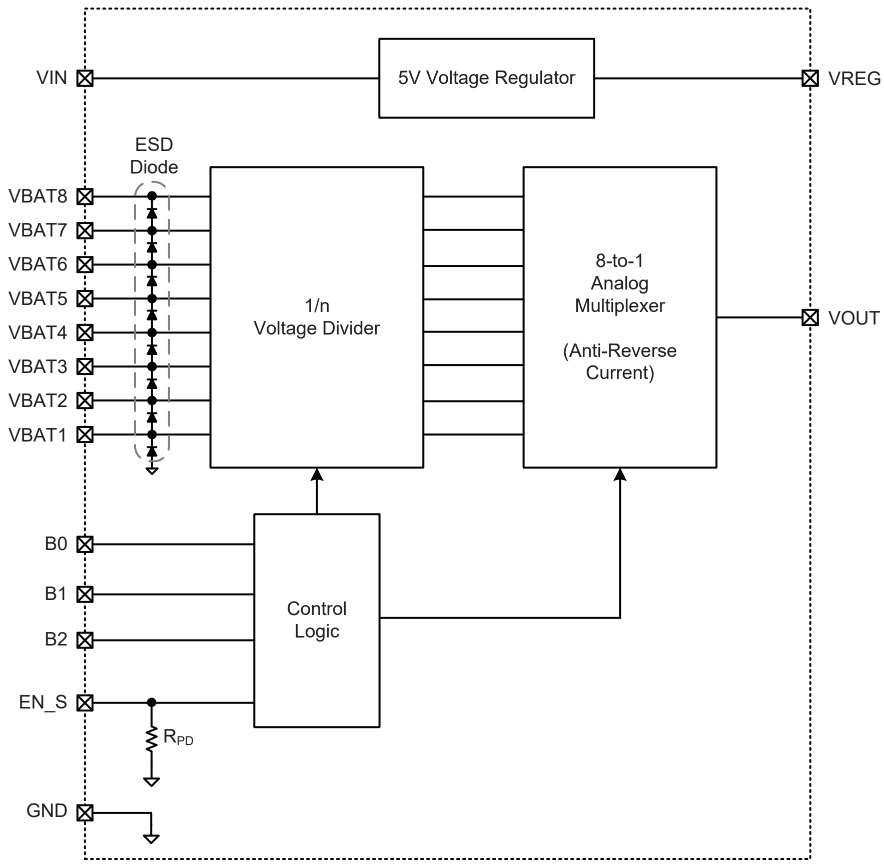
Typical Application Circuit



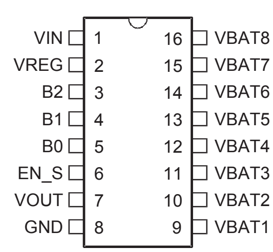
Note: 1. If less than 8 serial batteries are used, connect the unused VBATn to the highest voltage potential.

2. The bold lines indicate that these connections need to be as short as possible.

Functional Block Diagram



Pin Assignment



HT7Q1520
16 NSOP-A

Pin Description

Pin No.	Pin Name	Type	Pin Discpription
1	VIN	P	Input supply voltage. Connect to the top VBATn
2	VREG	O	Regulator 5V/30mA output. Connect a 4.7μF capacitor to GND
3	B2	I	8-to-1 analog multiplexer selection bit - MSB
4	B1	I	8-to-1 analog multiplexer selection bit
5	B0	I	8-to-1 analog multiplexer selection bit - LSB
6	EN_S	I	Enable terminal for the 8-to-1 analog multiplexer. Connected to 1MΩ internal pull low resistor
7	VOUT	O	8-to-1 analog multiplexer output. Connect a 2.2nF capacitor to GND.
8	GND	G	Ground terminal
9	VBAT1	I	Battery cell 1 positive terminal and battery cell 2 negative terminal
10	VBAT2	I	Battery cell 2 positive terminal and battery cell 3 negative terminal
11	VBAT3	I	Battery cell 3 positive terminal and battery cell 4 negative terminal
12	VBAT4	I	Battery cell 4 positive terminal and battery cell 5 negative terminal
13	VBAT5	I	Battery cell 5 positive terminal and battery cell 6 negative terminal
14	VBAT6	I	Battery cell 6 positive terminal and battery cell 7 negative terminal
15	VBAT7	I	Battery cell 7 positive terminal and battery cell 8 negative terminal
16	VBAT8	I	Battery cell 8 positive terminal

Absolute Maximum Ratings

Parameter		Value	Unit
V_{IN}		-0.3 to +40	V
V_{REG}, V_{OUT}, B2, B1, B0, EN_S, V_{BAT1}		-0.3 to +5.5	V
$\Delta[V_{BATi}\sim V_{BAT(i-1)}]$, i=8, 7, 6, 5, 4, 3, 2		-0.3 to +5.5	V
Operating Temperature Range		-40 to +85	°C
Maximum Junction Temperature		+125	°C
Storage Temperature Range		-65 to +160	°C
Lead Temperature (Soldering 10sec)		+260	°C
ESD Susceptibility	Human Body Model	±6000	V
	Machine Model	±350	V
Junction-to-Ambient Thermal Resistance, θ_{JA}	16NSOP (150mil)	100	°C/W

Recommended Operating Ratings

Parameter	Value	Unit
V_{IN}	7.5 to 36.0	V
T_A	-40 to +85	°C

Note that Absolute Maximum Ratings indicate limitations beyond which damage to the device may occur. Recommended Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specified performance limits.

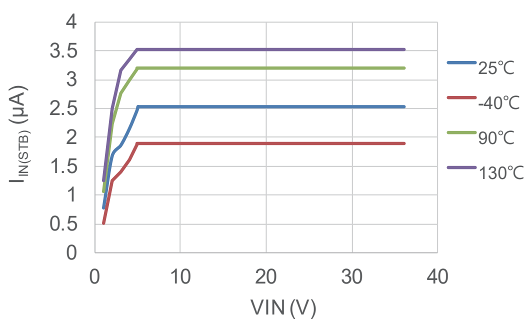
Electrical Characteristics

V_{IN}=36V, C_{REG}=4.7μF, C_{OUT}=2.2nF and T_a=25°C, unless otherwise specified.

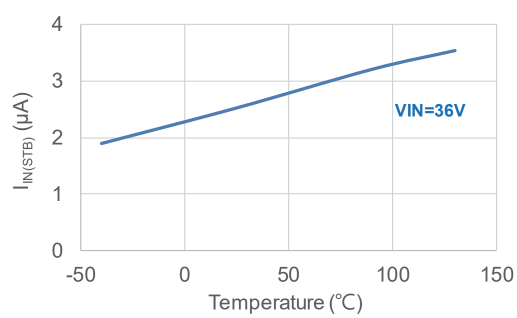
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply and Input						
V_{IN}	Supply Voltage	—	7.5	—	36.0	V
$I_{IN(SCAN)}$	Supply Current – Scan	EN_S=1, Scan B2~B0 with frequency 100Hz	—	2.5	4.0	μA
$I_{IN(STB)}$	Supply Current – Standby	B0=B1=B2=EN_S=0	—	2.5	4.0	μA
V_{Bi}	Cell Voltage Range	i=1~8	2.5	—	4.5	V
I_{Bi}	Cell Input Leakage Current	V_{BATi}=5.5V×i, EN_S=0, V_{IN}=V_{BAT8}, i=1~8	-0.1	—	0.1	μA
$I_{Bi(ACT)}$	Cell Input Current when Monitoring Voltage	V_{BATi}=4.2V×i, EN_S=1, V_{IN}=36V, i=1~8	19	24	35	μA
$I_{B1(REV)}$	VBAT1 Input Reverse Current	V_{BAT8}=36V, V_{BAT1}=2.5V, B2~B0=0b'111, Measure I_{B1}	-0.1	—	0.1	μA
Voltage Regulator						
V_{REG}	Regulator Output Voltage	I_{LOAD}=10mA	4.95	5.00	5.05	V
I_{REG}	Regulator Output Current	V_{IN}=7.5V, T_a=-40~85°C	30	—	—	mA
ΔV_{REG}	Load Regulation	I_{LOAD}=0~30mA	—	50	—	mV
$\Delta V_{REG}/(V_{REG}\times\Delta V_{IN})$	Line Regulation	V_{IN}=7.5V~36V, I_{LOAD}=10mA	—	0.02	—	%/V
$\Delta V_{REG}/(V_{REG}\times\Delta T_A)$	Temperature Coefficient	I_{LOAD}=1mA, T_a=-40~85°C	—	±100	—	ppm/°C
Accumulative Cell Voltage Monitor						
R	Divided Resistance	—	120	170	220	KΩ
$Ratio8_{(NORM)}$	VBAT8 Accumulative Cell Voltage Divided Ratio (Normalised)	V_{BAT8}=20V~36V, B2~B0=0b'111, EN_S=1	0.995	1.000	1.005	—
		V_{BAT8}=20V~36V, B2~B0=0b'111, EN_S=1, T_a=-40~85°C	0.990	1.000	1.010	—
$Ratio7_{(NORM)}$	VBAT7 Accumulative Cell Voltage Divided Ratio (Normalised)	V_{BAT7}=17.5V~31.5V, B2~B0=0b'110, EN_S=1	0.995	1.000	1.005	—
		V_{BAT7}=17.5V~31.5V, B2~B0=0b'110, EN_S=1, T_a=-40~85°C	0.990	1.000	1.010	—
$Ratio6_{(NORM)}$	VBAT6 Accumulative Cell Voltage Divided Ratio (Normalised)	V_{BAT6}=15V~27V, B2~B0=0b'101, EN_S=1	0.995	1.000	1.005	—
		V_{BAT6}=15V~27V, B2~B0=0b'101, EN_S=1, T_a=-40~85°C	0.990	1.000	1.010	—
$Ratio5_{(NORM)}$	VBAT5 Accumulative Cell Voltage Divided Ratio (Normalised)	V_{BAT5}=12.5V~22.5V, B2~B0=0b'100, EN_S=1	0.995	1.000	1.005	—
		V_{BAT5}=12.5V~22.5V, B2~B0=0b'100, EN_S=1, T_a=-40~85°C	0.990	1.000	1.010	—
$Ratio4_{(NORM)}$	VBAT4 Accumulative Cell Voltage Divided Ratio (Normalised)	V_{BAT4}=10V~18V, B2~B0=0b'011, EN_S=1	0.995	1.000	1.005	—
		V_{BAT4}=10V~18V, B2~B0=0b'011, EN_S=1, T_a=-40~85°C	0.990	1.000	1.010	—
$Ratio3_{(NORM)}$	VBAT3 Accumulative Cell Voltage Divided Ratio (Normalised)	V_{BAT3}=7.5V~13.5V, B2~B0=0b'010, EN_S=1	0.995	1.000	1.005	—
		V_{BAT3}=7.5V~13.5V, B2~B0=0b'010, EN_S=1, T_a=-40~85°C	0.990	1.000	1.010	—

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$Ratio2_{(NORM)}$	VBAT2 Accumulative Cell Voltage Divided Ratio (Normalised)	V_{BAT2}=5V~9V, B2~B0=0b'001, EN_S=1	0.995	1.000	1.005	—
		V_{BAT2}=5V~9V, B2~B0=0b'001, EN_S=1, T_a=-40~85°C	0.990	1.000	1.010	—
$Ratio1_{(NORM)}$	VBAT1 Accumulative Cell Voltage Divided Ratio (Normalised)	V_{BAT1}=2.5V~4.5V, B2~B0=0b'000, EN_S=1	0.995	1.000	1.005	—
		V_{BAT1}=2.5V~4.5V, B2~B0=0b'000, EN_S=1, T_a=-40~85°C	0.990	1.000	1.010	—
Input Logic						
f_{MAX}	B2~B0 Scan Frequency	C_{OUT} = 2.2nF	100	—	—	Hz
V_{IH}	Input Logic High Threshold	V_{IN}=7.5~36V, B2, B1, B0 and EN_S pins	2.5	—	—	V
V_{IL}	Input Logic Low Threshold	V_{IN}=7.5~36V, B2, B1, B0 and EN_S pins	—	—	0.8	V
R_{PD}	Pull Low Resistance	EN_S pin	—	1	—	MΩ
I_{LEAK}	Input Logic Leakage	V_{IN}=7.5V~36V, B2, B1 and B0 pins	—	—	0.1	μA

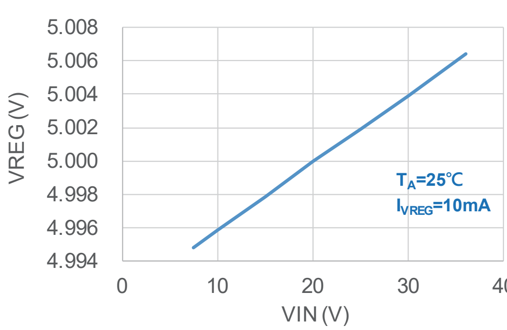
Typical Performance Characteristics



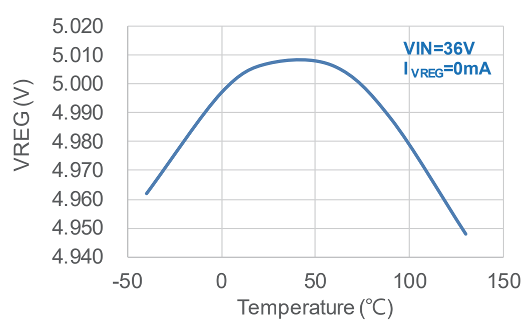
$I_{IN(STB)}$ vs. V_{IN}



$I_{IN(STB)}$ vs. Temperature

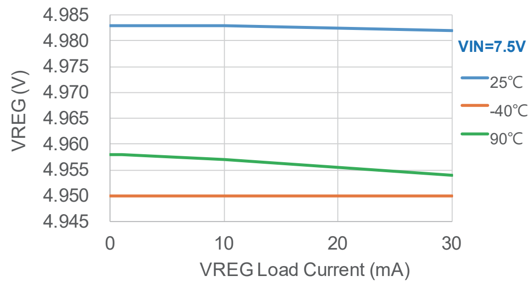


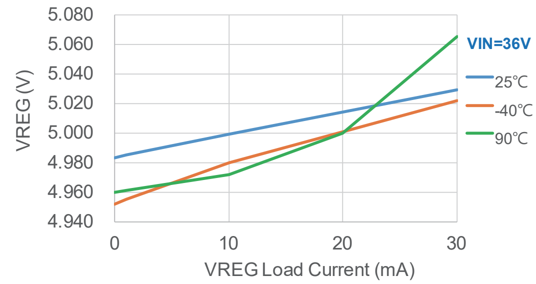
V_{REG} vs. V_{IN}



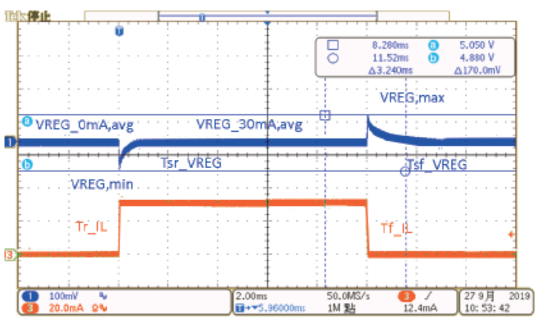
V_{REG} vs. Temperature

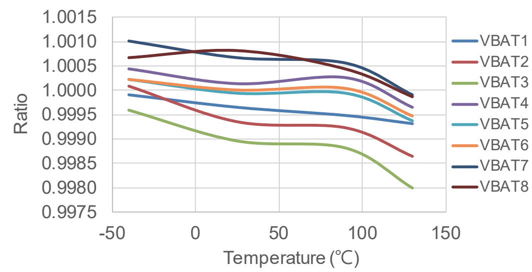
Typical Performance Characteristics (Continued)





V_{REG} vs. Load Current

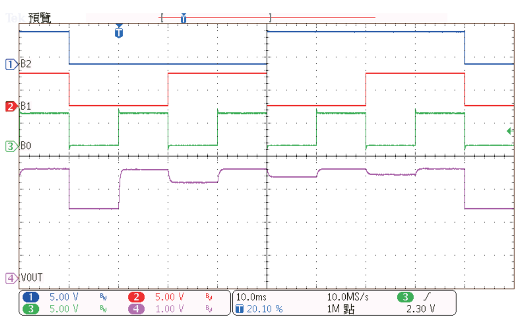




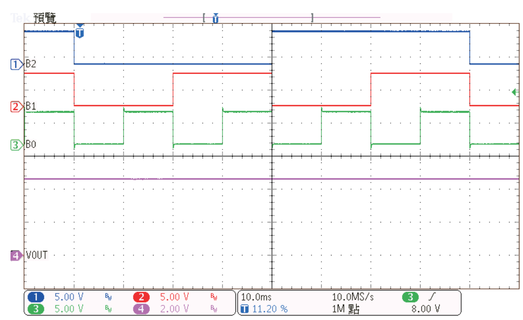
(Averaged values from 3 samples)

VREG Load Transient (0mA ⇄ 30mA)

Cell Voltage Divided Ratio vs. Temperature

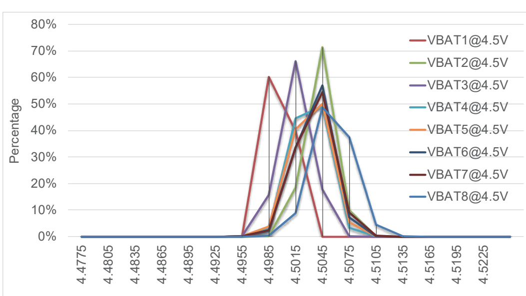


Cell Voltage from 1 to 8: 2.5V, 4.5V, 2.5V, 4.5V, 2.5V, 4.5V, 2.5V, 4.5V

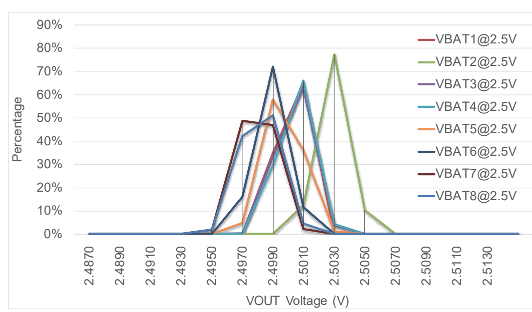


Cell Voltage from 1 to 8: all equal to 4.2V

V_{OUT} Scanning Waveform (Scan from Cell 1 to Cell 8 and Repeat)



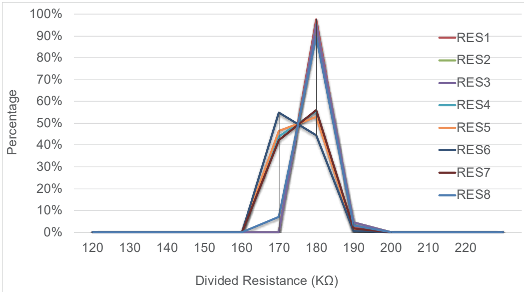
$V_{OUT(MIN)}$=4.4775V, $V_{OUT(MAX)}$=4.5225V



$V_{OUT(MIN)}$=2.4875V, $V_{OUT(MAX)}$=2.5125V

Wafer Level V_{OUT} Voltage Statistics Distribution

Typical Performance Characteristics (Continued)



R_{MIN}=120KΩ, R_{MAX}=220KΩ

Wafer Level Divided Resistance Statistics Distribution

Functional Description

Accumulative Cell Voltage Monitor

The accumulative cell voltage monitor consists of high voltage switches, voltage dividers and an 8-to-1 analog multiplexer as shown in Fig 1. The high voltage switches are implemented using an anti-reverse current topology which provides isolation between the output voltage and the unselected VBATs.

B2, B1 and B0 are used to control the p-type switches S1~S8 only if EN_S='H'. The control truth table is shown below. This produces an accumulative cell voltage, V_{BATn}, divided by "n" on V_{OUT}. This accurate ±0.5% voltage divided ratio is designed to minimise any mismatch errors.

EN_S	B2	B1	B0	S8	S7	S6	S5	S4	S3	S2	S1	V_{OUT} (V)
0	X	X	X	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1	V_{BAT1}×1/1
1	0	0	1	0	0	0	0	0	0	1	0	V_{BAT2}×1/2
1	0	1	0	0	0	0	0	0	1	0	0	V_{BAT3}×1/3
1	0	1	1	0	0	0	0	1	0	0	0	V_{BAT4}×1/4
1	1	0	0	0	0	0	1	0	0	0	0	V_{BAT5}×1/5
1	1	0	1	0	0	1	0	0	0	0	0	V_{BAT6}×1/6
1	1	1	0	0	1	0	0	0	0	0	0	V_{BAT7}×1/7
1	1	1	1	1	0	0	0	0	0	0	0	V_{BAT8}×1/8
Power on states				0	0	0	0	0	0	0	0	0

Table 1: Accumulative Cell Voltage Monitor Truth Table

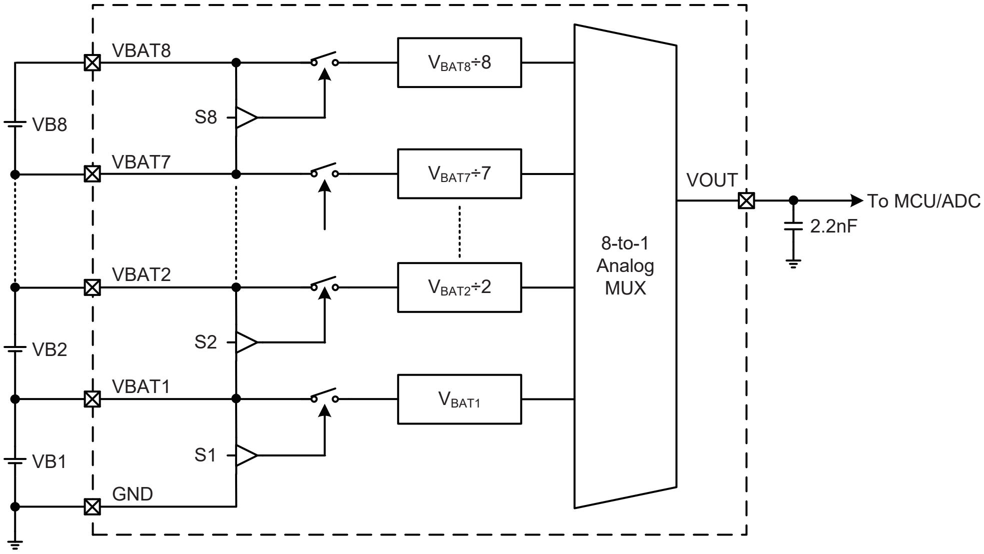
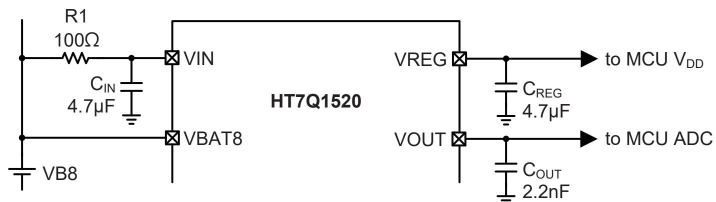


Fig 1. Accumulative Cell Voltage Monitor Functional Block

Application Information



VIN, VREG, VOUT Capacitors

The VIN input capacitor C_{IN} and VREG output capacitor C_{REG} are recommended to have a value of 4.7μF respectively and for better input noise filtering and output load transient behavior. A recommended 2.2nF noise filtering capacitor should be connected between VOUT and GND terminals. Note that higher noise capacitance value of C_{OUT} will lower the acceptable scan frequency.

VIN Input Resistor

The VIN input resistor and capacitor lower the voltage spike applied on the V_{IN} and can improve the stability of V_{REG} that provides power source to external MCUs. The recommended resistance value of VIN input resistor is 50Ω in 3-cell applications and 100Ω in 4 to 8-cell applications.

Cell Voltage Monitor Scan Frequency

The HT7Q1520 device can output accumulative cell voltage to external MCU/ADC for monitoring battery voltage status. The Fig2 and Fig3 show the timing diagrams of cell voltage monitor scanning for 5S and 8S applications. The HT7Q1520 starts to charge the VOUT capacitor from 0V to the selected cell voltage when the EN_S receives an 'L' to 'H' signal. In order to insure the external MCU A/D conversion accuracy, the A/D conversion procedure has to wait before the HT7Q1520's VOUT capacitor is fully charged. The suggested minimum waiting time is 5ms after EN_S rises from 'L' to 'H' or cell voltage monitor channel is switched. It is recommended that the maximum scan frequency for accumulative cell voltage monitoring is less than 100Hz and that EN_S='0' when the voltage scanning procedure has finished for power saving purposes.

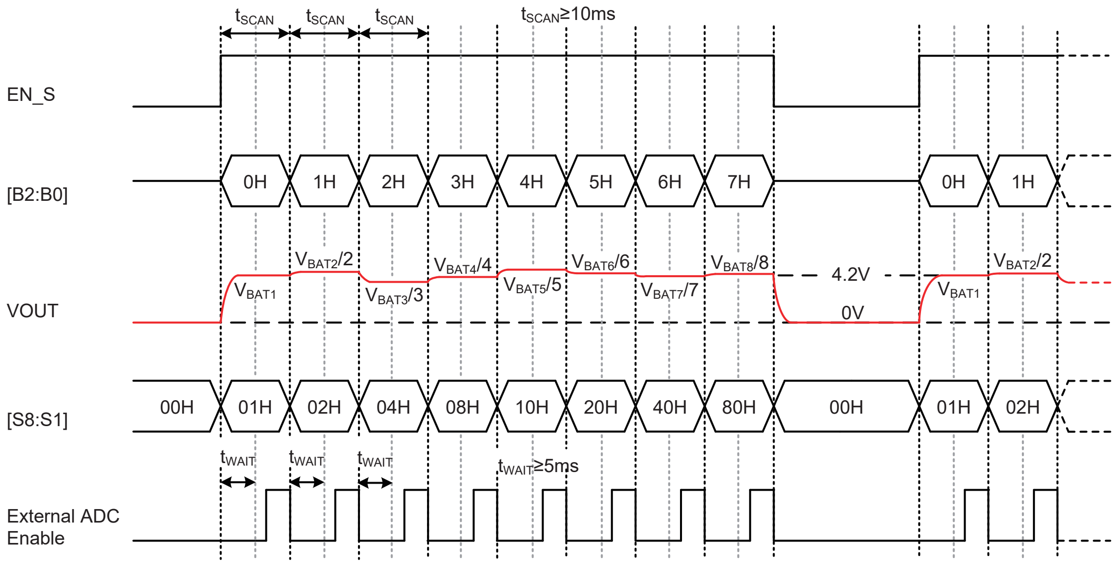


Fig 2. 8S Battery Monitoring Timing

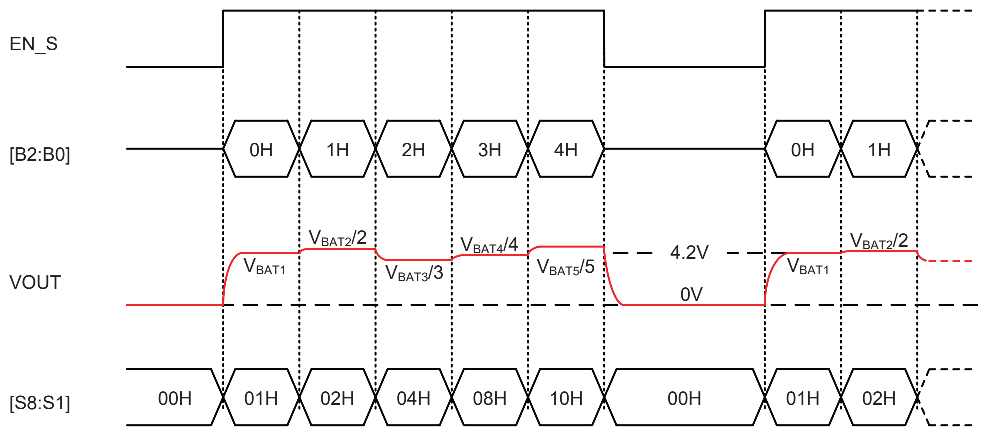


Fig 3. 5S Battery Monitoring Timing

Acquiring Cell Voltage Monitor Output with External MCU ADC

The HT7Q1520 could output the battery cell voltage to an external MCU for monitoring the battery status when it is in charging or discharging state. As shown in Fig.4, the external MCU ADC samples the V_{OUT} voltage via an ADC sampling capacitor (C_{SAMPLE}), which is typically 5pF to 50pF. Due to the charge sharing effect, the voltage on the VOUT capacitor (C_{OUT}) drops while the ADC samples that with the initially zero-voltage C_{SAMPLE}. A voltage-drop occurs on the C_{OUT} after the first ADC sampling, and then it needs a recharge time to recharge the C_{OUT}. Referring to Fig.5, a pre-charge procedure of C_{SAMPLE} during the VOUT capacitor recharge time is recommended to minimize the charge sharing effect by means of performing several sampling without clearing the charges in the C_{SAMPLE}.

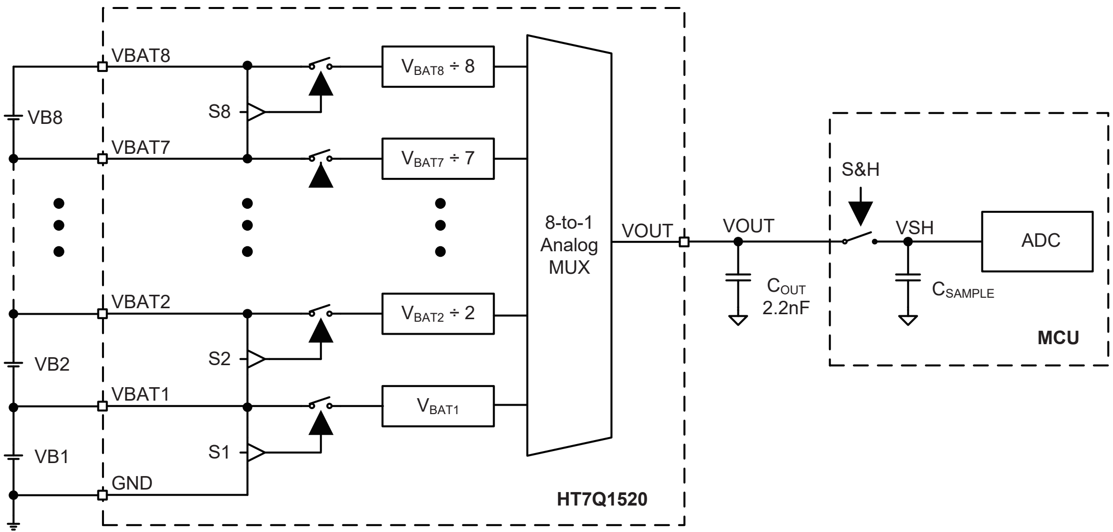


Fig 4. HT7Q1520 + MCU/ADC Functional Block

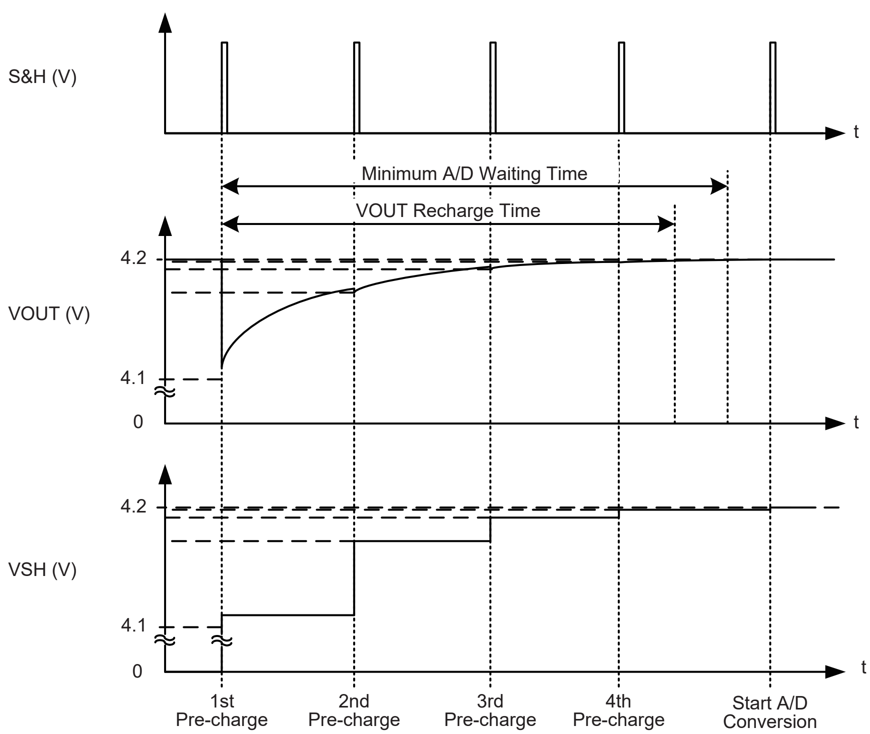


Fig 5. ADC Sampling Recommended Timing

For the best conversion accuracy, the A/D conversion has to wait before the C_{OUT} recharge is complete. The recommended minimum waiting time from the first sampling to A/D conversion beginning is listed in Table2.

MCU/ADC Sampling Capacitance (pF)	5	10	20	30	40	50
Recommended minimum A/D waiting time (μs)	370	660	950	1120	1240	1340

Table 2. ADC Recommended Waiting Time

Voltage Spike Suppression on VBATn and VIN

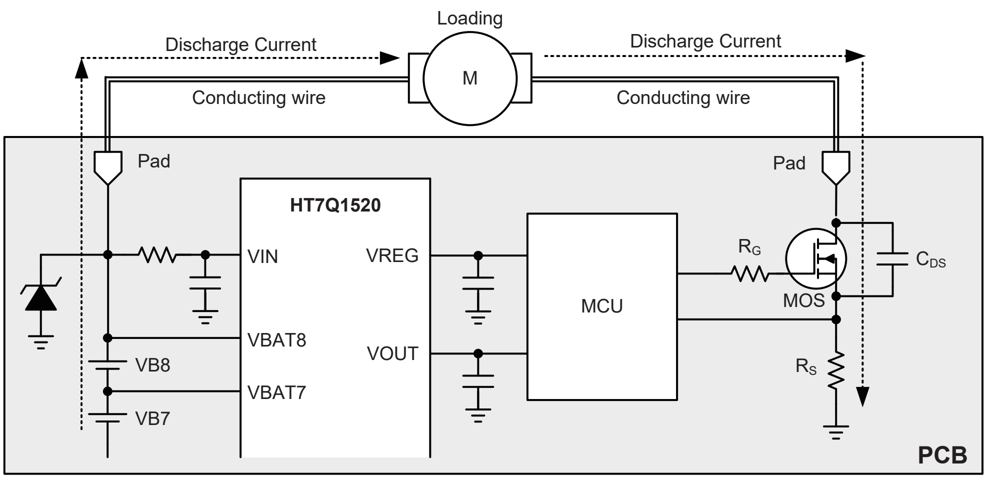


Fig 6. Simplified Typical BMS System Discharge Path Diagram

Most battery-management systems would monitor charge and discharge current to prevent over-current damage. Due to the parasitic inductance on conducting wires and PCB layout connections, a large voltage spike may occur while the MCU-controlled MOS rapidly shuts down the charge or discharge current, and this spike may damage HT7Q1520 VBATn or VIN pins. Any voltage spike on the VBATn and VIN pins should not over the limitation in Absolute Maximum Ratings, which is 40V. Four recommended measures listed below would help to reduce the voltage spike.

1. Ensure that the external conducting wires and PCB layout connections where large charge or discharge current flows are as short as possible.
2. Adjust the slew rate of MOS switch with the Gate resistor R_G. Turn off the MOS switch with a slower slew rate can lower voltage spike, however the trade off is a slower protection response time.
3. Add a capacitor (C_{DS}) between the drain and source nodes of the MOS switch as shown in Fig6. The recommended capacitance is 0.1μF to 0.22μF.
4. Add a 39V Zener diode between the highest voltage potential node of the battery cells and GND.

PCB Layout Considerations

The following placement/layout guidelines are suggested for the sake of noise reduction and voltage spike suppression.

1. The VIN filter capacitor and resistor must be placed close to the VIN pin. [Region (A)]
2. The VREG regulation and noise filter capacitor must be placed close to the VREG pin. [Region (B)]
3. The VOUT noise filter capacitor must be placed close to the VOUT pin. [Region (C)]
4. Placing a ground line between VIN and VREG lines would improve the ability of resisting surge. [Region (D)]
5. The tracks where large current would flow through should be wide and short to suppress the voltage spike at the time when MOS switch changes its ON/OFF state.
6. The power ground and signal ground should be connected at final output pad (B-) for less noise disturbance. [Region (E)]

Evaluation Board

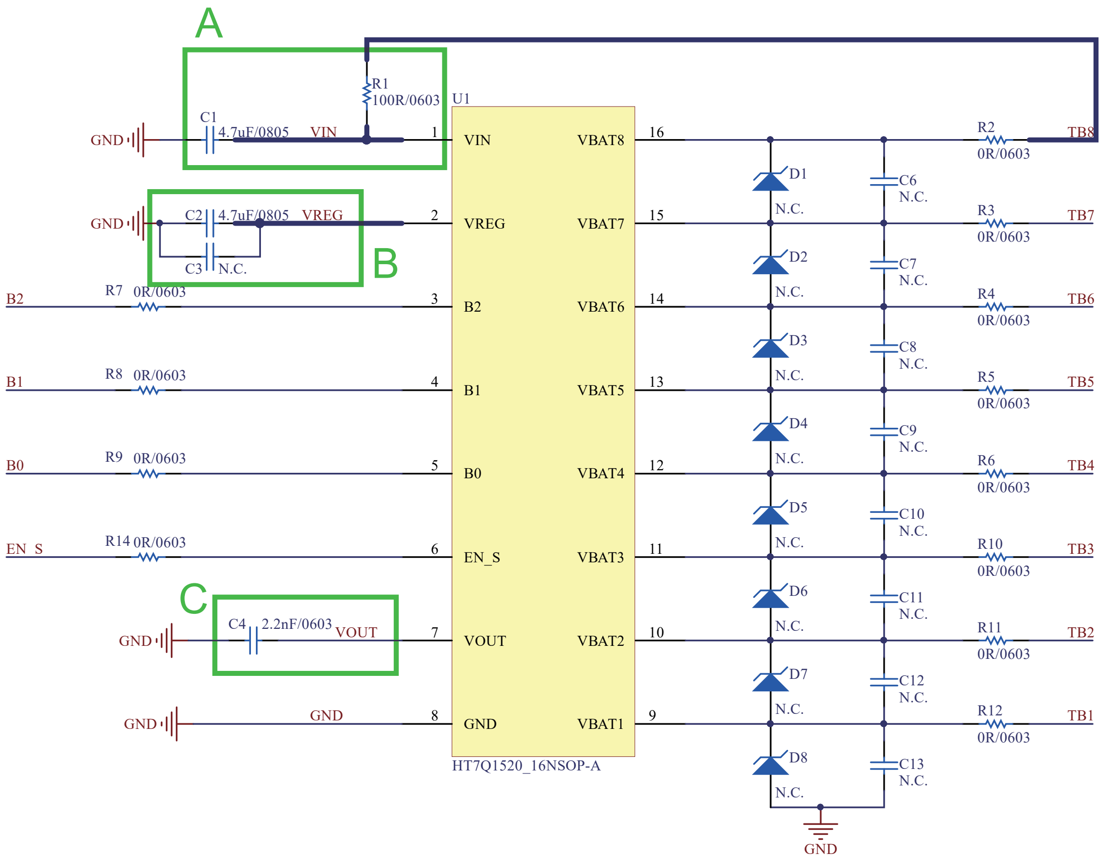


Fig 7. HT7Q1520 Evaluation Board Schematic

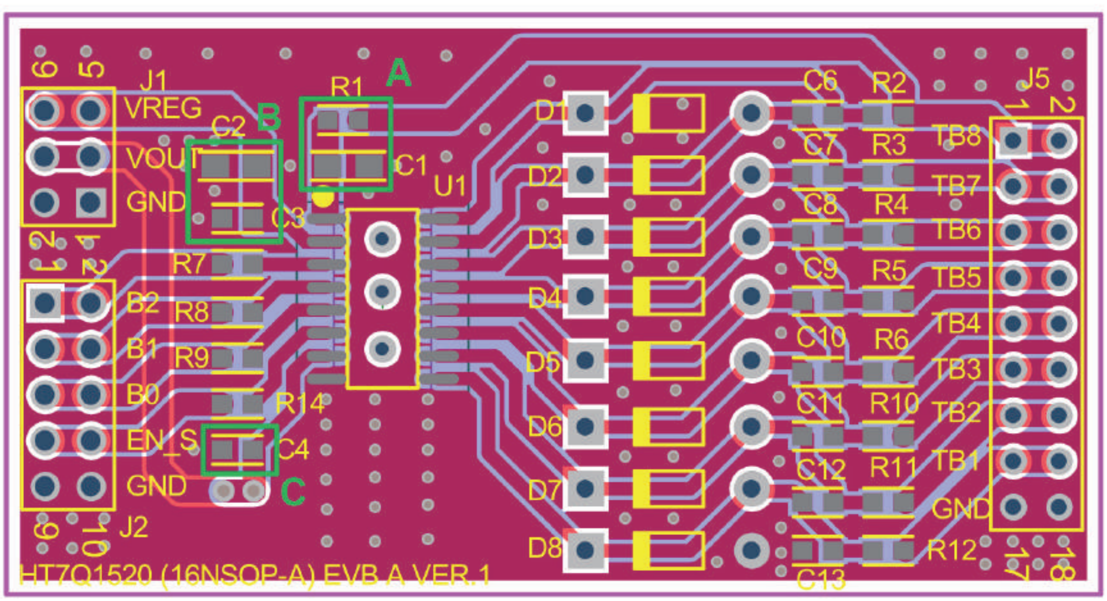


Fig 8. HT7Q1520 Evaluation Board Layout

Reference 6S Battery Management System Board

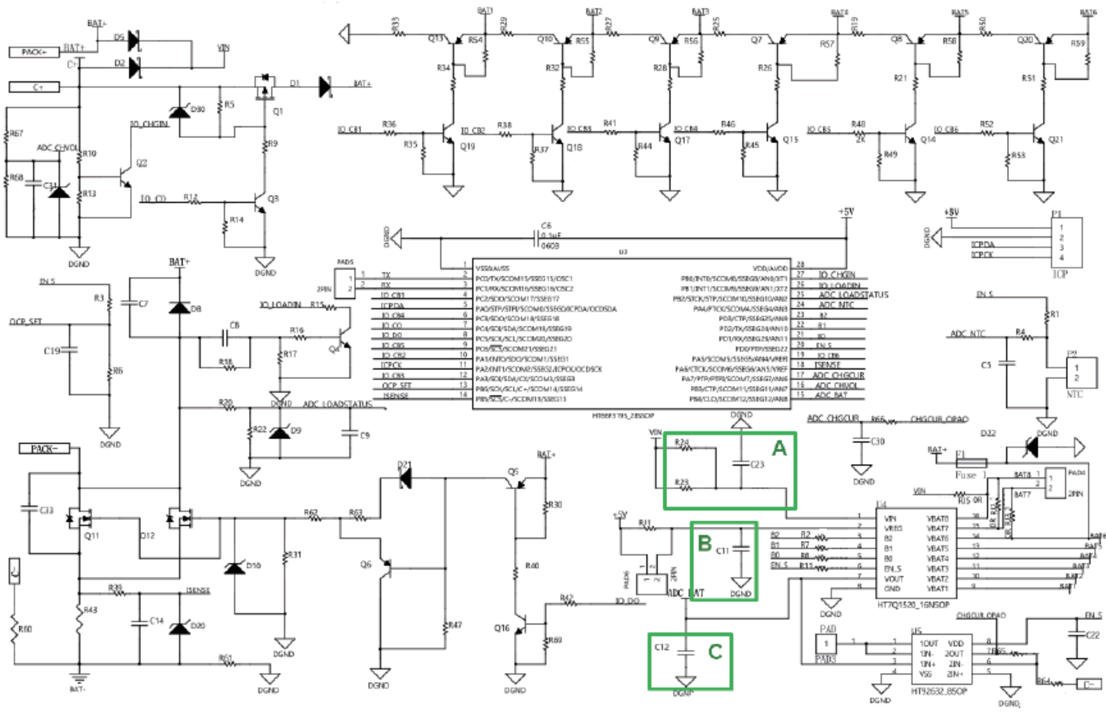


Fig 9. Reference HT7Q1520 6S BMS System Schematic

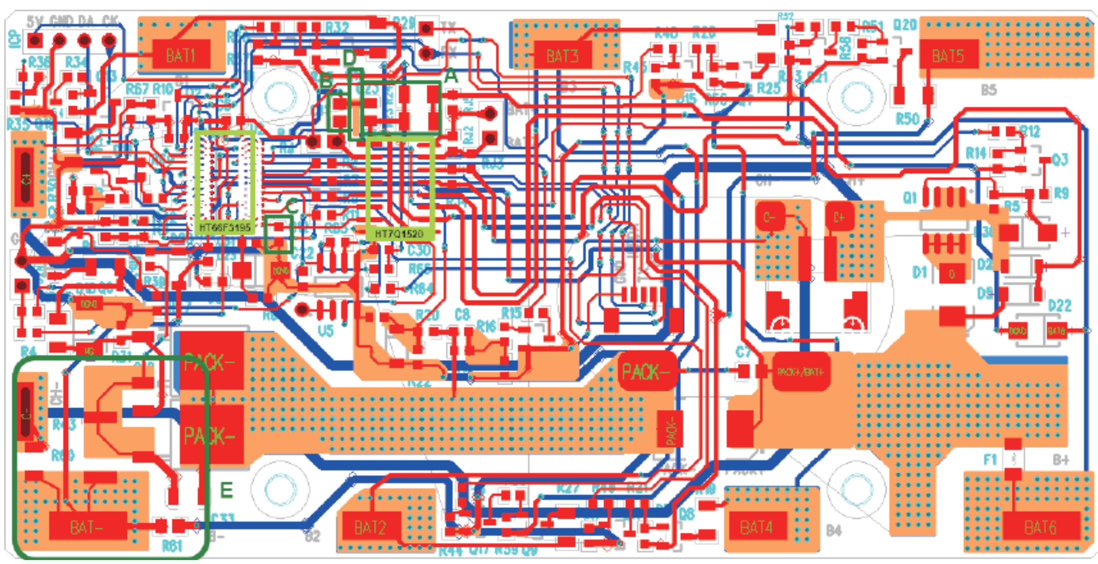


Fig 10. Reference HT7Q1520 6S BMS System PCB Layout

Thermal Consideration

The maximum power dissipation depends upon the thermal resistance of the IC package, PCB layout, rate of surrounding airflow and difference between the junction and ambient temperature. The maximum power dissipation can be calculated using the following formula:

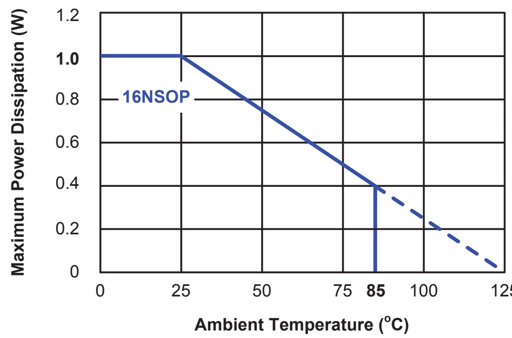
$$P_{D(MAX)} = (T_{J(MAX)} - T_a) / \theta_{JA} \quad (W)$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_a is the ambient temperature and θ_{JA} is the junction-to-ambient thermal resistance of the IC package.

For maximum operating rating conditions, the maximum junction temperature is 125°C. However, it is recommended that the maximum junction temperature does not exceed 125°C during normal operation to maintain high reliability. The de-rating curve of the maximum power dissipation is shown below:

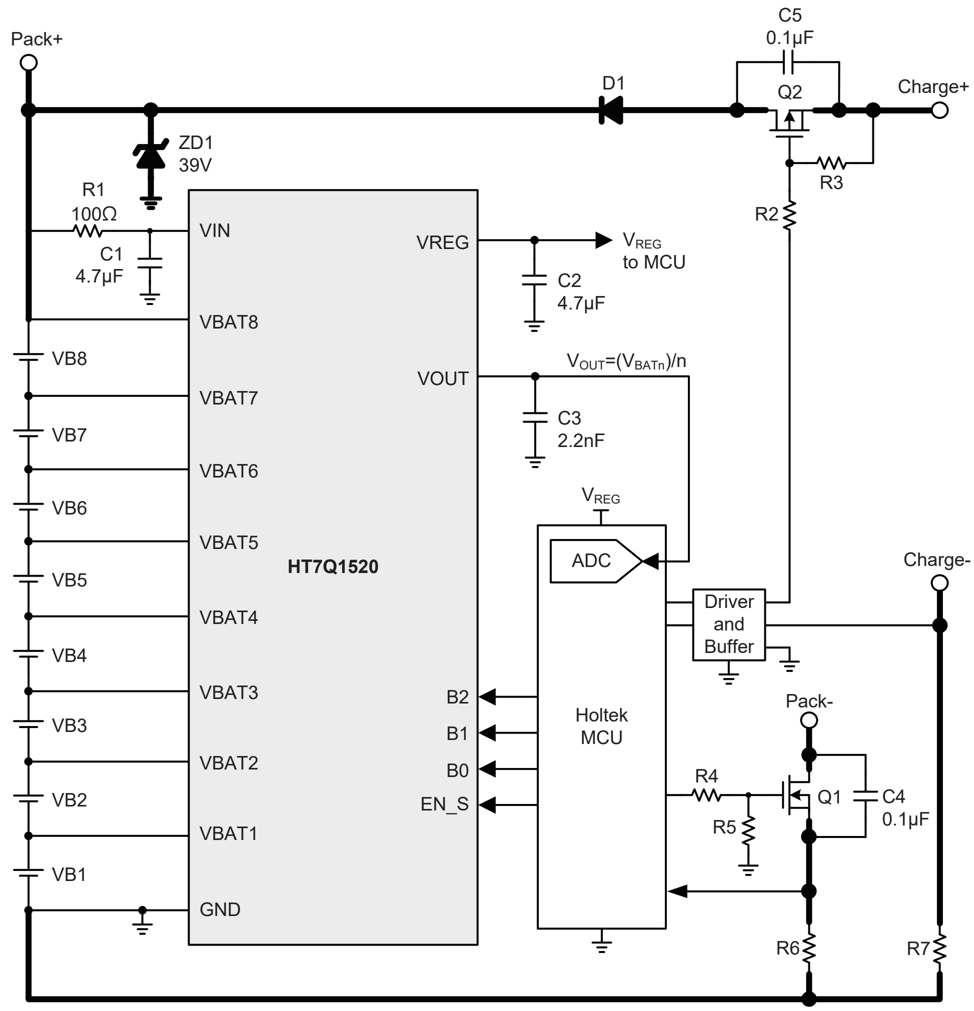
$$P_{D(MAX)} = (125^{o}C - 25^{o}C) / (100^{o}C/W) = 1.0W \quad (16NSOP)$$

For a fixed $T_{J(MAX)}$ of 125°C, the maximum power dissipation depends upon the operating ambient temperature and the package's thermal resistance, θ_{JA}. The de-rating curve below shows the effect of rising ambient temperature on the maximum recommended power dissipation.

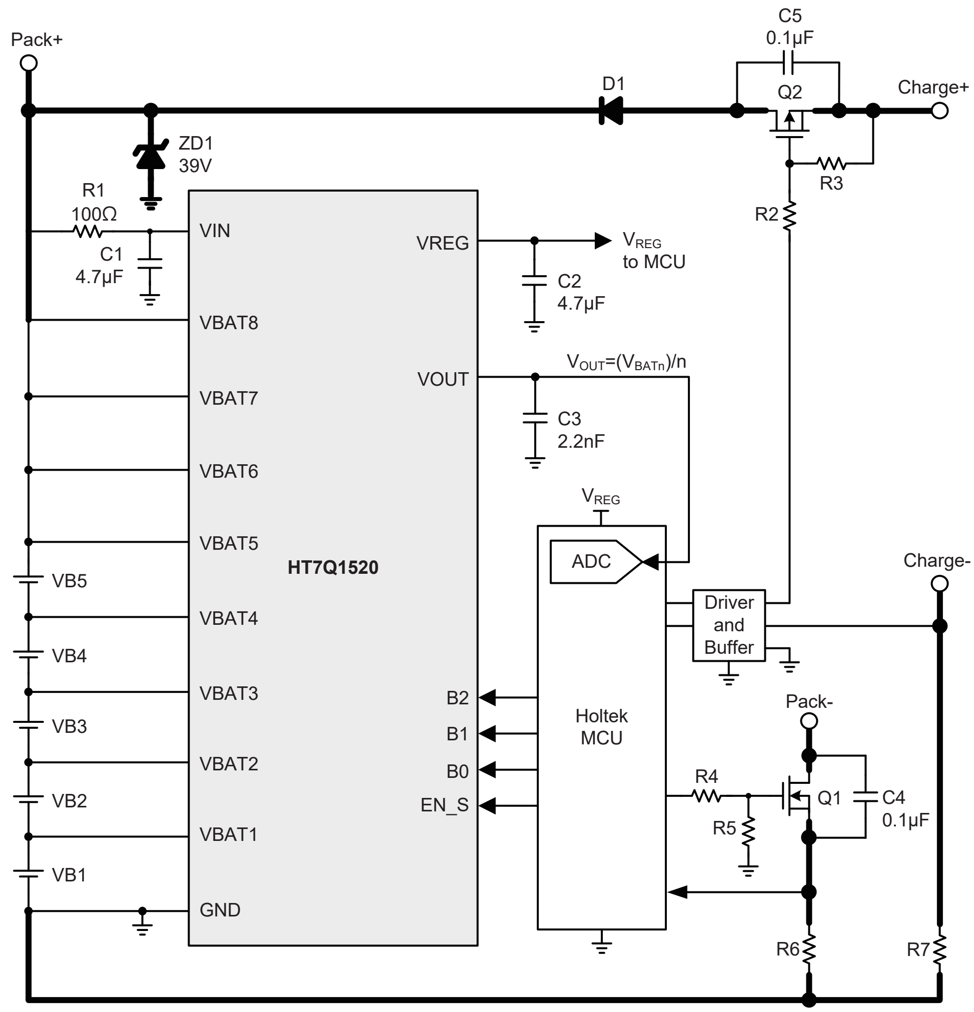


Application Circuits

8S Battery Monitoring Typical Application Circuit



5S Battery Monitoring Typical Application Circuit



Note: If less than 8 serial batteries are used, connect the unused VBATn to the highest voltage potential. Do not leave any VBATn floating to prevent damage to the device.

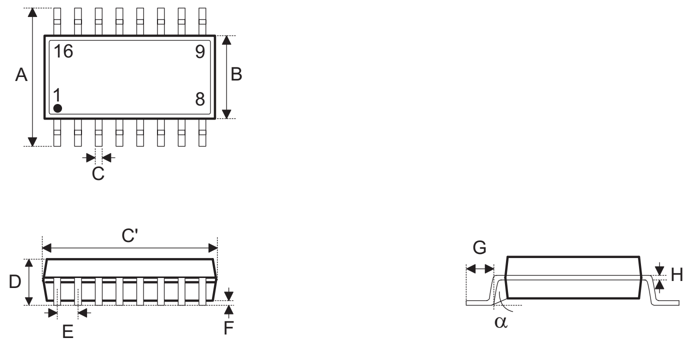
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the package information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

16-pin NSOP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.012	—	0.020
C'	—	0.390 BSC	—
D	—	—	0.069
E	—	0.050 BSC	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.000 BSC	—
B	—	3.900 BSC	—
C	0.31	—	0.51
C'	—	9.900 BSC	—
D	—	—	1.75
E	—	1.270 BSC	—
F	0.10	—	0.25
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°