# HT16L23
# RAM Mapping 52×4 / 48×8 LCD Driver

## Feature

- Logic operating voltage: 1.8V~5.5V
- LCD operating voltage ($V_{LCD}$): 2.4V~6.0V
- Internal 32kHz RC oscillator
- Bias: 1/3 or 1/4; Duty: 1/4 or 1/8
- Internal LCD bias generation with voltage-follower buffers
- External VLCD pin to supply LCD operating voltage
- Integrated regulator to adjust LCD operating voltage: 3.0V, 3.2V, 3.3V, 3.4V, 4.4V, 4.5V, 4.6V, 5.0V
- Integrated LED driver
- Support $I^2C$ or SPI 3-wire serial interface controlled by IFS pin
- Four selectable LCD frame frequencies: 64Hz or 85.3Hz or 128Hz or 170.6Hz
- Up to 48×8 bits RAM for display data storage
- Display pixel:
  - 52×4 pixel: 52 segments and 4 commons
  - 48×8 pixel: 48 segments and 8 commons
- Support two driver output mode segment/LED on SEG44~SEG51/LED7~LED0
- Versatile blinking modes: off, 0.5Hz, 1Hz, 2Hz
- R/W address auto increment
- Low power consumption
- Manufactured in silicon gate CMOS process
- Package type: 64-pin LQFP

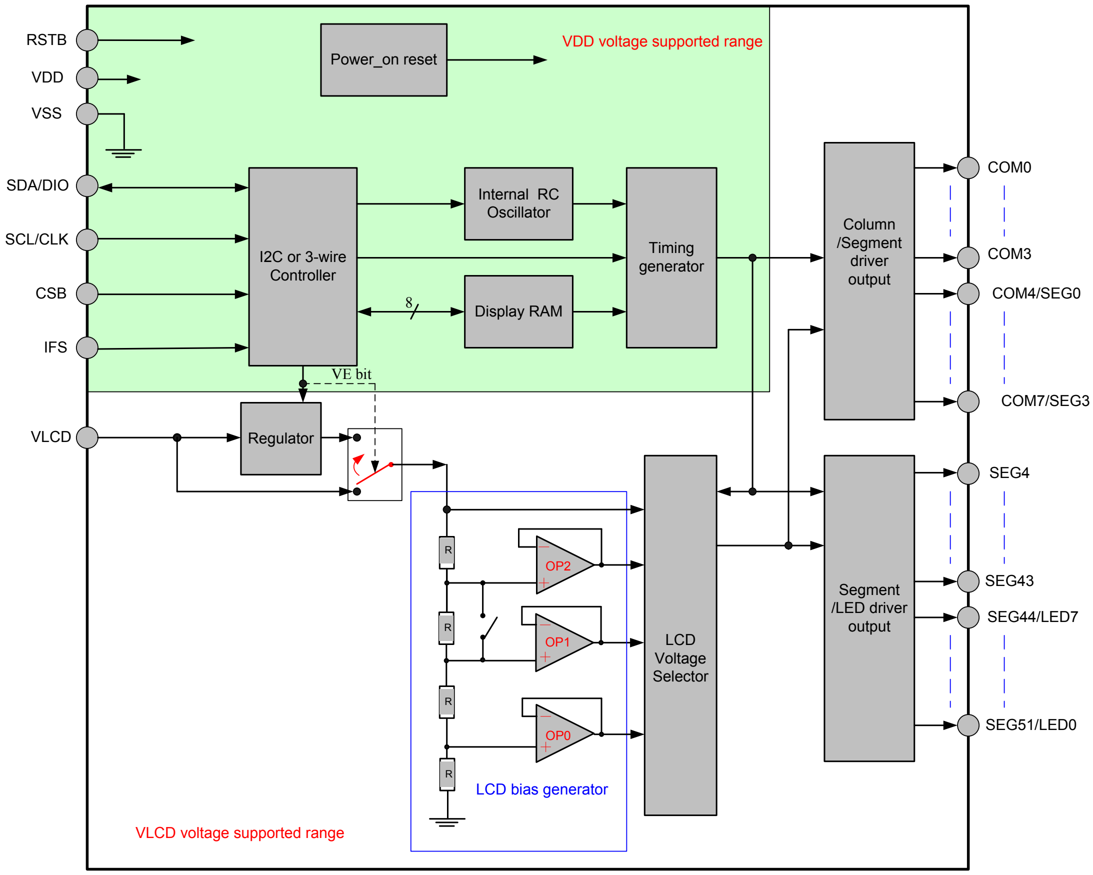
## Applications

- Leisure products
- Games
- Telephone display
- Audio combo display
- Video player display
- Kitchen appliance display
- Measurement equipment display
- Household appliance
- Consumer electronics

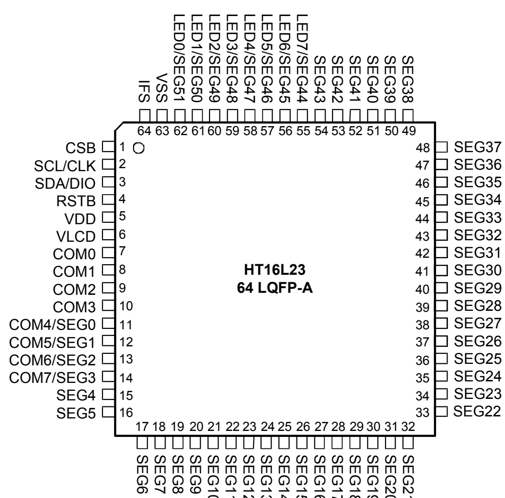
## General Description

The HT16L23 device is a memory mapping and multi-function LCD controller/driver. The display segments of the device are 208 patterns (52 segments and 4 commons) for 1/4 duty display or 384 patterns (48 segments and 8 commons) for 1/8 duty display. It can also support LED drive outputs on certain segment pins. The software configuration feature of the HT16L23 device makes it suitable for multiple LCD applications including LCD modules and display subsystems. The HT16L23 device communicates with most microprocessors/microcontrollers via a two-wire bidirectional $I^2C$ or a three-wire SPI interface.

## Block Diagram



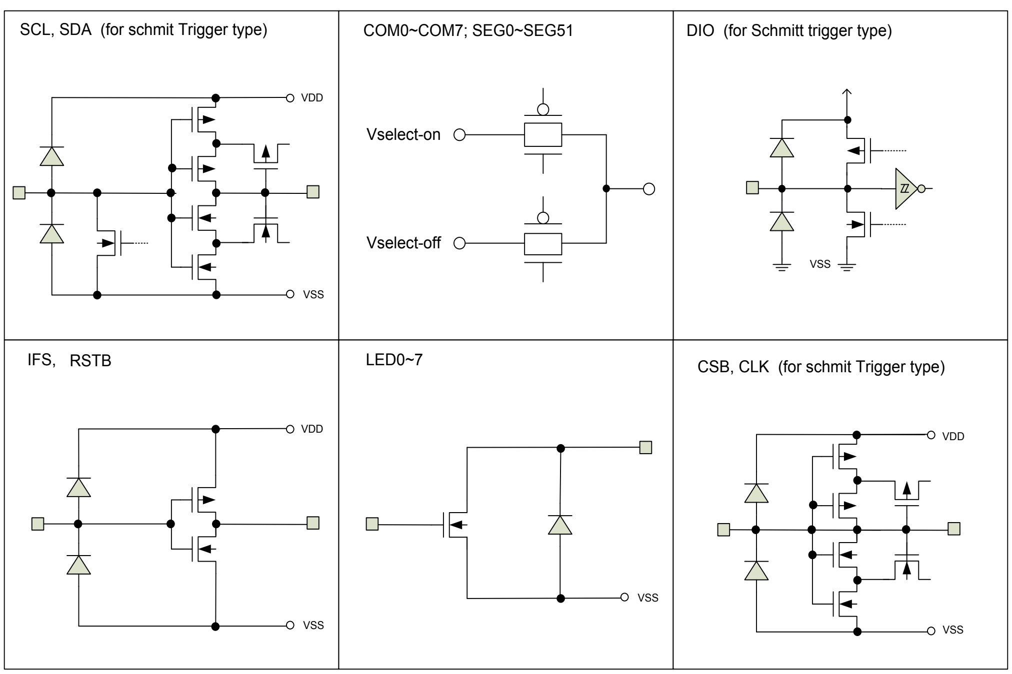

## Pin Assignment



## Pin Description

| Pin Name | Type | Description |
|---|---|---|
| SDA/DIO | I/O | Serial data input/output pin<br>• Serial data (SDA) input/output for 2-wire I²C interface is an NMOS open drain structure.<br>• Serial data (DIO) input/output for 3-wire SPI interface is a CMOS input/output structure. |
| SCL/CLK | I | Serial clock input pin<br>• Serial data (SCL) is clock input for 2-wire I²C interface.<br>• Serial data (CLK) is clock input for 3-wire SPI interface. |
| CSB | I | Chip select pin<br>This pin is available for 3-wire SPI interface and not used for I²C interface. |
| IFS | I | Communication interface select pin<br>This pin is used to select the communication interface. When this pin is connected to VDD, the device communicates with MCU or microprocessors via a 2-wire I²C interface. When this pin is connected to VSS, the device communicates with MCU or microprocessors suing a 3-wire SPI interface. |
| COM0~COM3 | O | LCD common outputs. |
| COM4/SEG0~COM7/SEG3 | O | LCD common/segment multiplexed driver outputs. |
| SEG4~SEG43 | O | LCD segment outputs. |
| SEG44/LED7~SEG51/LED0 | O | LCD segment/LED multiplexed driver outputs. |
| RSTB | I | Reset input pin<br>1. This pin is used to initialize all the internal registers and the commands pin.<br>2. If use internal power on reset circuit only, the RSTB pin must be connected to $V_{DD}$. |
| VDD | — | Positive power supply. |
| VSS | — | Negative power supply, ground. |
| VLCD | — | LCD power supply pin |

## Approximate Internal Connections



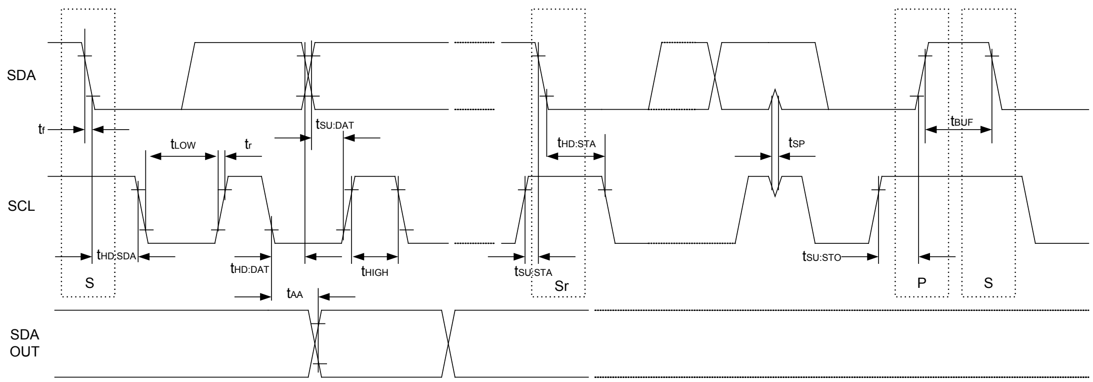
## Absolute Maximum Ratings

Supply voltage ........................................ $V_{SS}$−0.3V to $V_{SS}$+6.6V
Input voltage ........................................ $V_{SS}$−0.3V to $V_{DD}$+0.3V
LED driver output current (total)........................................ 88mA
Storage temperature ........................................-55°C to +150°C
Operating temperature ........................................-40°C to +85°C

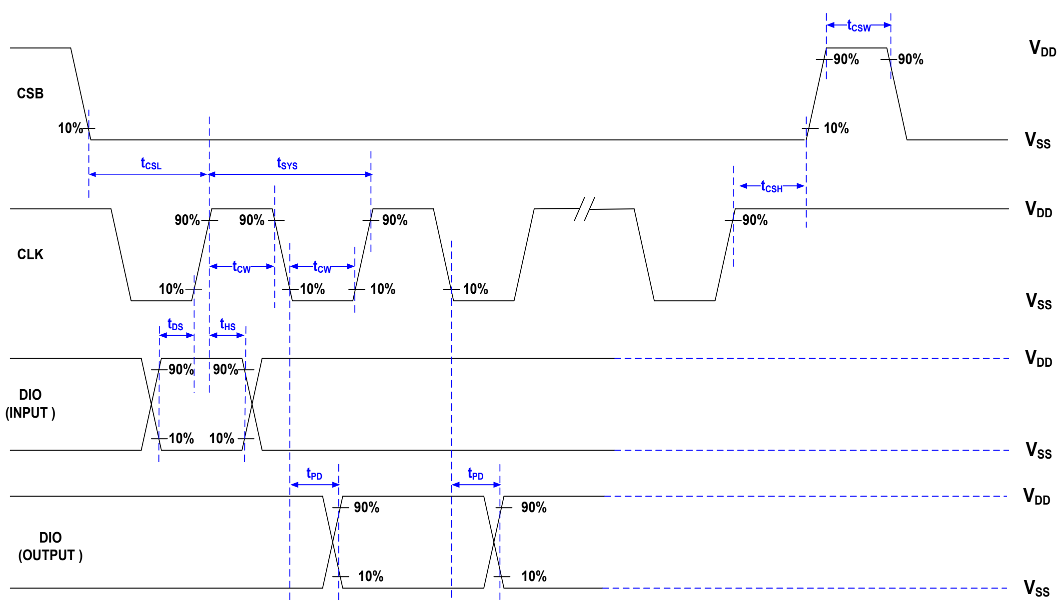
Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

## Timing Diagrams

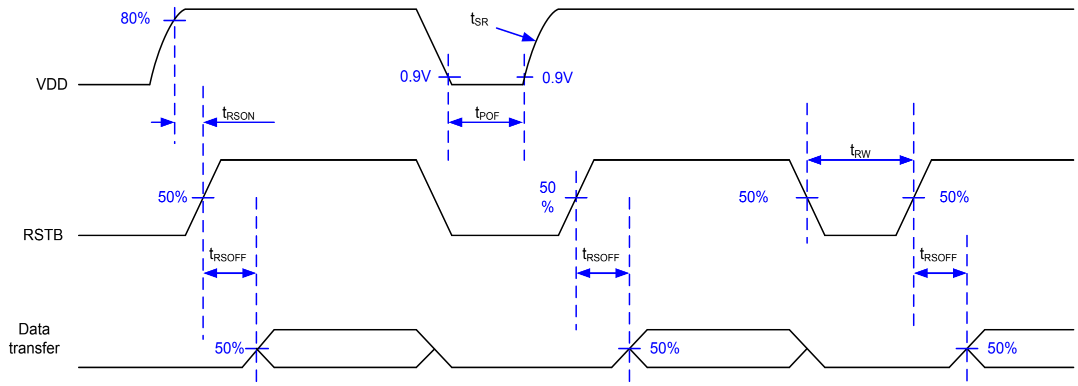
### I²C Timing




### SPI Timing



### Reset Timing




Note: 1. If the conditions of reset timing are not satisfied in power ON/OFF sequence, the internal power on reset (POR) circuit will not operate normally.

2. If the $V_{DD}$ drops lower than the minimum operating voltage during operating, the conditions of power on reset timing must also be satisfied. That is the $V_{DD}$ drop to 0.9V and keep at 0.9V for 10ms (min.) before rising to the normal operating voltage.

3. Data transfers on the I²C or SPI 3-wire serial interface should at least be delayed for 1ms after the power-on sequence to ensure that the reset operation is complete.

## D.C. Characteristics

Unless otherwise specified, $V_{SS}$ = 0V; $V_{DD}$ = 1.8 to 5.5V; Ta =-40~85°C

| Symbol | Parameter | Test Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ | Condition | | | | |
| $V_{DD}$ | Operating Voltage | — | — | 1.8 | — | 5.5 | V |
| $V_{LCD}$ | LCD Operating Voltage | — | — | 2.4 | — | 6.0 | V |
| $V_{IH}$ | Input High Voltage | — | CSB, CLK, DIO, RSTB | $0.7V_{DD}$ | — | $V_{DD}$ | V |
| $V_{IL}$ | Input Low Voltage | — | CSB, CLK, DIO, RSTB | 0 | — | $0.3V_{DD}$ | V |
| $I_{IL}$ | Input Leakage Current | — | $V_{IN}$=$V_{SS}$ or $V_{DD}$ | -1 | — | 1 | μA |
| $I_{OH}$ | High Level Output Current | 2.0V | $V_{OH}$=$0.9V_{DD}$, DIO | -2 | — | — | mA |
| | | 3.3V | | -6 | — | — | mA |
| | | 5.0V | | -12 | — | — | mA |
| $I_{OL}$ | Low Level Output Current | 2.0V | $V_{OL}$=0.4V, SDA, DIO | 3 | — | — | mA |
| | | 3.3V | | 6 | — | — | mA |
| | | 5.0V | | 9 | — | — | mA |
| $I_{DD}$ | Operating Current | 2.0V | No load, $f_{LCD}$=64Hz, 1/3bias LCD display on, internal system oscillator on, $V_{LCD}$ pin input voltage =5V, disable integrated regulator | — | 1 | 2.5 | μA |
| | | 3.3V | | — | 2 | 5 | μA |
| | | 5.0V | | — | 4 | 10 | μA |

| Symbol | Parameter | Test Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ | Condition | | | | |
| $I_{LCD1}$ | Operating Current | 2.0V | No load, $f_{LCD}$=64Hz, 1/3bias, LCD display on, internal system oscillator on, $V_{LCD}$ pin input voltage=5V, disable integrated regulator | — | 25 | 40 | μA |
| $I_{LCD2}$ | Operating Current | 2.0V | No load, $f_{LCD}$=64Hz, 1/3bias, LCD display on, internal system oscillator on, $V_{LCD}$ pin input voltage=5.5V, regulator output is set to 5V | — | 35 | 56 | μA |
| $I_{STB1}$ | Standby Current for $V_{DD}$ | 3.3V | No load, 1/3bias, LCD display off, internal system oscillator off, $V_{LCD}$ pin input voltage =5V disable integrated regulator | — | — | 1 | μA |
| | | 5.0V | | — | — | 2 | μA |
| $I_{STB2}$ | Standby Current for $V_{LCD}$ | 3.3V | No load, 1/3bias, LCD display off, internal system oscillator off, $V_{LCD}$ pin input voltage =5V, disable integrated regulator | — | — | 1 | μA |
| | | 5.0V | | — | — | 2 | μA |
| $V_{reg}$ | Regulator Output | — | $V_{LCD}$ pin input voltage=5.5V, regulator output is set to 4.5V, Ta=-40°C~85°C | 4.35 | 4.5 | 4.65 | V |
| | | | $V_{LCD}$ pin input voltage=5.5V, regulator output is set to 4.5V, Ta=25°C | 4.42 | 4.5 | 4.58 | V |
| $I_{OL1}$ | LCD Common Sink Current | — | $V_{LCD}$=3.3V, $V_{OL}$=0.33V, disable integrated regulator | 250 | 400 | — | μA |
| | | | $V_{LCD}$=5V, $V_{OL}$=0.5V, disable integrated regulator | 500 | 800 | — | μA |
| $I_{OH1}$ | LCD Common Source Current | — | $V_{LCD}$=3.3V, $V_{OH}$=2.97V, disable integrated regulator | -140 | -230 | — | μA |
| | | | $V_{LCD}$=5V, $V_{OH}$=4.5V, disable integrated regulator | -300 | -500 | — | μA |
| $I_{OL2}$ | LCD Segment Sink Current | — | $V_{LCD}$=3.3V, $V_{OL}$=0.33V, disable integrated regulator | 250 | 400 | — | μA |
| | | | $V_{LCD}$=5V, $V_{OL}$=0.5V, disable integrated regulator | 500 | 800 | — | μA |
| $I_{OH2}$ | LCD Segment Source Current | — | $V_{LCD}$=3.3V, $V_{OH}$=2.97V, disable integrated regulator | -140 | -230 | — | μA |
| | | | $V_{LCD}$=5V, $V_{OH}$=4.5V, disable integrated regulator | -300 | -500 | — | μA |
| $I_{OL3}$ | LED Sink Current | — | $V_{LCD}$=3.3V, $V_{OL}$=1V, when SP1 bit is set to “1” | 10 | — | — | mA |
| | | | $V_{LCD}$=5.0V, $V_{OL}$=2V, when SP1 bit is set to “1” | 20 | — | — | mA |

Note:

1. Please use the integrated regulator when the Regulator output voltage is less than ($V_{LCD}$ - 0.5V).

2. If 8 LEDs turn on at the same time, total current of LED drivers can not be allowed more than 80mA.

## A.C. Characteristics

Unless otherwise specified, $V_{DD}$ =1.8 to 5.5V; $V_{SS}$ = 0V; Ta =-40~85°C

| Symbol | Parameter | Test Condition $V_{DD}$ | Test Condition | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $f_{LCD1}$ | LCD Frame Frequency | — | Ta=25°C, $V_{DD}$=3.3V | Frame frequency is set to 64Hz | 57.6 | 64 | 70.4 | Hz |
| | | | | Frame frequency is set to 85.3Hz | 76 | 85.3 | 94.0 | |
| | | | | Frame frequency is set to 128Hz | 115.2 | 128 | 140.8 | |
| | | | | Frame frequency is set to170.6Hz | 152 | 170.6 | 188.0 | |
| $f_{LCD2}$ | | — | Ta=-40~85°C, $V_{DD}$=2.5~5.5V | Frame frequency is set to 64Hz | 51.2 | 64 | 83.0 | Hz |
| | | | | Frame frequency is set to 85.3Hz | 68 | 85.3 | 111 | |
| | | | | Frame frequency is set to 128Hz | 102.4 | 128 | 166 | |
| | | | | Frame frequency is set to 170.6Hz | 136 | 170.6 | 222 | |
| $f_{LCD3}$ | | — | Ta=-40~85°C, $V_{DD}$=1.8~2.5V | Frame frequency is set to 64Hz | 45.0 | — | 64 | Hz |
| | | | | Frame frequency is set to 85.3Hz | 59.0 | — | 85.3 | |
| | | | | Frame frequency is set to 128Hz | 90.0 | — | 128 | |
| | | | | Frame frequency is set to 170.6Hz | 118.0 | — | 170.6 | |
| $t_{SR}$ | $V_{DD}$ Slew Rate | 3.3<br>5.0 | — | | 0.05 | — | — | V/ms |
| $t_{POF}$ | $V_{DD}$ Off Times | 3.3<br>5.0 | $V_{DD}$ drop down to 0.9V | | 10 | — | — | ms |
| $t_{RSON}$ | RSTB Input Time | 3.3<br>5.0 | When RSTB signal is externally input from a microcontroller etc. | | 250 | — | — | ns |
| | | 3.3<br>5.0 | R=100kΩ and C=0.1μF (See application circuit) | | — | 100 | — | ms |
| $t_{RW}$ | RSTB Pulse Width | 3.3<br>5.0 | When RSTB signal is externally input from a microcontroller etc. | | 400 | — | — | ns |
| $t_{RSOFF}$ | Wait Time for Data Transfers | 3.3<br>5.0 | 2-wire I$^2$C or 3-wire SPI interface | | 1 | — | — | ms |

Note: $f_{LCD} = 1/t_{LCD}$

## A.C. Characteristics – I²C Interface

Unless otherwise specified, $V_{SS}$=0V; $V_{DD}$=1.8V to 5.5V; Ta=-40~85°C

| Symbol | Parameter | Condition | $V_{DD}$=1.8V to 5.5V | | $V_{DD}$=3.0V to 5.5V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $f_{SCL}$ | Clock Frequency | — | — | 100 | — | 400 | kHz |
| $t_{BUF}$ | Bus Free Time | Time in which the bus must be free before a new transmission can start | 4.7 | — | 1.3 | — | μs |
| $t_{HD:STA}$ | Start Condition Hold Time | After this period, the first clock pulse is generated | 4 | — | 0.6 | — | μs |
| $t_{LOW}$ | SCL Low Time | — | 4.7 | — | 1.3 | — | μs |
| $t_{HIGH}$ | SCL High Time | — | 4 | — | 0.6 | — | μs |
| $t_{SU:STA}$ | Start Condition Setup Time | Only relevant for repeated START condition | 4.7 | — | 0.6 | — | μs |
| $t_{HD:DAT}$ | Data Hold Time | — | 0 | — | 0 | — | ns |
| $t_{SU:DAT}$ | Data Setup Time | — | 250 | — | 100 | — | ns |
| $t_R$ | SDA and SCL Rise Time | Note | — | 1 | — | 0.3 | μs |
| $t_F$ | SDA and SCL Fall Time | Note | — | 0.3 | — | 0.3 | μs |
| $t_{SU:STO}$ | Stop Condition Set-up Time | — | 4 | — | 0.6 | — | μs |
| $t_{AA}$ | Output Valid From Clock | — | — | 3.5 | — | 0.9 | μs |
| $t_{SP}$ | Input Filter Time Constant (SDA and SCL Pins) | Noise suppression time | — | 20 | — | 20 | ns |

Note: These parameters are periodically sampled but not 100% tested.

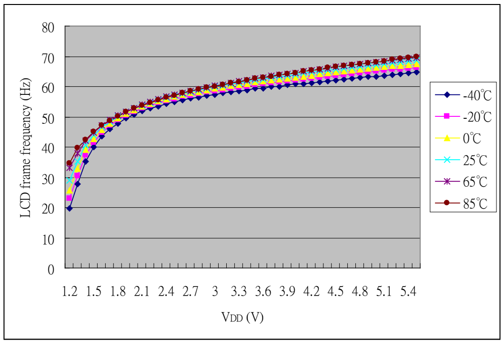
## A.C. Characteristics – SPI Interface

Unless otherwise specified, $V_{DD}$ =1.8 to 5.5V; $V_{SS}$ = 0V; Ta =-40~85°C

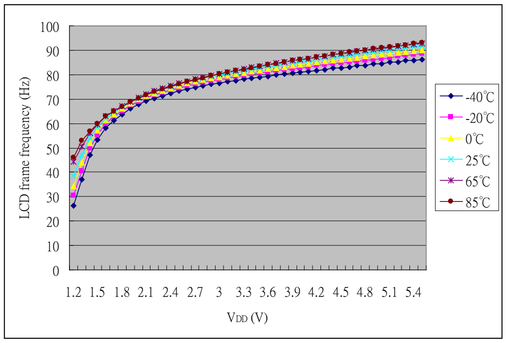
| Symbol | Parameter | Test Condition | | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ | Condition | | | | | |
| $t_{SYS}$ | Clock Cycle Time | — | For write data | | 250 | — | — | ns |
| | | | For read data | | 1000 | — | — | ns |
| $t_{CW}$ | Clock Pulse Width | — | For write data | | 50 | — | — | ns |
| | | — | For read data | | 400 | — | — | ns |
| $t_{DS}$ | Data Setup Time | — | For write data | | 50 | — | — | ns |
| $t_{DH}$ | Data Hold Time | — | For write data | | 50 | — | — | ns |
| $t_{CSW}$ | "H" CSB Pulse Width | — | — | | 50 | — | — | ns |
| $t_{CSL}$ | CSB Setup Time (CSB↓–CLK↑) | — | For write data | | 50 | — | — | ns |
| | | | For read data | | 400 | — | — | ns |
| $t_{CSH}$ | CS Hold Time (CLK↑–CSB↑) | — | — | | 2 | — | — | μs |
| $t_{PD}$ | DATA Output Delay Time (CLK–DIO) | — | $C_O$=15pF | $t_{PD}$=10% to 90% | — | — | 350 | ns |
| | | | | $t_{PD}$=90% to 10% | | | | |

## Characteristics Curves – $f_{LCD}$ vs. $V_{DD}$ vs. Temperature

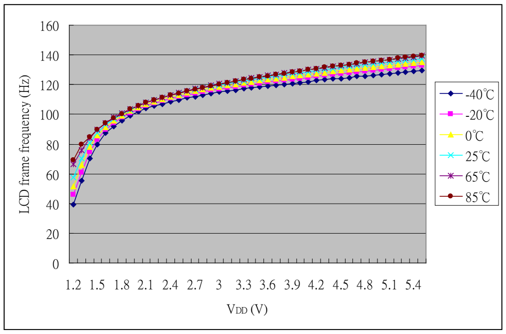
**LCD frame frequency is set to 64Hz**



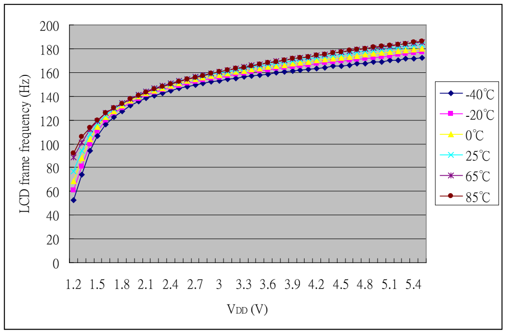

**LCD frame frequency is set to 85.3Hz**




**LCD frame frequency is set to 128Hz**




**LCD frame frequency is set to 170.6Hz**



## Functional Description

### Power-On Reset

When the power is applied, the device is initialized by an internal power-on reset circuit. The status of the internal circuits after initialization is as follows:

- All common outputs are set to $V_{LCD}$.
- All segment outputs are set to $V_{LCD}$.
- The drive mode 1/4 duty output and 1/3 bias is selected.
- The system oscillator and the LCD bias generator are off state.
- LCD display is off state.
- Integrated regulator is disabled.
- The segment/LED shared pin is set as the segment pin.
- Frame frequency is set to 64Hz.
- Blinking function is switched off.

### Reset Function

When the RSTB pin is pulled to a low level, a reset operation is executed and it will initialize all functions. The status of the internal circuits after initialization is as follows:

- All common outputs are set to $V_{LCD}$.
- All segment outputs are set to $V_{LCD}$.
- The drive mode 1/4 duty output and 1/3 bias is selected.
- The system oscillator and the LCD bias generator are off state.
- LCD display is off state.
- Integrated regulator is disabled.
- The segment/LED shared pin is set as the segment pin.
- Frame frequency is set to 64Hz.
- Blinking function is switched off.

### Display Memory – RAM Structure

The display RAM is static 48×8-bits RAM which stores the LCD data. Logic "1" in the RAM bit-map indicates the "on" state of the corresponding LCD segment; similarly, logic 0 indicates the off state.

The contents of the RAM data are directly mapped to the LCD data. The first RAM column corresponds to the segments operated with respect to COM0. In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with COM1, COM2 and COM3 respectively. The LCD display duty can be 1/4 or 1/8 determined by a Duty bit contained in the Drive Mode Command. The following diagram is a data transfer format for I²C or SPI interface.

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| LCD | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| LED | LED7 | LED6 | LED5 | LED4 | LED3 | LED2 | LED1 | LED0 |

**LCD Display or LED output data transfer format for I²C or SPI interface**

### 1/4 Duty Display Mode

- **52×4 Display Mode**

When the SP1 bit is set to "0" and the SP0 bit is set to "0" or "1", the drive mode is selected as 52 segments by 4 commons. This drive mode is also the default setting after a reset.

| Output | COM3 | COM2 | COM1 | COM0 | Output | COM3 | COM2 | COM1 | COM0 | Address |
|---|---|---|---|---|---|---|---|---|---|---|
| SEG1 | | | | | SEG0 | | | | | 00H |
| SEG3 | | | | | SEG2 | | | | | 01H |
| SEG5 | | | | | SEG4 | | | | | 02H |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| SEG51 | | | | | SEG50 | | | | | 19H |
| | D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 | Data |

**RAM mapping of 52×4 display mode**

- **48×4 Display Mode**

When the SP1 bit is set to "1" and the SP0 bit is set to "0", the drive mode is selected as 48 segments by 4 commons together with 4 LED driving outputs.

| Output | COM3 | COM2 | COM1 | COM0 | Output | COM3 | COM2 | COM1 | COM0 | Address |
|---|---|---|---|---|---|---|---|---|---|---|
| SEG1 | | | | | SEG0 | | | | | 00H |
| SEG3 | | | | | SEG2 | | | | | 01H |
| SEG5 | | | | | SEG4 | | | | | 02H |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| SEG47 | | | | | SEG46 | | | | | 17H |
| | D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 | Data |

**RAM mapping of 48×4 display mode**

- **44×4 Display Mode**

When the SP1 bit is set to "1" and the SP0 bit is set to "1", the drive mode is selected as 44 segments by 4 commons together with 8 LED driving outputs.

| Output | COM3 | COM2 | COM1 | COM0 | Output | COM3 | COM2 | COM1 | COM0 | Address |
|---|---|---|---|---|---|---|---|---|---|---|
| SEG1 | | | | | SEG0 | | | | | 00H |
| SEG3 | | | | | SEG2 | | | | | 01H |
| SEG5 | | | | | SEG4 | | | | | 02H |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| SEG43 | | | | | SEG42 | | | | | 15H |
| | D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 | Data |

**RAM mapping of 44×4 display mode**

### 1/8 Duty Display Mode

- **48×8 Display Mode**

When the SP1 bit is set to "0" and the SP0 bit is set to "0" or "1", the drive mode is selected as 48 segments by 8 commons.

| Output | COM7 | COM6 | COM5 | COM4 | COM3 | COM2 | COM1 | COM0 | Address |
|---|---|---|---|---|---|---|---|---|---|
| SEG4 | | | | | | | | | 00H |
| SEG5 | | | | | | | | | 01H |
| SEG6 | | | | | | | | | 02H |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| SEG51 | | | | | | | | | 2FH |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Data |

**RAM mapping of 48×8 display mode**

- **44×8 Display Mode**

When the SP1 bit is set to "1" and the SP0 bit is set to "0", the drive mode is selected as 44 segments by 8 commons together with 4 LED driving outputs.

| Output | COM7 | COM6 | COM5 | COM4 | COM3 | COM2 | COM1 | COM0 | Address |
|---|---|---|---|---|---|---|---|---|---|
| SEG4 | | | | | | | | | 00H |
| SEG5 | | | | | | | | | 01H |
| SEG6 | | | | | | | | | 02H |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| SEG47 | | | | | | | | | 2BH |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Data |

**RAM mapping of 48×8 display mode**

- **40×8 Display Mode**

When the SP1 bit is set to "1" and the SP0 bit is set to "1", the drive mode is selected as 40 segments by 8 commons together with 8 LED driving outputs.

| Output | COM7 | COM6 | COM5 | COM4 | COM3 | COM2 | COM1 | COM0 | Address |
|---|---|---|---|---|---|---|---|---|---|
| SEG4 | | | | | | | | | 00H |
| SEG5 | | | | | | | | | 01H |
| SEG6 | | | | | | | | | 02H |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| SEG43 | | | | | | | | | 27H |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Data |

**RAM mapping of 48×8 display mode**

## System Oscillator

The timing for the internal logic and the LCD drive signals are generated by an internal oscillator. The System Clock frequency ($f_{SYS}$) determines the LCD frame frequency. During initial system power on the System Oscillator will be in the stop state.

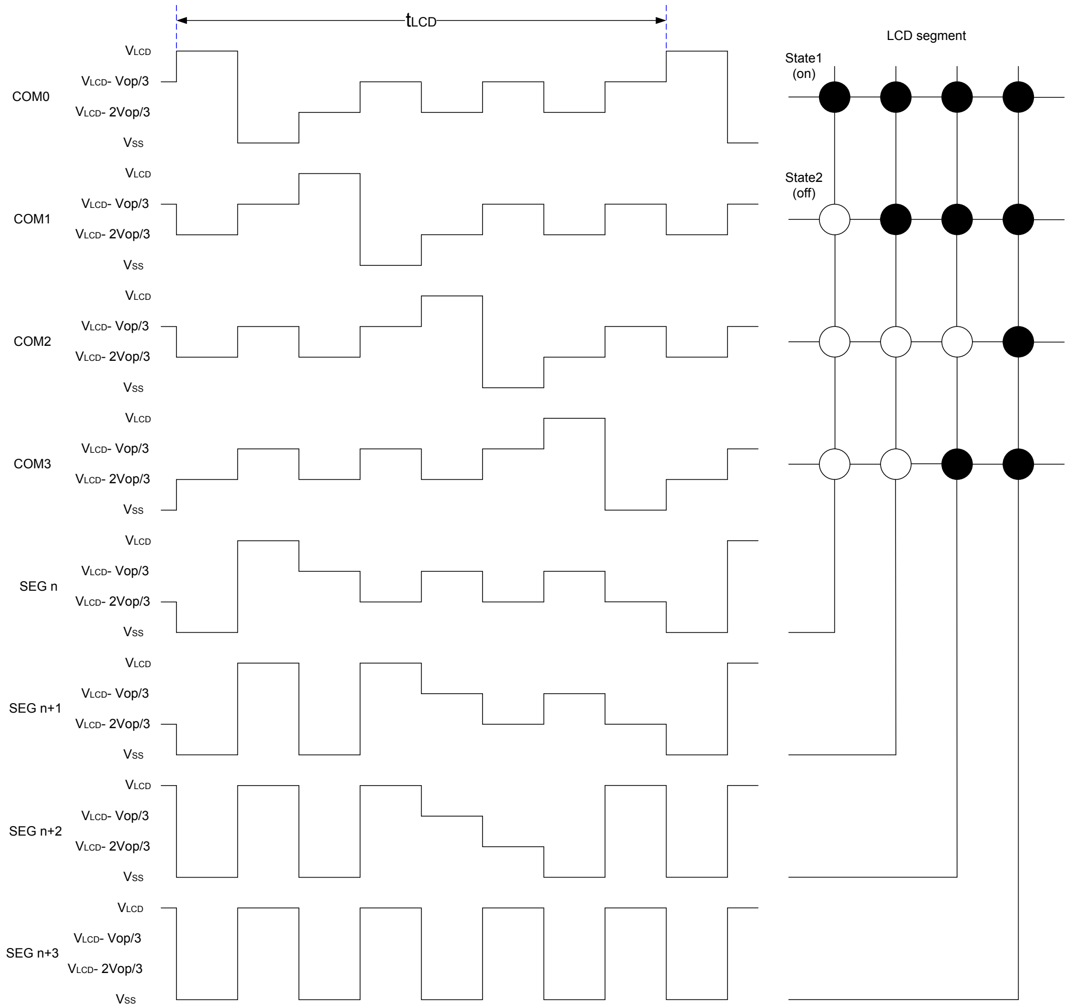
## LCD Bias Generator

The LCD supply power can come from the external VLCD pin or the internal regulator output voltage determined using the Internal Voltage Adjustment (IVA) setting command. The device provides an external VLCD pin and also integrates an internal regulator. The LCD voltage may be temperature compensated externally through the Voltage supply to the VLCD pin. The internal regulator can also provide the LCD operating voltage. Therefore, the full-scale LCD voltage ($V_{OP}$) is obtained from ($V_{LCD} – V_{SS}$) or ($V_{reg} – V_{SS}$).

Fractional LCD biasing voltages, known as 1/3 or 1/4 bias voltage, are obtained from an internal voltage divider of four series resistors connected between $V_{LCD}$ and $V_{SS}$. The centre resistor can be switched out of circuits to provide a 1/3 bias voltage level configuration.

## LCD Drive Mode Waveforms

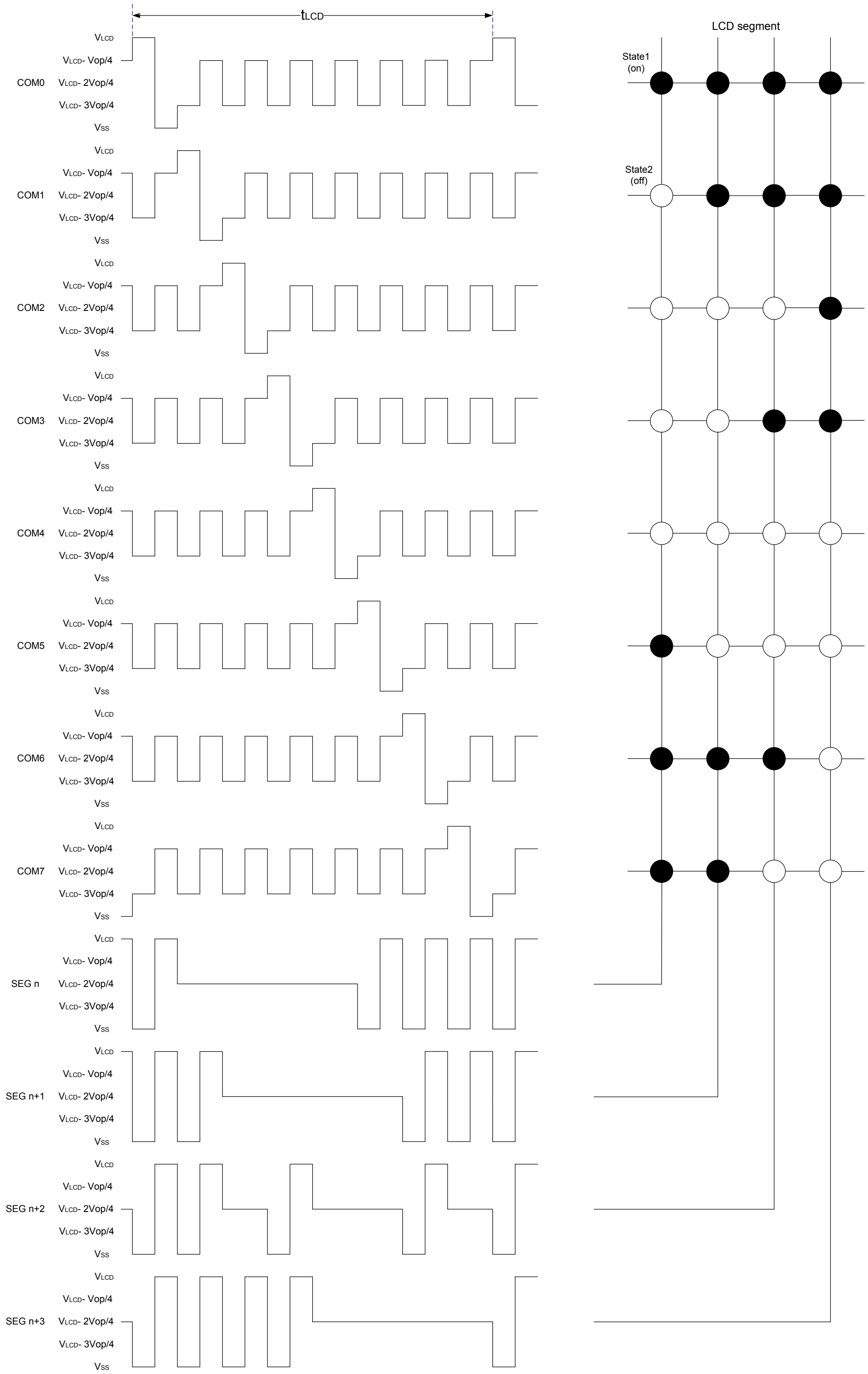
- When the LCD drive mode is selected as 1/4 duty and 1/3 bias, the waveform and LCD display is shown as follows:




**Waveforms for 1/4 duty drive mode with1/3 bias ($V_{OP}$=$V_{LCD}$−$V_{SS}$)**

Note: $t_{LCD}$ = 1/$f_{LCD}$

• When the LCD drive mode is selected as 1/8 duty and 1/4bias, the waveform and LCD display is shown as follows:




**Waveforms for 1/8 duty drive mode with1/4 bias ($V_{OP}=V_{LCD}-V_{SS}$)**

Note: $t_{LCD} = 1/f_{LCD}$

## Segment Driver Outputs

The LCD drive section includes 52 segment outputs SEG0~SEG51 or 48 segment outputs SEG4~SEG51 which should be connected directly to the LCD panel. The segment output signals are generated in accordance with the multiplexed column signals and with the data resident in the display latch. The unused segment outputs should be left open-circuit when less than 52 or 48 segment outputs are required.

## Column Driver Outputs

The LCD drive section includes 4 column outputs COM0~COM3 or 8 column outputs COM0~COM7 which should be connected directly to the LCD panel. The column output signals are generated in accordance with the selected LCD drive mode. The unused column outputs should be left open-circuit if less than 4 or 8 column outputs are required.

## Address Pointer

The addressing mechanism for the display RAM is implemented using the address pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the address pointer by the Display Data Input command.

## Blinking Function

The device contains versatile blinking capabilities. The whole display can be blinked at frequencies selected by the Blinking Frequency command. The blinking frequency is a subdivided ratio of the system frequency. The ratio between the system oscillator and blinking frequencies depends on the blinking mode in which the device is operating, as shown in the following table:

| Blinking Mode | Blinking Frequency (Hz) |
|---|---|
| 0 | Blink off |
| 1 | 2 |
| 2 | 1 |
| 3 | 0.5 |

## Frame Frequency

The HT16L23 device provides four frame frequencies selected with Frame Frequency command known as 64Hz, 85.3Hz, 128Hz and 170.6Hz respectively.

## LED Function

The LED pins are NMOS-structured output pins. The Data for the LED output is contained in the LED output setting command, starting from the most significant bit. When a written data bit for a LED pin is set to 1, the corresponding driving LED lights up while the LED is switched off when the written data bit is 0. The LED pins are pin-shared with the LCD segment pins and can be selected using the SP1 and SP0 bits in the Drive Mode command.

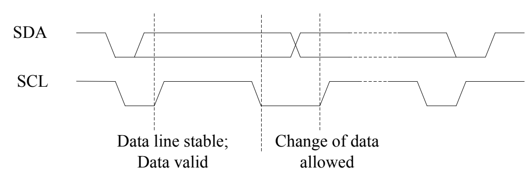
# I²C Serial Interface

## I²C Operation

The device supports I²C serial interface. The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to the positive supply via pull-up resistors with a typical value of 4.7kΩ. When the bus is free, both lines are high. Devices connected to the bus must have open-drain or open-collector outputs to implement a wired-or function. Data transfer is initiated only when the bus is not busy.

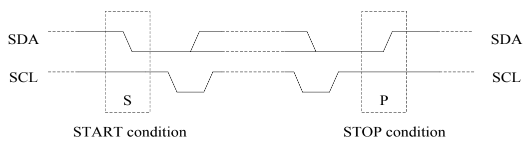
### Data Validity

The data on the SDA line must be stable during the high period of the serial clock. The high or low state of the data line can only change when the clock signal on the SCL line is Low as shown in the diagram.



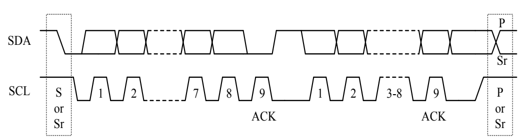
### START and STOP Conditions

- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In some respects, the START(S) and repeated START (Sr) conditions are functionally identical.



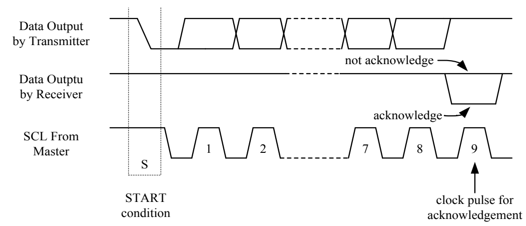

### Byte Format

Every byte put on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit, MSB, first.




### Acknowledge

- Each bytes of eight bits is followed by one acknowledge bit. This Acknowledge bit is a low level placed on the bus by the receiver. The master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an Acknowledge, ACK, after the reception of each byte.
- The device that acknowledges must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.
- A master receiver must signal an end of data to the slave by generating a not-acknowledge, NACK, bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse to not acknowledge. The master will generate a STOP or repeated START condition.




### Slave Addressing

- The slave address byte is the first byte received following the START condition form the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines a read or write operation to be performed. When the R/$\overline{W}$ bit is "1", then a read operation is selected. A "0" selects a write operation.
- The HT16L23 address bits are "0111110". When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an Acknowledge on the SDA line.

Slave Address

MSB LSB

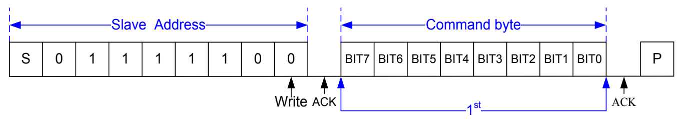
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | R/$\overline{W}$ |

## I²C Interface Write Operation

### Byte Write Operation

- **Single Command Type**

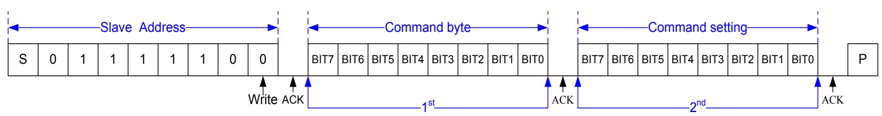
A Single Command write operation requires a START condition, a slave address with an R/$\overline{W}$ bit, a command byte and a STOP condition for a single command write operation.




**I²C Single Command Type Write Operation**

- **Compound Command Type**

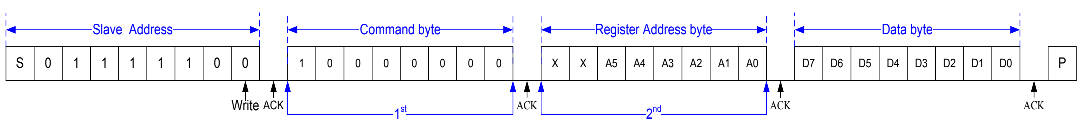
A Compound Command write operation requires a START condition, a slave address with an R/$\overline{W}$ bit, a command byte, a command setting byte and a STOP condition for a compound command write operation.




**I²C Compound Command Type Write Operation**

- **Display RAM Single Data Byte**

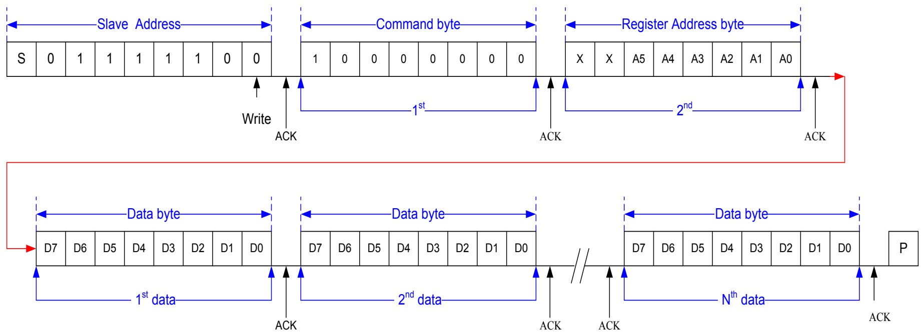
A display RAM data byte write operation requires a START condition, a slave address with an R/$\overline{W}$ bit, a display data input command byte, a valid Register Address byte, a Data byte and a STOP condition.




**I²C Display RAM Single Data Byte Write Operation**

### Display RAM Page Write Operation

After a START condition the slave address with the R/$\overline{W}$ bit is placed on the bus followed with a display data input command byte and the specified display RAM Register Address of which the contents are written to the internal address pointer. The data to be written to the memory will be transmitted next and then the internal address pointer will be incremented by 1 to indicate the next memory address location after the reception of an acknowledge clock pulse. After the internal address point reaches the maximum memory address, the address pointer will be reset to 00H.



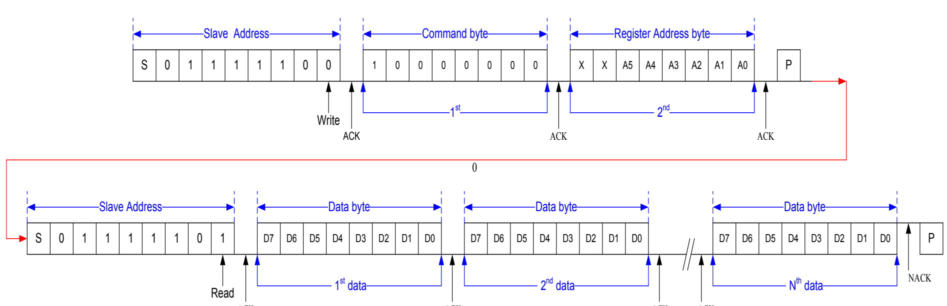

I²C Interface N Bytes Display RAM Data Write Operation

| Duty | SP1 | SP0 | Maximum Memory Address |
|---|---|---|---|
| 1/4 | 0 | X | 19H |
| | 1 | 0 | 17H |
| | 1 | 1 | 15H |
| 1/8 | 0 | X | 2FH |
| | 1 | 0 | 2BH |
| | 1 | 1 | 27H |

## I²C Interface Display RAM Read Operation

In this mode, the master reads the HT16L23 data after setting the slave address. Following the R/$\overline{W}$ bit (="0") is an acknowledge bit, a command byte and the register address byte which is written to the internal address pointer. After the start address of the Read Operation has been configured, another START condition and the slave address transferred on the bus followed by the R/$\overline{W}$ bit (="1"). Then the MSB of the data which was addressed is transmitted first on the I²C bus. The address pointer is only incremented by 1 after the reception of an acknowledge clock. That means that if the device is configured to transmit the data at the address of $A_{N+1}$, the master will read and acknowledge the transferred new data byte and the address pointer is incremented to $A_{N+2}$. After the internal address pointer reaches the maximum memory address, the address pointer will be reset to 00H.

This cycle of reading consecutive addresses will continue until the master sends a STOP condition.




I²C Interface N Bytes Display RAM Data Read Operation

## SPI Serial Interface

### SPI Operation

The device also includes a 3-wire SPI serial interface. The SPI operations are described as follows:

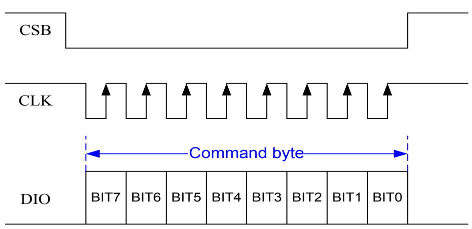
- The CSB pin is used to activate the data transfer. When the CSB pin is at a high level, the SPI operation will be reset and stopped. If the CSB pin changes state from high to low, data transmission will start.
- The data is transferred from the MSB of each byte and is shifted into the shift register during each CLK rising edge.
- The input data is automatically latched into the internal register for each 8-bits of input data after the CSB signal goes low.
- For read operations, the MCU should assert a high pulse on the CSB pin to change the data transfer direction from input mode to output mode on the DIO pin after sending the command byte and the setting values. If the MCU sets the CSB signal to a high level again after receiving the output data, the data direction on the DIO pin will be changed into input mode and the read operation will end.
- For a read operation, the data is output on the DIO pin at the CLK falling edge.
- For display RAM data read/write operations using the SPI interface, the read/write control bit is contained in the Display Data Input Command. Refer to the Display Data Input Command description for more details.

## SPI Interface Write Operation

### Byte Write Operation

- **Single Command Type**

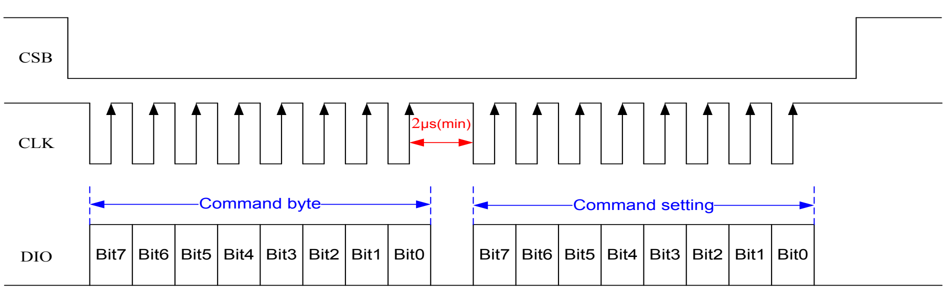
A Single Command write operation is activated by the CSB signal going low. The 8-bit command byte is shifted from the MSB into the shift register at each CLK rising edge.




**SPI Single Command Type Write Operation**

- **Compound Command Type**

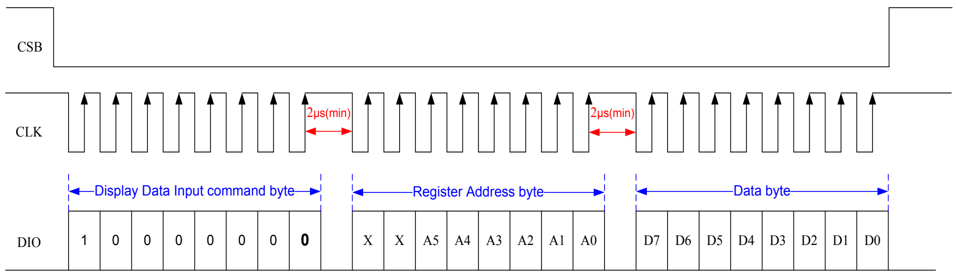
For a compound command, an 8-bit command byte is first shifted into the shift register followed by an 8-bit command setting. Note that the CLK high pulse width, after the command byte has been shifted in, must remain at this level for at least 2μs after which the command setting data can be consecutively shifted in.




**SPI Compound Command Type Write Operation**

- **Display RAM Single Data Byte**

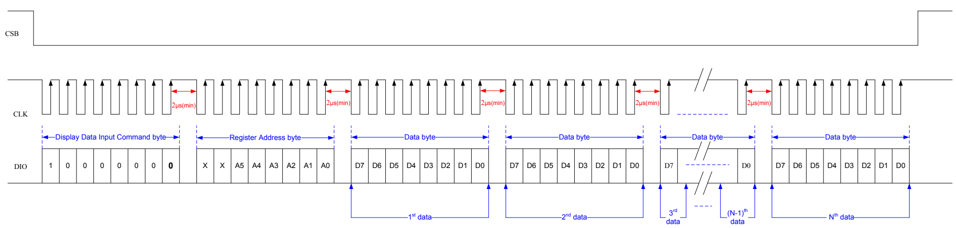
The display RAM single data write operation consists of a display data input (write) command, a register address and a write data byte.




**SPI Display RAM Single Data Byte Write Operation**

### Display RAM Page Write Operation

The display RAM Page write operation consists of a display data write command, a register address of which the contents are written to the internal address pointer followed by N bytes of written data. The data to be written to the memory will be transmitted next and then the internal address pointer will be automatically incremented by 1 to indicate the next memory address location. After the internal address point reaches the maximum memory address, the address pointer will be reset to 00H.



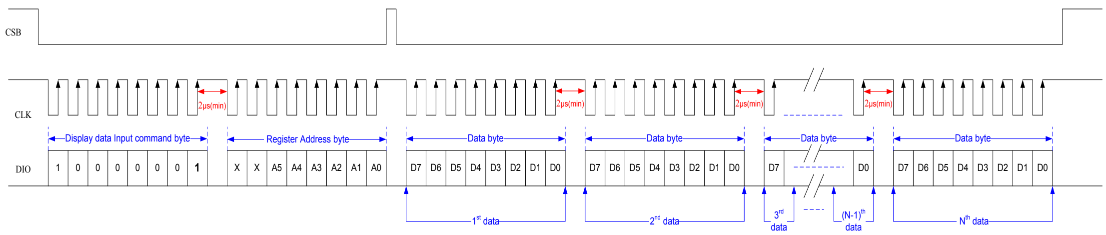
**SPI Interface N Bytes Display RAM Data Write Operation**

| Duty | SP1 | SP0 | Maximum Memory Address |
|---|---|---|---|
| 1/4 | 0 | X | 19H |
| | 1 | 0 | 17H |
| | 1 | 1 | 15H |
| 1/8 | 0 | X | 2FH |
| | 1 | 0 | 2BH |
| | 1 | 1 | 27H |

### SPI Interface Display RAM Read Operation

In this mode, the master reads the HT16L23 data after sending the Display Data Input command when the CSB pin changes state from high to low. Following the read/write control bit, which is contained in the Display Data Input command, is the register address byte which is written to the internal address pointer. After the start address of the Read Operation has been configured, another CSB high pulse is placed on the bus and then the MSB of the data which was addressed is transmitted first on the SPI bus. The address pointer is only incremented by 1 after the reception of each data byte. That means that if the device is configured to transmit the data at the address of $A_{N+1}$, the master will read the transferred data byte and the address pointer is incremented to $A_{N+2}$. After the internal address pointer reaches the maximum memory address, the address pointer will be reset to 00H.

This cycle of reading consecutive addresses will continue until the master pulls the CSB line to a high level to terminate the data transfer.




**SPI Interface N Bytes Display RAM Data Read Operation**

## Command Summary

### Software Reset Command

This command is used to initialize the HT16L23 device.

| Function | Byte | (MSB) Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | (LSB) Bit0 | Note | R/W | Def |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Soft reset command | 1st | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | — | W | — |

Note:
- When this software reset command is executed, all the command registers are initialized to the default values.
- After the reset command is executed, the device will experience an internal initialization for 1ms.
- Normal operation can be executed after the device initialization is complete.
- During the initialization period, no commands can be executed.
- If the programmed command is not defined, the function will not be affected.

The status of the internal circuits after initialization is as follows:
- All segment/common outputs are set to $V_{LCD}$.
- The drive mode 1/4 duty output and 1/3 bias is selected.
- The system oscillator and the LCD bias generator are in an off state.
- The LCD display is in an off state and the integrated regulator is disabled.
- The segment/LED shared pin is setup as a segment pin.
- The frame frequency is set to 64Hz.
- The blinking function is switched off.

### Drive Mode Command

| Function | Byte | (MSB) Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | (LSB) Bit0 | Note | R/W | Def |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive mode setting command | 1st | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | — | W | — |
| Duty, bias and pin-shared setting | 2nd | X | X | SP1 | SP0 | X | Duty | X | Bias | — | W | 00H |

Note:

| Bit | | Duty | Bias |
|---|---|---|---|
| Duty | Bias | | |
| 0 | 0 | 1/4duty | 1/3bias |
| 0 | 1 | 1/4duty | 1/4bias |
| 1 | 0 | 1/8duty | 1/3bias |
| 1 | 1 | 1/8duty | 1/4bias |

| SP1 | SP0 | Segment/LED Shared Pin Selected | |
|---|---|---|---|
| | | Segment48~51/LED3~0 | Segment44~47/LED7~4 |
| 0 | X | Set as segment pins | Set as segment pins |
| 1 | 0 | Set as LED pins | Set as segment pins |
| 1 | 1 | Set as LED pins | Set as LED pins |

- Power on status: The drive mode 1/4 duty output and 1/3 bias is selected and also the segment output pins are selected.
- If the programmed command is not defined, the function will not be affected.

### Display Data Input Command

This command sends data from MCU to the memory MAP of the HT16L23 device.

| Function | Byte | (MSB) Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | (LSB) Bit0 | Note | R/W | Def |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Display data input/ output command | 1st | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Write operation | W | — |
| | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Read operation for 3-wire SPI interface used only. | R | — |
| Address pointer | 2nd | X | X | A5 | A4 | A3 | A2 | A1 | A0 | Display data start address of memory map | W | 00H |

Note:

| Duty | SP1 | SP0 | Maximum Memory Address |
|---|---|---|---|
| 1/4 | 0 | X | 19H |
| | 1 | 0 | 17H |
| | 1 | 1 | 15H |
| 1/8 | 0 | X | 2FH |
| | 1 | 0 | 2BH |
| | 1 | 1 | 27H |

- Power on status: The address is set to 00H.
- If the programmed command is not defined, the function will not be affected.

### System Mode Command

This command controls the internal system oscillator on/off and display on/off.

| Function | Byte | (MSB) Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | (LSB) Bit0 | Note | R/W | Def |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| System mode setting command | 1st | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | — | W | — |
| System oscillator and display on/off setting | 2nd | X | X | X | X | X | X | S | E | — | W | 00H |

Note:

| Bit | | Internal System Oscillator | LCD Display |
|---|---|---|---|
| S | E | | |
| 0 | X | off | off |
| 1 | 0 | on | off |
| 1 | 1 | on | on |

- Power on status: Display off and disable the internal system oscillator.
- If the programmed command is not defined, the function will not be affected.

### Frame Frequency Command

This command selects the frame frequency.

| Function | Byte | (MSB) Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | (LSB) Bit0 | Note | R/W | Def |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Frame frequency command | 1st | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | — | W | — |
| Frame frequency setting | 2nd | X | X | X | X | X | X | F1 | F0 | — | W | 02H |

Note:

| Bit [1:0] | Frame Frequency |
|---|---|
| F1, F0 | |
| 00 | 85.3Hz |
| 01 | 170.6Hz |
| 10 | 64Hz |
| 11 | 128Hz |

- Power on status: Frame frequency is set to 64Hz.
- If the programmed command is not defined, the function will not be affected.

### Blinking Frequency Command

This command defines the blinking frequency of the display modes.

| Function | Byte | (MSB) Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | (LSB) Bit0 | Note | R/W | Def |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Blinking frequency command | 1st | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | — | W | — |
| Blinking frequency setting | 2nd | X | X | X | X | X | X | BK1 | BK0 | — | W | 00H |

Note:

| Bit | | Blinking Frequency |
|---|---|---|
| BK1 | BK0 | |
| 0 | 0 | Blinking off |
| 0 | 1 | 2Hz |
| 1 | 0 | 1Hz |
| 1 | 1 | 0.5Hz |

- Power on status: Blinking function is switched off.
- If the programmed command is not defined, the function will not be affected.

## LED Output Command

This command defines the blinking frequency of the display modes.

| Function | Byte | (MSB) Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | (LSB) Bit0 | Note | R/W | Def |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LED output command | 1st | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | — | W | — |
| LED output data | 2nd | X | X | X | X | LED3 | LED2 | LED1 | LED0 | When [SP1:SP0]=10 used | W | 00H |
| | | LED7 | LED6 | LED5 | LED4 | LED3 | LED2 | LED1 | LED0 | When [SP1:SP0]=11 used | | |

Note:
- The LED registers and latches are cleared after a new configuration is written into the SP1 and SP0 bits in the driver mode command.
- If the programmed command is not defined, the function will not be affected.

## Internal Voltage Adjustment (IVA) Setting Command

The internal voltage ($V_{LCD}$) adjustment can provide sixteen kinds of regulator voltage adjustment options by setting the LCD operating voltage adjustment command.

| Function | Byte | (MSB) Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | (LSB) Bit0 | Note | R/W | Def |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Internal voltage adjustment(IVA) setting | 1st | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | — | W | — |
| Internal voltage adjust control | 2nd | X | X | X | VE | X | V2 | V1 | V0 | The "VE" bit is used to enable or disable the internal regulator adjustment for the LCD voltage. The V3~V0 bits can be used to adjust the $V_{LCD}$ voltage. | W | 00H |

Note:

| VE | Regulator Adjustment |
|---|---|
| 0 | Off–bias voltage is supplied from VLCD pin |
| 1 | On–bias voltage is supplied from the internal regulator |

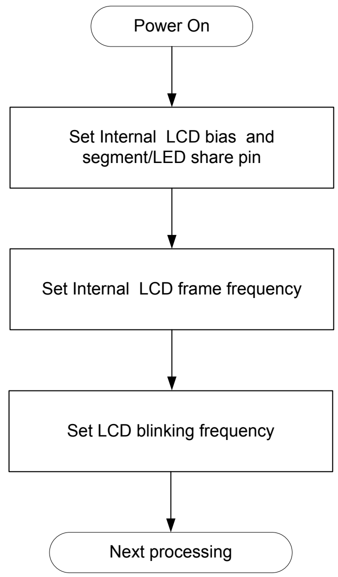
| V2 | V1 | V0 | Regulator Output Voltage (V) |
|---|---|---|---|
| 0 | 0 | 0 | 3.0V |
| 0 | 0 | 1 | 3.2V |
| 0 | 1 | 0 | 3.3V |
| 0 | 1 | 1 | 3.4V |
| 1 | 0 | 0 | 4.4V |
| 1 | 0 | 1 | 4.5V |
| 1 | 1 | 0 | 4.6V |
| 1 | 1 | 1 | 5.0V |

- Power on status: Disable the internal regulator.
- When the $V_{LCD}$ voltage is lower than 3.5V, it is recommended to disable the internal regulator so that the VLCD voltage is directly connected to the internal bias voltage generator.
- Caution: Use the internal regulator when the "Regulator output voltage<$V_{LCD}$−0.5V"
- If the programmed command is not defined, the function will not be affected.

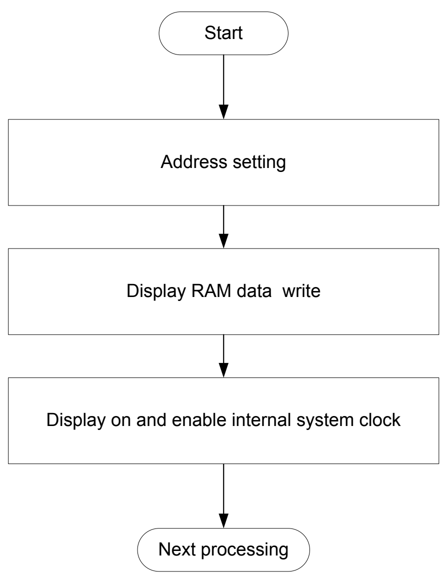
## Operation Flow Chart

Access procedures are illustrated below using flowcharts.

### Initialization




### Display Data Read/Write (Address Setting)



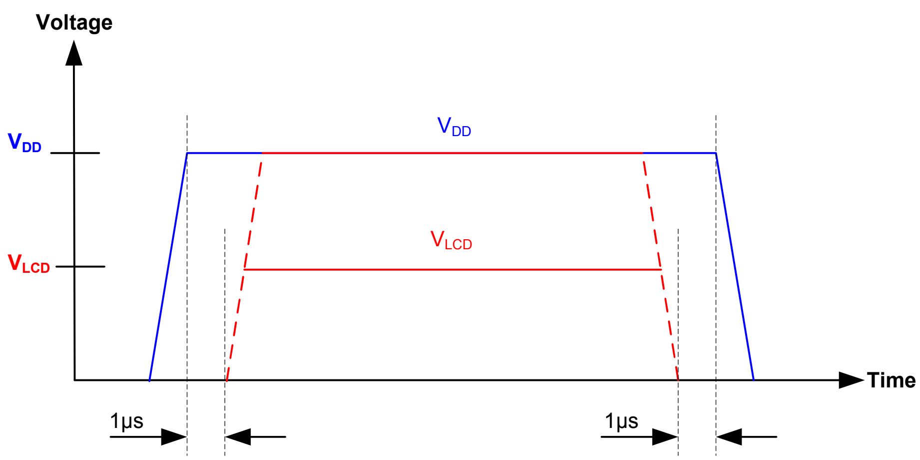
## Power Supply Sequence

- If the power is individually supplied on the LCD and VDD pins, it is strongly recommended to follow the Holtek power supply sequence requirement.
- If the power supply sequence requirement is not followed, it may result in malfunction.

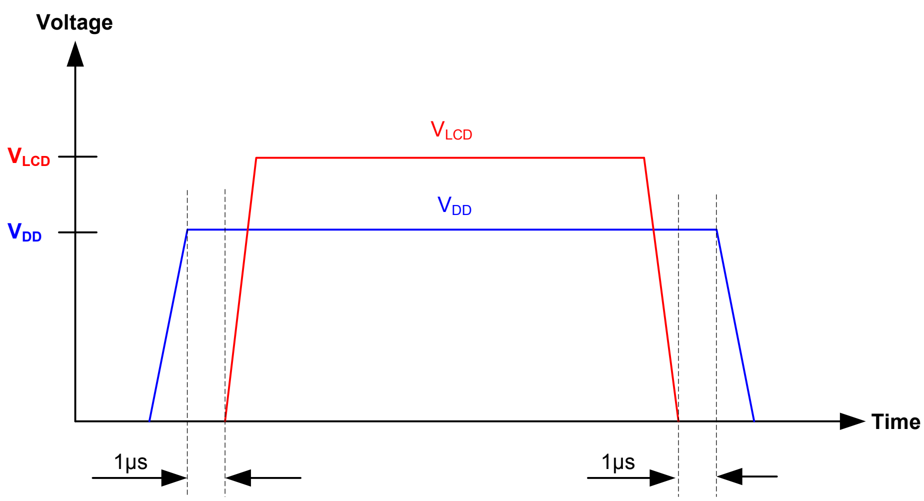
Holtek Power Supply Sequence Requirement:

1. Power-on sequence:
   Turn on the logic power supply $V_{DD}$ first and then turn on the LCD driver power supply $V_{LCD}$.
2. Power-off sequence:
   Turn off the LCD driver power supply $V_{LCD}$. First and then turn off the logic power supply $V_{DD}$.
3. The Holtek Power Supply Sequence Requirement must be followed no matter whether the $V_{LCD}$ voltage is higher than the $V_{DD}$ voltage.

- When the $V_{LCD}$ voltage is smaller than or is equal to $V_{DD}$ voltage application




- When the $V_{LCD}$ voltage is greater than $V_{DD}$ voltage application

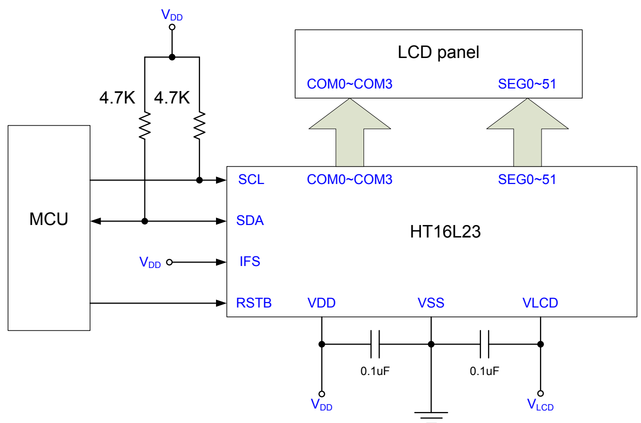


## Application Circuit

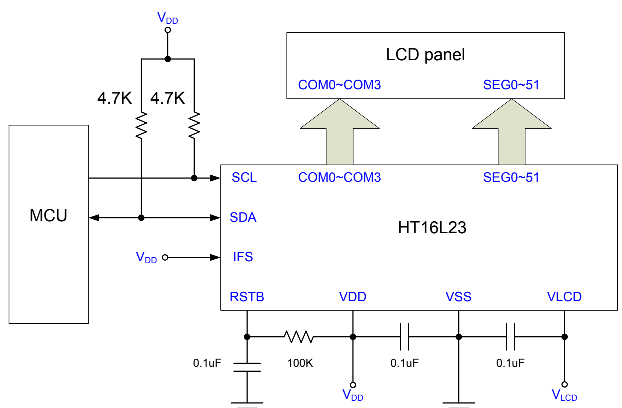
### I²C Interface

- **1/4 Duty, [SP1:SP0]=0x**

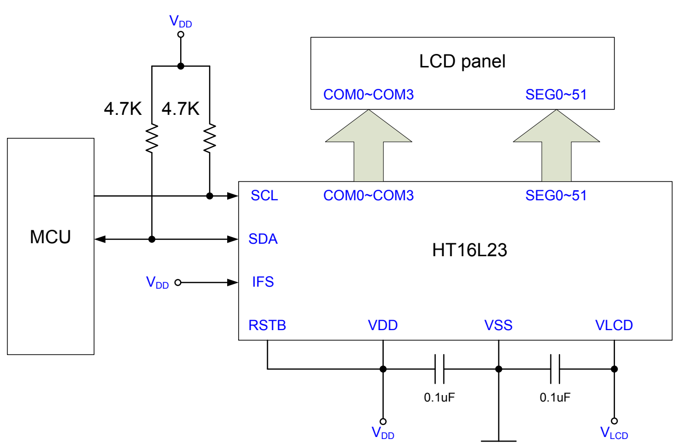
**(1) RSTB pin is connected to a MCU.**




**(2) RSTB pin is connected to external resistor and capacitor.**

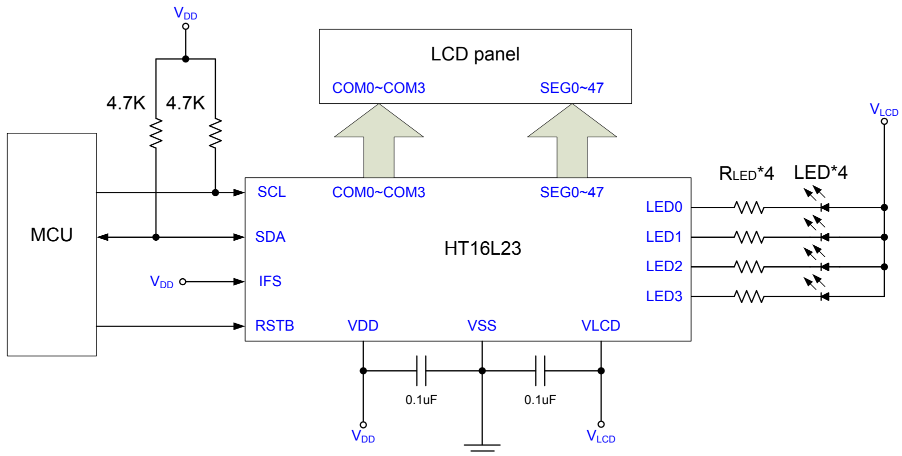



**(3) Use internal power on reset circuit only, the RSTB pin must be connected to $V_{DD}$**

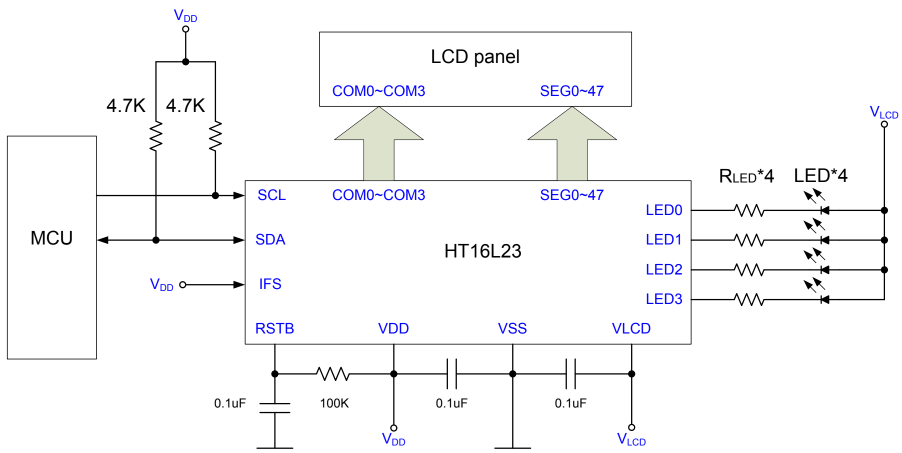


- **1/4 Duty, [SP1:SP0]=10**

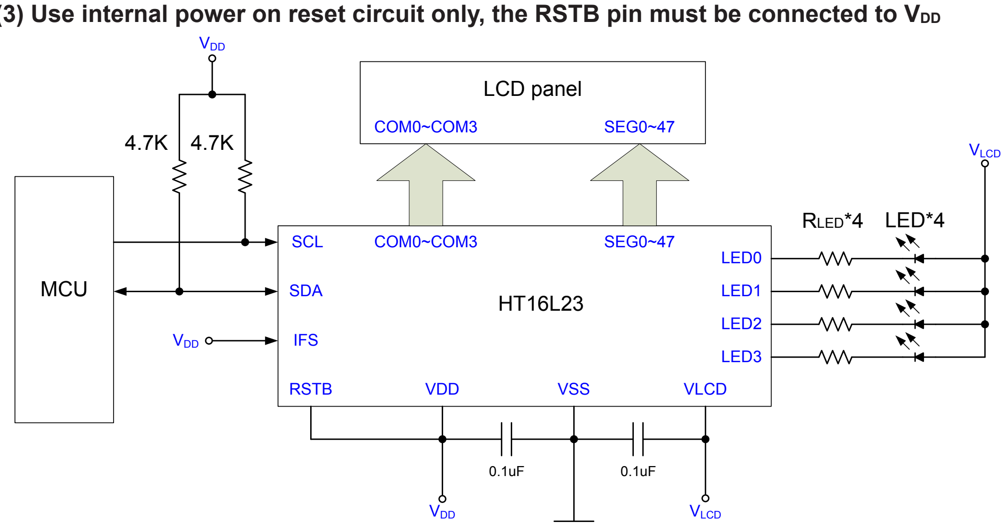
**(1) RSTB pin is connected to a MCU.**




**(2) RSTB pin is connected to external resistor and capacitor.**

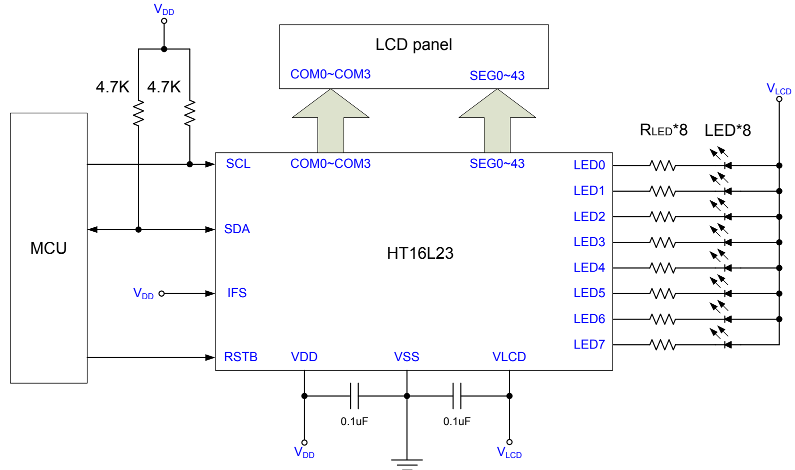



**(3) Use internal power on reset circuit only, the RSTB pin must be connected to $V_{DD}$**

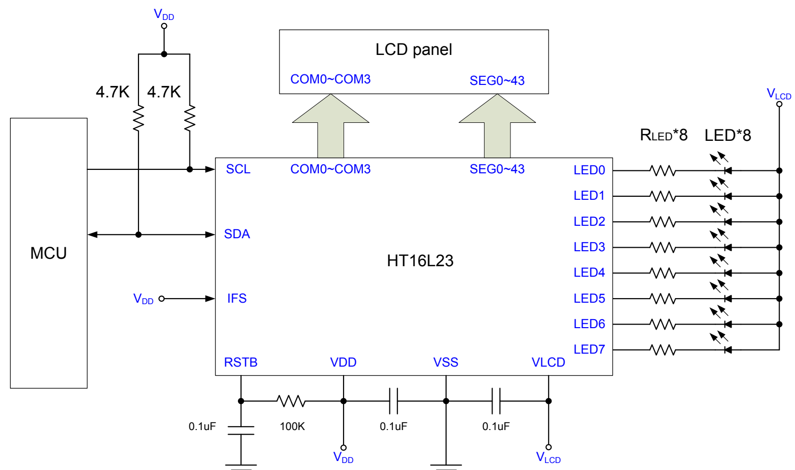


- **1/4 duty, [SP1:SP0]=11**

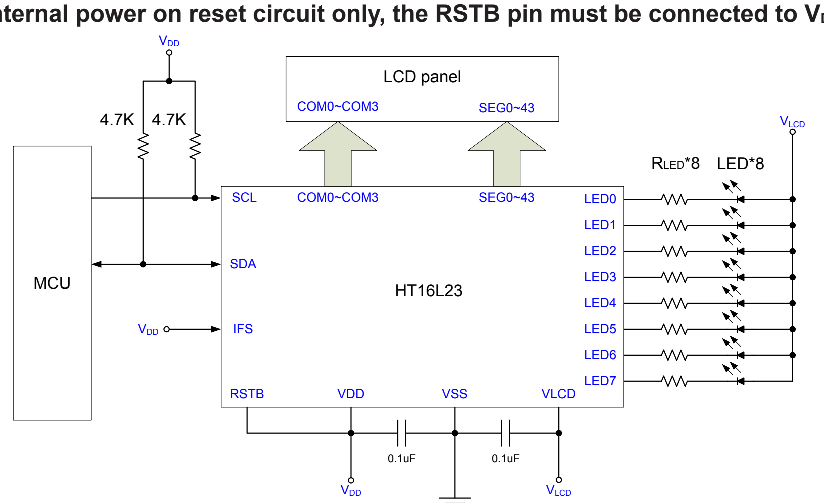
**(1) RSTB pin is connected to a MCU.**




**(2) RSTB pin is connected to external resistor and capacitor.**

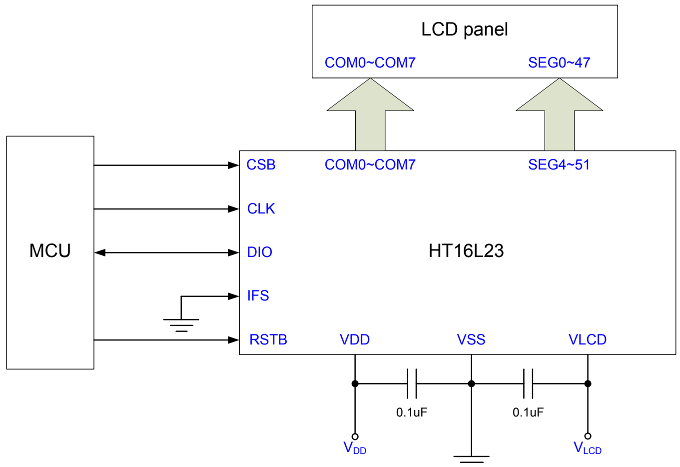



**(3) Use internal power on reset circuit only, the RSTB pin must be connected to $V_{DD}$**

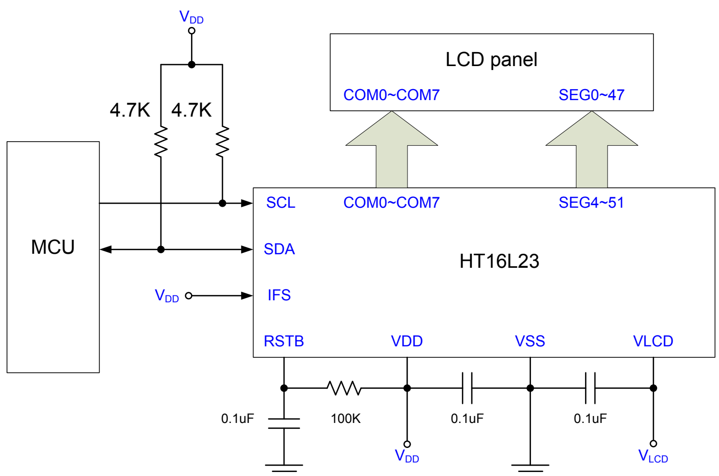


- **1/8 duty, [SP1:SP0]=0x**

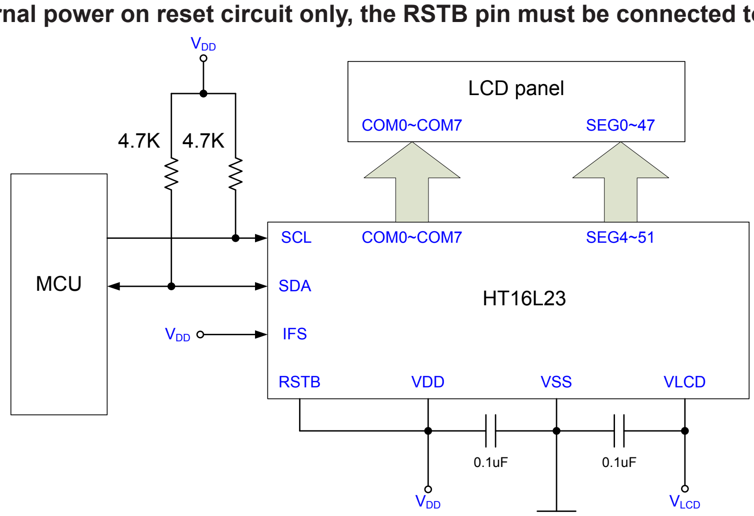
**(1) RSTB pin is connected to a MCU.**




**(2) RSTB pin is connected to external resistor and capacitor.**

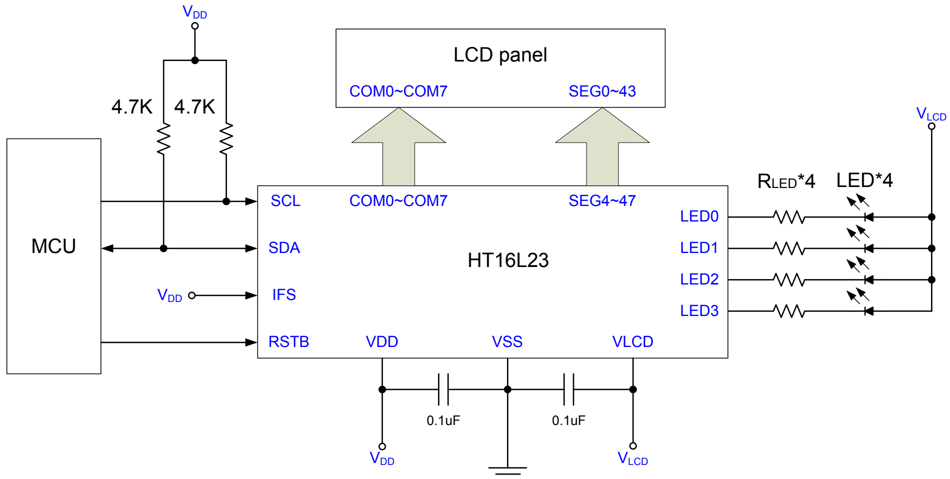



**(3) Use internal power on reset circuit only, the RSTB pin must be connected to $V_{DD}$**

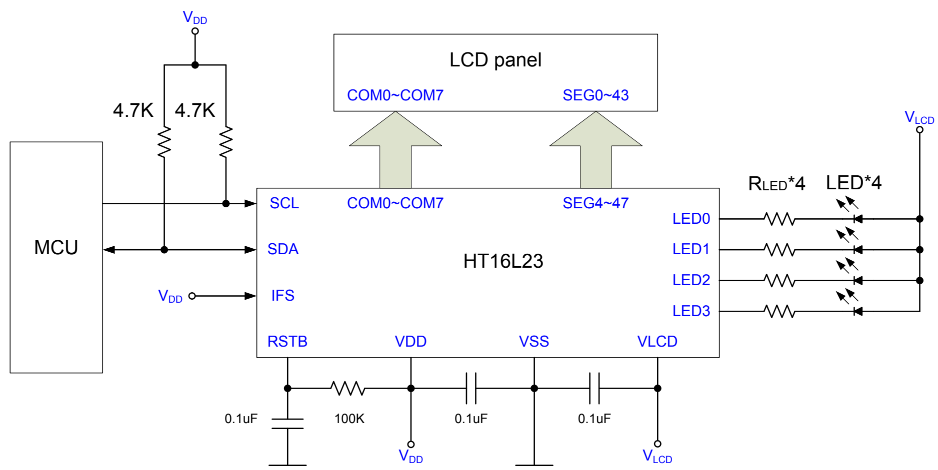


- **1/8 duty, [SP1:SP0]=10**

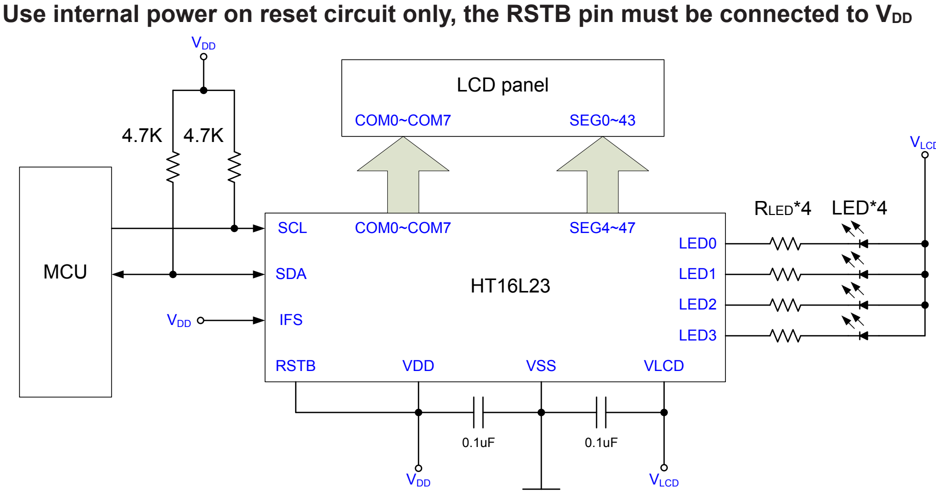
**(1) RSTB pin is connected to a MCU.**




**(2) RSTB pin is connected to external resistor and capacitor.**

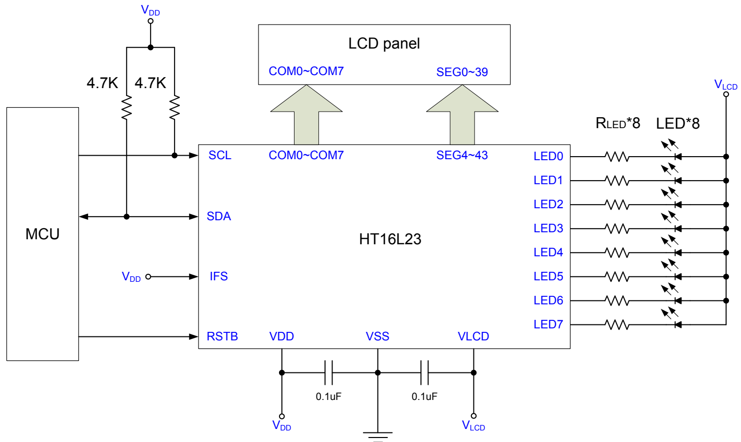



**(3) Use internal power on reset circuit only, the RSTB pin must be connected to $V_{DD}$**

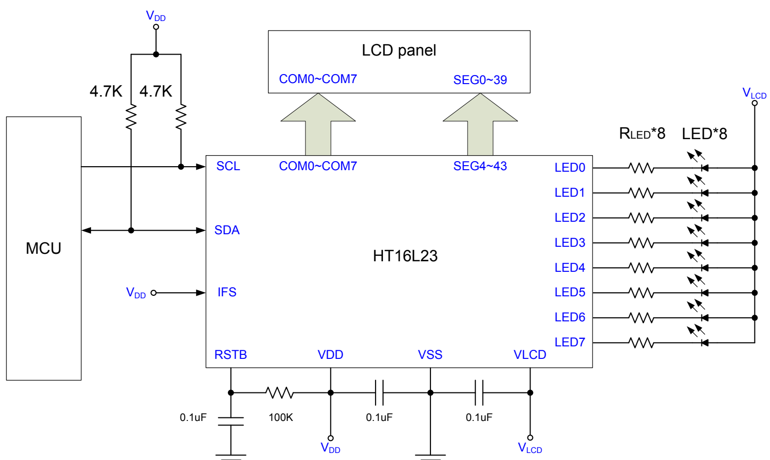


- **1/8 duty, [SP1:SP0]=11**

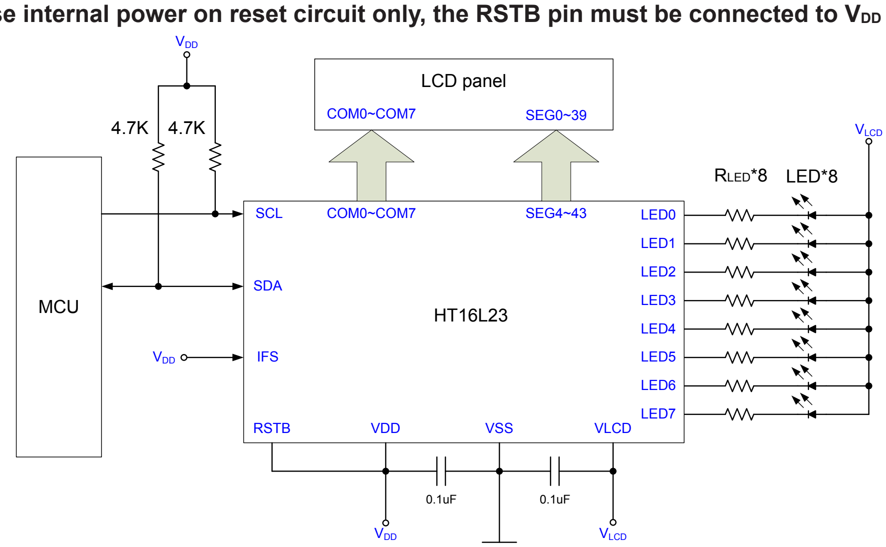
**(1) RSTB pin is connected to a MCU.**




**(2) RSTB pin is connected to external resistor and capacitor.**



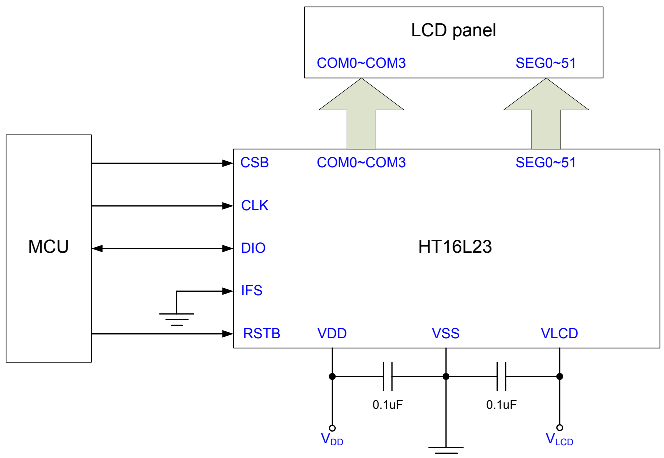

**(3) Use internal power on reset circuit only, the RSTB pin must be connected to $V_{DD}$**



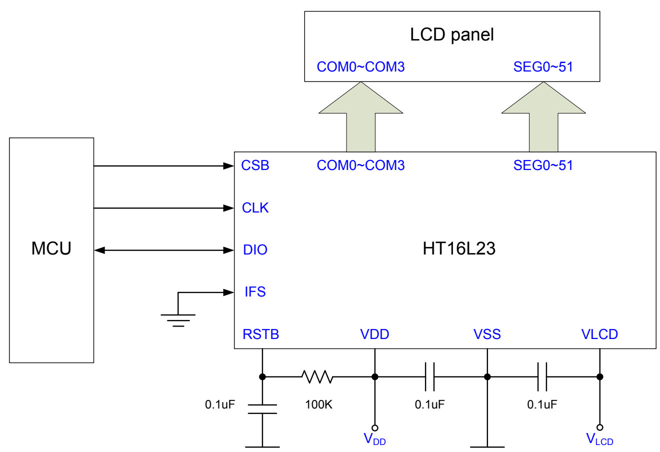
### SPI Interface

- **1/4 duty, [SP1:SP0]=0x**

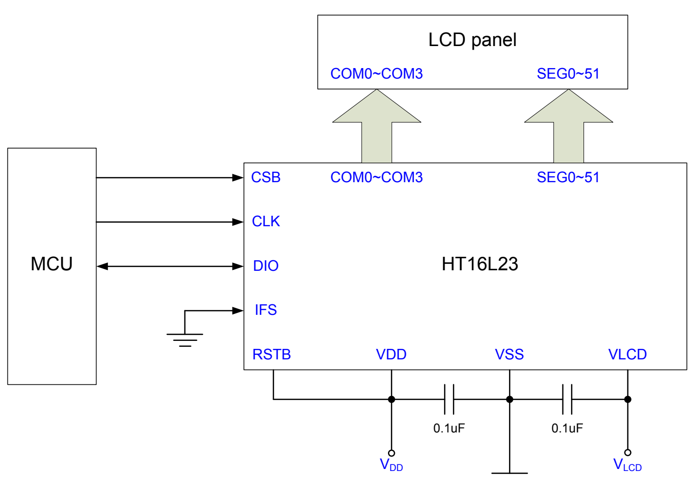
**(1) RSTB pin is connected to a MCU.**




**(2) RSTB pin is connected to external resistor and capacitor.**

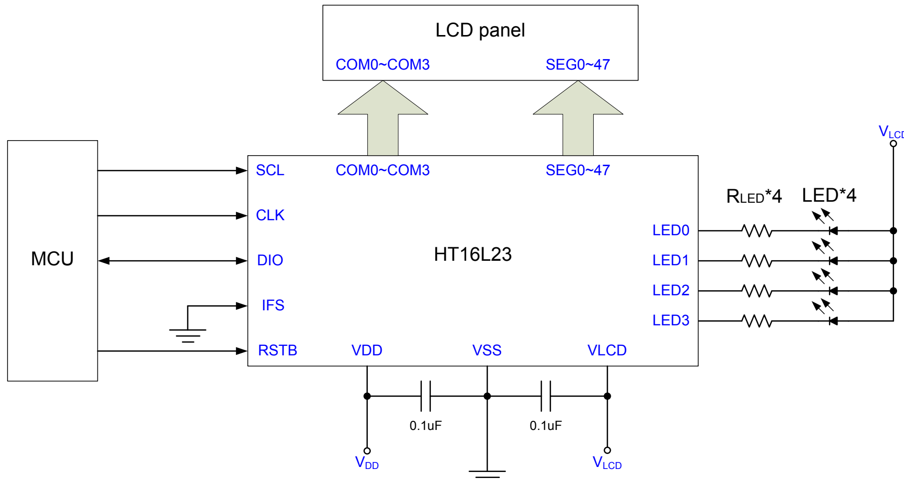



**(3) Use internal power on reset circuit only, the RSTB pin must be connected to $V_{DD}$**

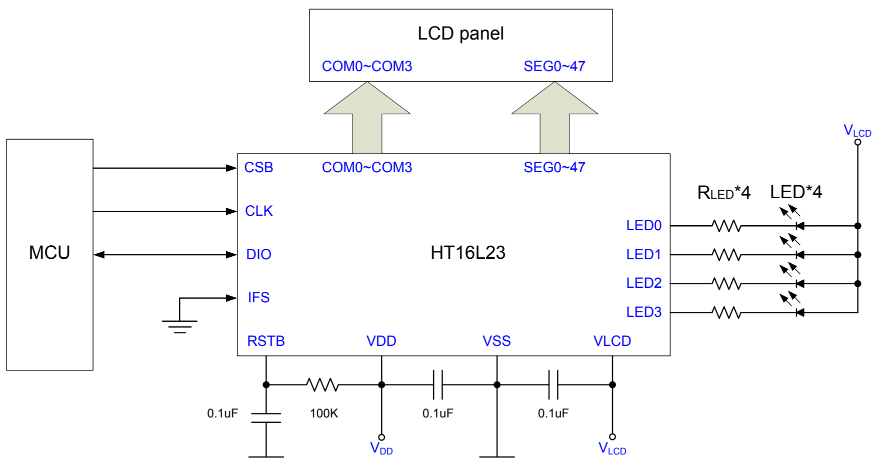


- **1/4 duty, [SP1:SP0]=10**

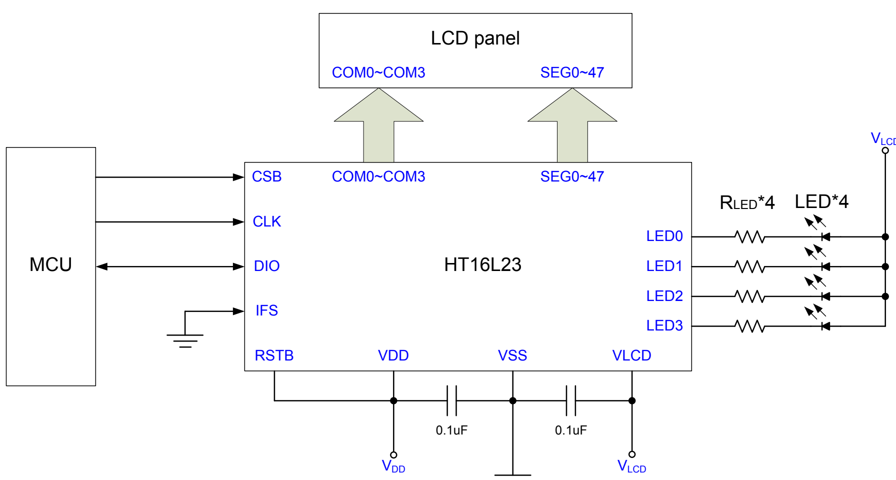
**(1) RSTB pin is connected to a MCU.**




**(2) RSTB pin is connected to external resistor and capacitor.**

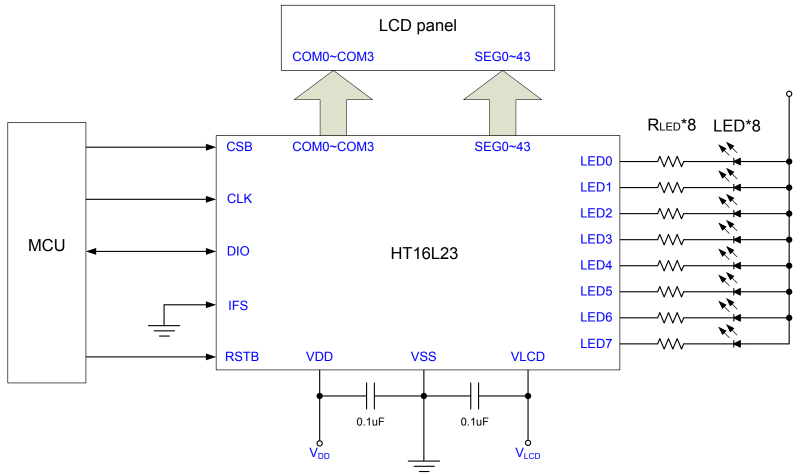



**(3) Use internal power on reset circuit only, the RSTB pin must be connected to $V_{DD}$**

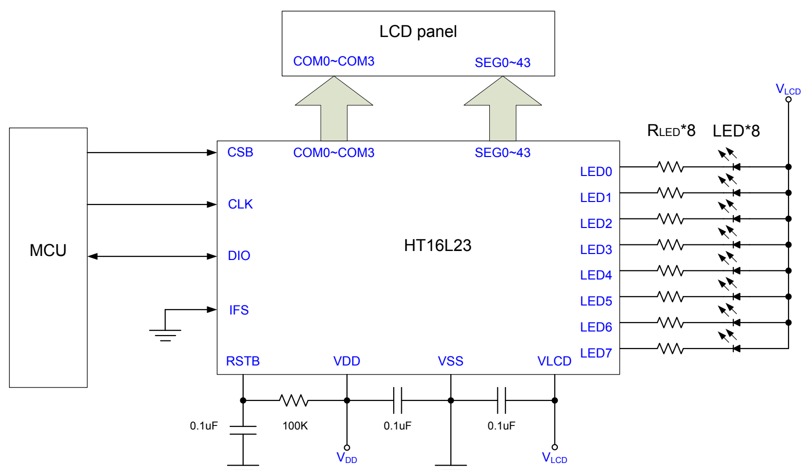


- **1/4 duty, [SP1:SP0]=11**

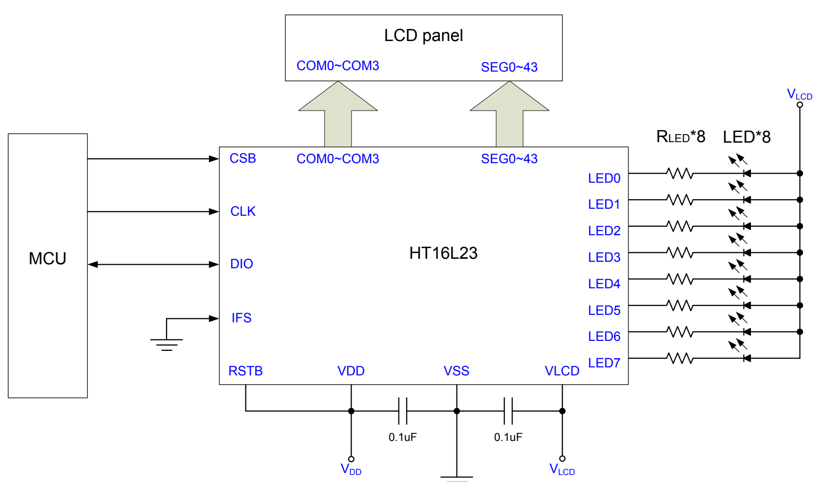
**(1) RSTB pin is connected to a MCU.**




**(2) RSTB pin is connected to external resistor and capacitor.**

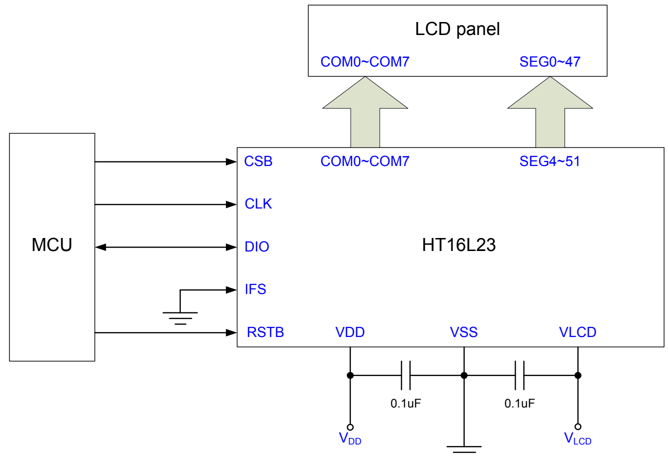



**(3) Use internal power on reset circuit only, the RSTB pin must be connected to $V_{DD}$**

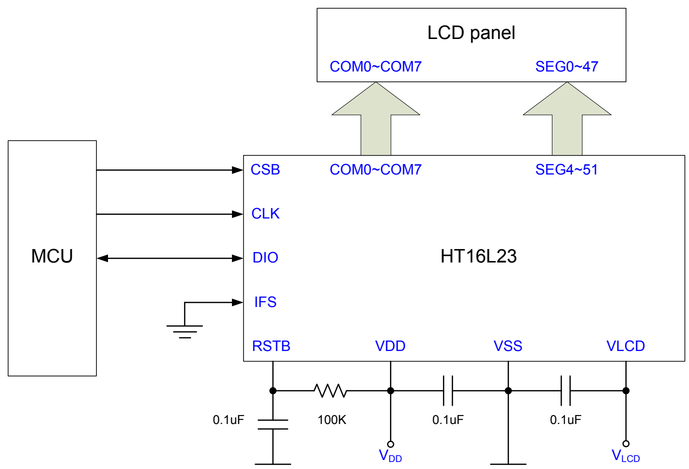


- **1/8 duty, [SP1:SP0]=0x**

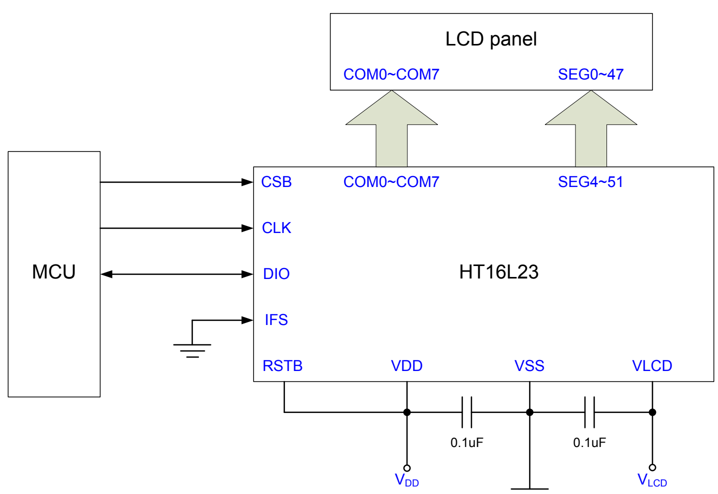
**(1) RSTB pin is connected to a MCU.**




**(2) RSTB pin is connected to external resistor and capacitor.**

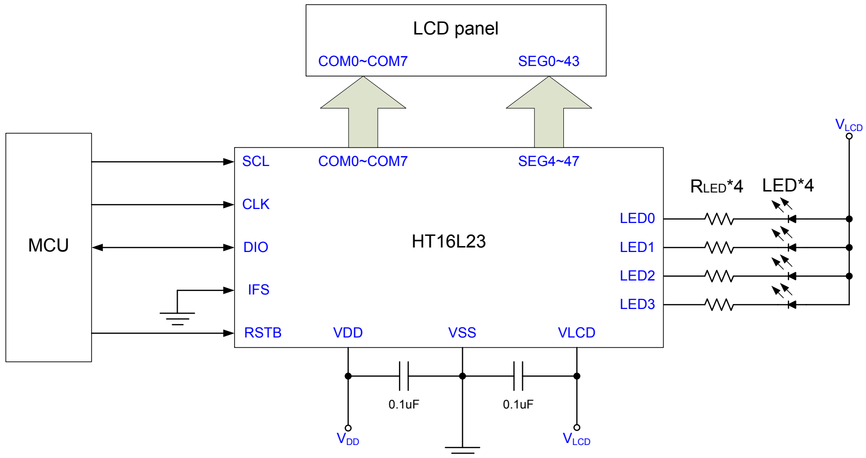



**(3) Use internal power on reset circuit only, the RSTB pin must be connected to $V_{DD}$**

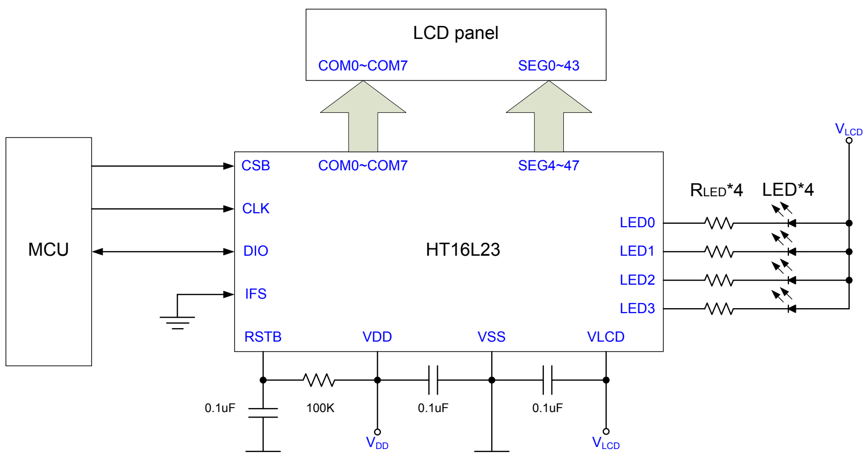


- **1/8 duty, [SP1:SP0]=10**

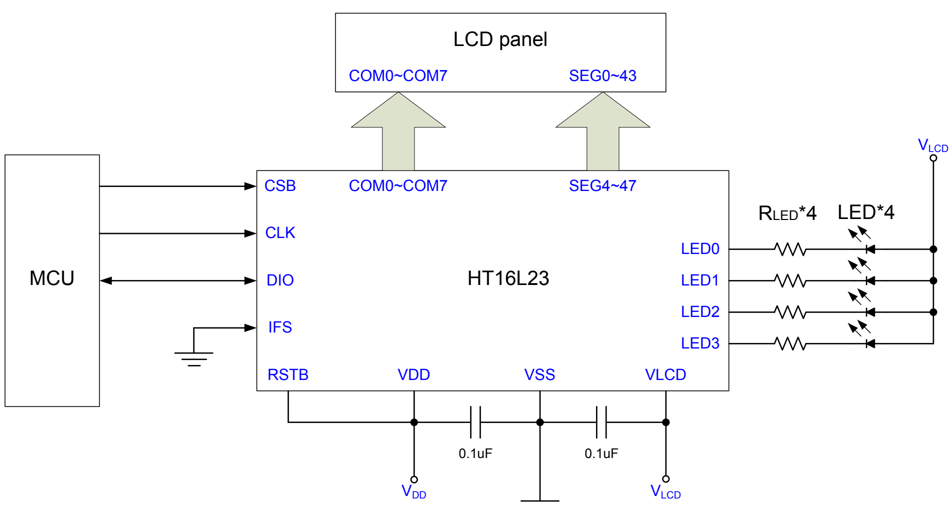
**(1) RSTB pin is connected to a MCU.**




**(2) RSTB pin is connected to external resistor and capacitor.**

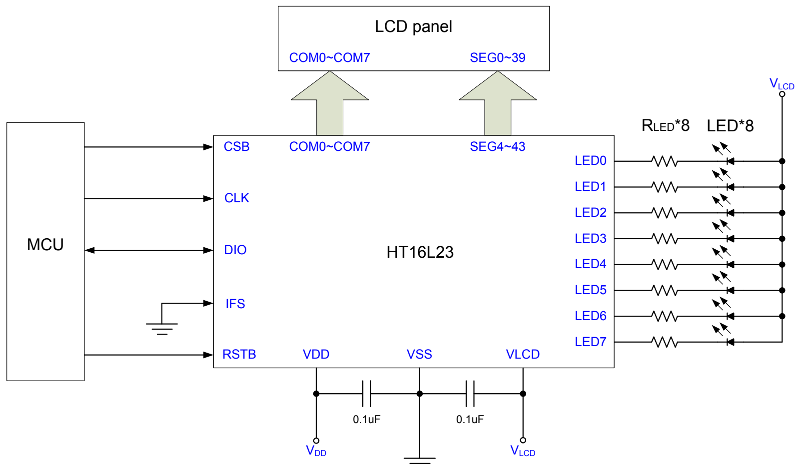



**(3) Use internal power on reset circuit only, the RSTB pin must be connected to $V_{DD}$**

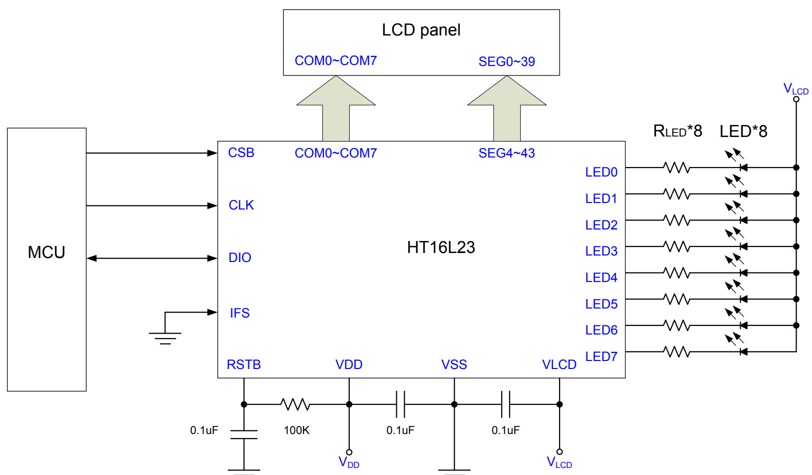


- **1/8 duty, [SP1:SP0]=11**

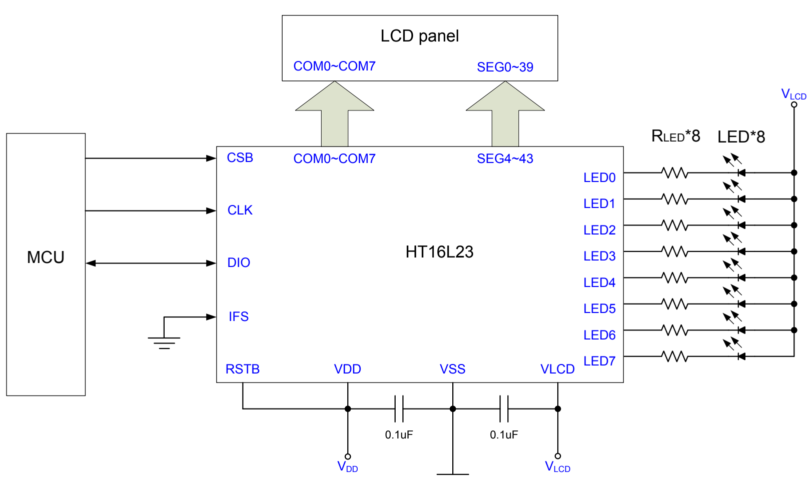
**(1) RSTB pin is connected to a MCU.**




**(2) RSTB pin is connected to external resistor and capacitor.**




**(3) Use internal power on reset circuit only, the RSTB pin must be connected to $V_{DD}$**



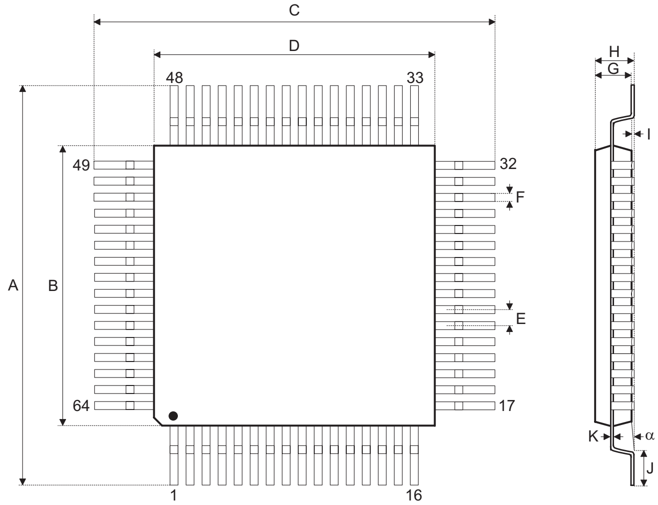
## Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

## 64-pin LQFP (7mm×7mm) Outline Dimensions




| Symbol | Dimensions in inch | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | 0.354 BSC | — |
| B | — | 0.276 BSC | — |
| C | — | 0.354 BSC | — |
| D | — | 0.276 BSC | — |
| E | — | 0.016 BSC | — |
| F | 0.005 | 0.007 | 0.009 |
| G | 0.053 | 0.055 | 0.057 |
| H | — | — | 0.063 |
| I | 0.002 | — | 0.006 |
| J | 0.018 | 0.024 | 0.030 |
| K | 0.004 | — | 0.008 |
| α | 0° | — | 7° |

| Symbol | Dimensions in mm | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | 9.00 BSC | — |
| B | — | 7.00 BSC | — |
| C | — | 9.00 BSC | — |
| D | — | 7.00 BSC | — |
| E | — | 0.40 BSC | — |
| F | 0.13 | 0.18 | 0.23 |
| G | 1.35 | 1.40 | 1.45 |
| H | — | — | 1.60 |
| I | 0.05 | — | 0.15 |
| J | 0.45 | 0.60 | 0.75 |
| K | 0.09 | — | 0.20 |
| α | 0° | — | 7° |