16×16 Constant Current LED Driver

HT16D33A/HT16D33B

Revision: V1.20 Date: August 06, 2019

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Features

- Logic Operating Voltage: 2.7V~5.5V
- LED Driver Operating Voltage: 4.5V~5.5V
- LED Display: 20 combinations of output pins (CA0 ~ CA19), can plan three matrix display mode
  - Matrix Type1: two groups of 9 rows and 10 commons LED Matrix. (Pins of the corresponding range: (CA0~CA9) + (CA10~CA19))
  - Matrix Type2: 12 rows and 12 commons. (Pins of the corresponding range: CA1~CA15)
  - Matrix Type3: 16 rows and 16 commons. (Pins of the corresponding range: CA1~CA19)
- LED Data RAM1 (Max.): 16 × 16 × 8 × (2) bits = (512) × 8 bits for Gray mode
- LED Data RAM2 (Max.): 16 × 16 × 4 × (2) bits = (256) × 8 bits for Fade mode
- LED Data RAM3 (Max.): 16 × 2 × 8 × (2) bits = (64) × 8 bits for LED On/Off Control
- Integrated 2.4MHz RC oscillator
- 2 frame memory for animations
- 256-level global brightness scale
- Binary scale mode or Gray scale mode
- Global blinking or fade function
- Automatic scroll function: left/right
- Internal Current Reference Control
- Support max. 48mA Sink Constant Current
- 16-level Maximum current setup selection
- Current matching to ±3%
- Over temperature protection circuit
- Open/short protection circuit for each dot
- I^2C-bus or SPI 3-wire Interface
- Cascade function for extend applications
- Package types: 24-pin SSOP-EP, 28-pin SSOP and 32-pin QFN

Applications

- Industrial control displays
- Mobile phones
- Traffic signboards and information displays
- Digital clocks, thermometers, counters, electronic meters
- Instrumentation readouts
- Other consumer applications
- LED displays

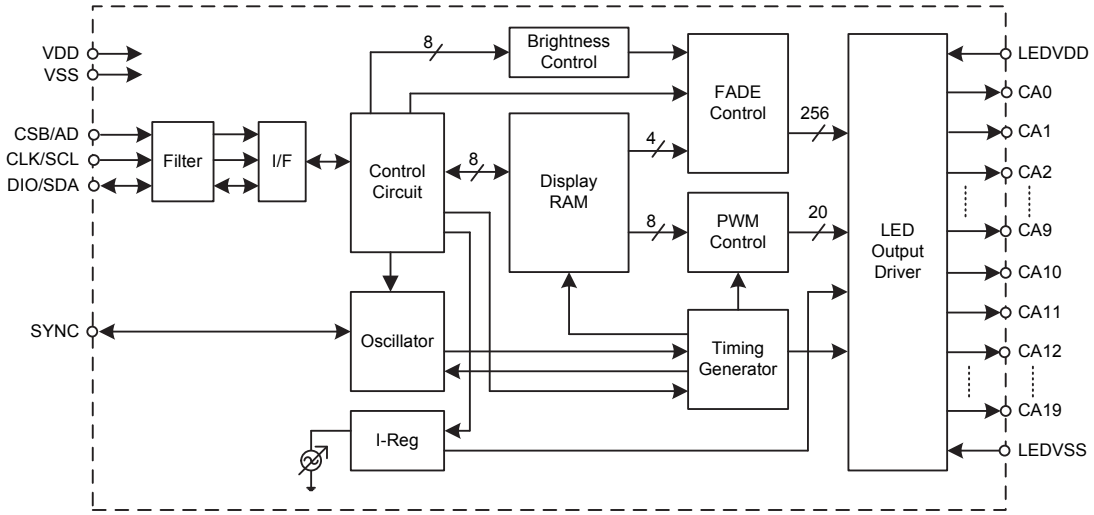
General Description

The HT16D33A and HT16D33B are high accuracy constant current and memory mapping LED display controller/drivers. The maximum display capacity of the devices is 256 patterns composed of 16 rows and 16 commons. The devices can generate a 256 step Gray Scale (PWM data) using software controlled PWM circuitry and 256 LED illumination levels using software controlled PWM circuitry. The devices provide constant current output control using software controlled for each row output terminal. A serial interface is provided to allow the devices to receive instructions for its command mode and data mode. Only three lines are required for device interfacing to a host controller. The display capacity can be easily extended by cascading the devices thus expanding its application possibilities. The devices are compatible with most microcontrollers offering easy interfacing via their two serial interfaces, an I^2C interface or an SPI 3-wire serial interface.

Selection Table

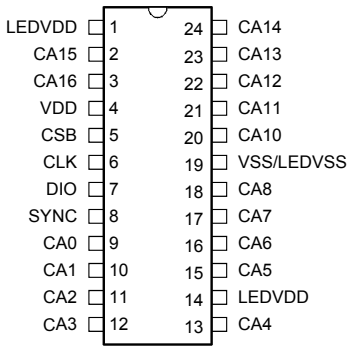
Part Number	Interface
HT16D33A	3-wire SPI
HT16D33B	I^2C

Block Diagram

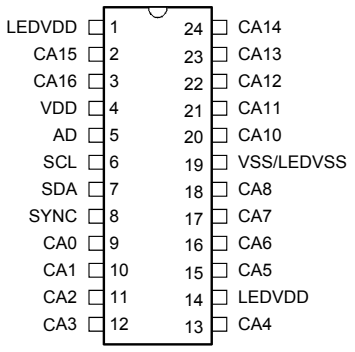


Note: This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

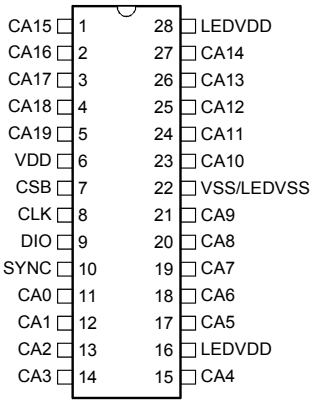
Pin Assignment



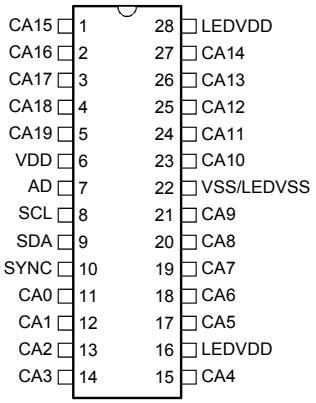
HT16D33A
24 SSOP-EP-A



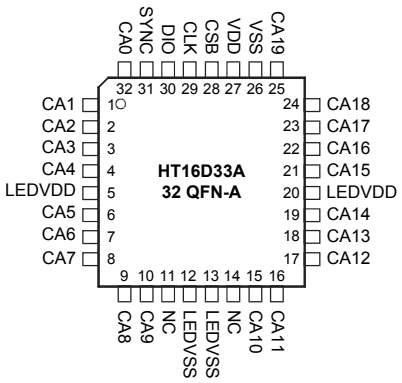
HT16D33B
24 SSOP-EP-A

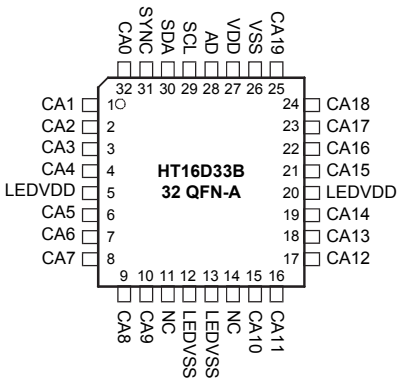


HT16D33A
28 SSOP-A



HT16D33B
28 SSOP-A





	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
32QFN																				
SCAN	S0_1	S1_1	S2_1	S3_1	S4_1	S5_1	S6_1	S7_1	S8_1	S9-1	S0_2	S1_2	S2_2	S3_2	S4_2	S5_2	S6_2	S7_2	S8_2	S9-2
9×10×2	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	CA14	CA15	CA16	CA17	CA18	CA19
SCAN		S1	S2	S3	S4	S5	S6	S7	S8		S9		S10	S11	S12	S13	S14	S15	S16	S17
12×12		CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8		CA10		CA12	CA13	CA14	CA15				
16×16		CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8		CA10		CA12	CA13	CA14	CA15	CA16	CA17	CA18	CA19
28SSOP																				
SCAN	S0_1	S1_1	S2_1	S3_1	S4_1	S5_1	S6_1	S7_1	S8_1	S9-1	S0_2	S1_2	S2_2	S3_2	S4_2	S5_2	S6_2	S7_2	S8_2	S9-2
9×10×2	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	CA14	CA15	CA16	CA17	CA18	CA19
SCAN		S1	S2	S3	S4	S5	S6	S7	S8		S9		S10	S11	S12	S13	S14	S15	S16	S17
12×12		CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8		CA10		CA12	CA13	CA14	CA15				
16×16		CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8		CA10		CA12	CA13	CA14	CA15	CA16	CA17	CA18	CA19
24SSOP-EP																				
SCAN	S0_1	S1_1	S2_1	S3_1	S4_1	S5_1	S6_1	S7_1	S8_1	S9-1	S0_2	S1_2	S2_2	S3_2	S4_2	S5_2	S6_2	S7_2	S8_2	S9-2
9×10×2	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8		CA10	CA11	CA12	CA13	CA14	CA15	CA16			
SCAN		S1	S2	S3	S4	S5	S6	S7	S8		S9		S10	S11	S12	S13	S14	S15	S16	S17
12×12		CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8		CA10		CA12	CA13	CA14	CA15				
16×16		CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8		CA10		CA12	CA13	CA14	CA15	CA16			

Note: in 12×12 and 16×16 modes, the CA0, CA9 and CA11 pin outputs are HI-z.

Output Pin	CA0	CA9	CA11	CA16	CA17	CA18	CA19
12×12	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z
16×16	HI-Z	HI-Z	HI-Z	CA16	CA17	CA18	CA19

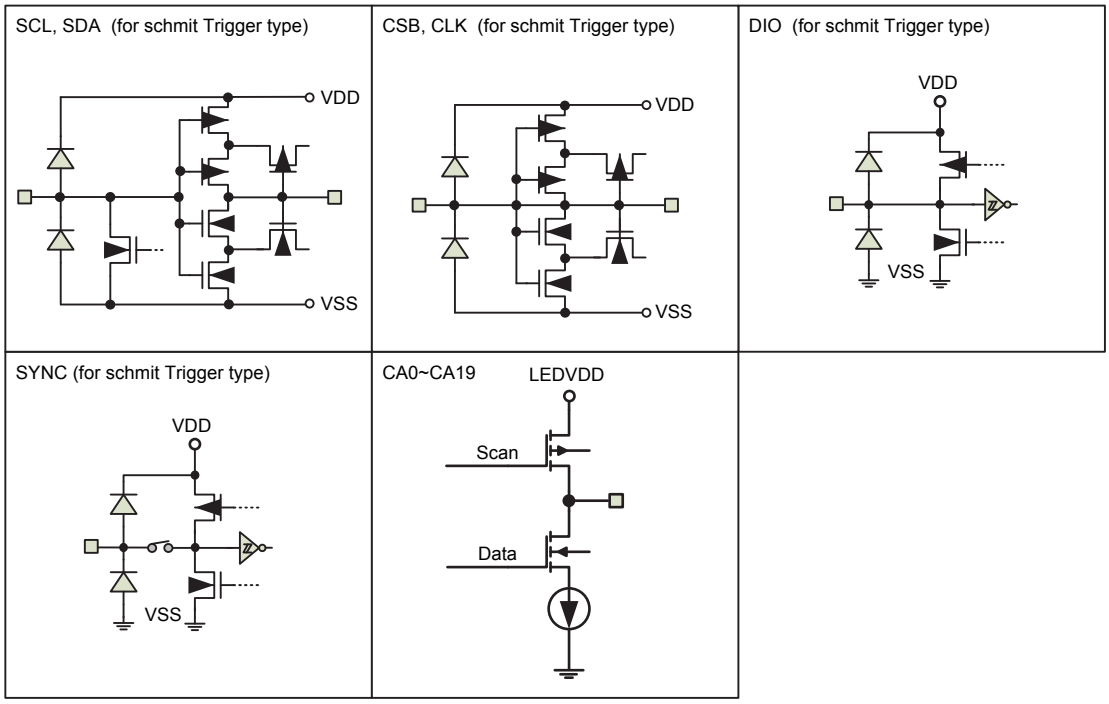
Package	Maximum Display Pixel		
	Matrix Type1 (9×10×2 Mode)	Matrix Type2 (12×12 Mode)	Matrix Type3 (16×16 Mode)
32QFN	180	144	256
28SSOP	180	144	256
24SSOP-EP	114	144	182

Pin Description

Pin Name	Type	Function
VDD	—	Positive power supply for logic circuit
VSS	—	Negative power supply for logic circuit, ground
LEDVDD	—	Positive power supply for driver circuit
LEDVSS	—	Negative power supply for driver circuit, ground
AD/CSB	I	I²C interface device address data set input pin for I²C interface Chip Select pin for SPI 3-wire Interface
SCL/CLK	I	Serial clock input pin Serial Clock (SCL) Input for I²C interface Serial Clock (CLK) Input for SPI 3-wire Interface
SDA/DIO	I/O	Serial data input/output pin. Data is input to or comes out from the shift register at rising edge of the clock I²C interface serial data (SDA) Input/Output – NMOS open-drain output SPI 3-wire serial interface serial data input/output – CMOS output
SYNC	I/O	Synchronization clock Input/output pin If the Master Mode command is programmed, the system clock is sourced from the internal RC oscillator and output on the SYNC pin. If the Slave Mode command is programmed, the system clock is input on the SYNC pin.
CA0~CA19	I/O	LED combinations of output pins. (row and commons combo pins) Constant current circuit, PWM control output pins, Control switch pin for matrix driver.
NC	—	No connection

Note: for SYNC and CA0~CA19 pins, the pin processing at unused is open.

Approximate Internal Connections



Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to V_{SS}+6.0V
Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V
Operating Temperature ..... -40°C to 85°C
Storage Temperature ..... -50°C to 125°C
Thermal Resistance (Rth) (24-pin SSOP-EP) ..... 35.3°C/W
(28-pin SSOP) ..... 80°C/W
(32-pin QFN) ..... 47°C/W
Max junction Temperature (Tj) ..... 125°C
Power Dissipation (PD) (Ta=25°C) (24-pin SSOP-EP) 2.83W
(Ta=85°C) (24-pin SSOP-EP) 1.13W
(Ta=25°C) (28-pin SSOP) 1.25W
(Ta=85°C) (28-pin SSOP) 0.50W
(Ta=25°C) (32-pin QFN) 2.13W
(Ta=85°C) (32-pin QFN) 0.85W
CAn Output Current (Single pin) 100mA
Total Power Line Current (Ta=25°C) 1000mA

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

V_{DD}=5V, LED_V_{DD}=5V, Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Logic Supply Voltage	—	—	2.7	—	5.5	V
LED_V_{DD}	LED Supply Voltage	—	—	4.5	—	5.5	V
I_{STB}	Standby Current	5V	No load, Power down mode, Matrix-type1 (System OSC off, LED display off)	—	1.0	2.0	μA
I_{DD}	Operating Current	5V	No load, LED ON, Matrix-type1, Constant current ratio set=33mA, Internal RC OSC, Output all on	—	4.5	7.0	mA
I_{LED_VDD}	Operating Current	5V	No load, LED ON, Matrix-type1, Constant current ratio set=33mA, Internal RC OSC, Output all on	—	2.1	3.5	mA
V_{IH}	Input High Voltage	5V	DIO, CLK, SDA, SCL, CSB, SYNC	0.7V_{DD}	—	5.0	V
V_{IL}	Input Low Voltage	5V	DIO, CLK, SDA, SCL, CSB, SYNC	0	—	0.3V_{DD}	V
I_{OH}	High Level Output Current	5V	V_{OH}=4.5V, SYNC, DIO	-10	-13	—	mA
I_{OL}	Low Level Output Current	5V	V_{OL}=0.5V, SYNC, DIO, SDA	18	25	—	mA
I_{CA_OH}	CAn Source Current	5V	Constant current ratio set=33mA, V_{OH}=4.5V, Matrix-type1	315	460	—	mA
I_{CA_OL}	CAn Constant Current	5V	Constant current ratio set=33mA, V_{DS}=0.7V~2V, Matrix-type1	—	33	—	mA
dI_{CA1} (1)	Bit Current Skew	5V	Constant current ratio set=33mA, V_{DS}=1V, Matrix-type1	—	±3.0	±5.0	%
dI_{CA2} (2)	Channel Current Skew	5V	Constant current ratio set=33mA, V_{DS}=1V, Matrix-type1	—	±3.0	±5.0	%
%/dV_{DS} (3)	Output Current vs. Output Voltage Regulation	5V	Constant current ratio set=33mA, V_{DS}=0.7V~2.0V, V_{DD}=5.0V, Matrix-type1	—	±0.3	±0.5	%/V
%/dV_{DD} (4)	Output Current vs. Supply Voltage Regulation	—	Constant current ratio set=33mA, V_{DD}=4.5V~5.5V, V_{DS}=1.0V, Matrix-type1	—	—	±1.0	%/V

Note: 1. Bit Skew:

$$\text{Pin } dI_{CA1}\,(\%) = \frac{I_{CA\_(n+1)}\,(V_{DS}=1V) - I_{CA\_n}\,(V_{DS}=1V)}{I_{CA\_(n+1)}\,(V_{DS}=1V) + I_{CA\_n}\,(V_{DS}=1V)\,/\,2} \times 100\% \quad \text{(n: CA pin number)}$$

2. Channel Skew:

$$+\,dI_{CA2}\,(\%) = \frac{I_{CA\_MAX} - I_{CA\_AVG}}{I_{CA\_AVG}} \times 100\% \quad \text{(n: CA pin number)}$$

$$-\,dI_{CA2}\,(\%) = \frac{I_{CA\_MIN} - I_{CA\_AVG}}{I_{CA\_AVG}} \times 100\% \quad \text{(n: CA pin number)}$$

Where:

I_{CA_AVG}: the average I_{CA} for all CA pins on V_{DS}=1V

I_{CA_MAX}: the max I_{CA} of all CA pins on V_{DS}=1.0V

I_{CA_MIN}: the min I_{CA} of all CA pins on V_{DS}=1.0V

3. $$\%/dV_{DS}\,(\%/V) = \frac{I_{CA\_MAX} - I_{CA\_MIN}}{(2.0V - 0.7V) \times I_{CA\_AVG}} \times 100\%$$

Where:

I_{CA_AVG}: the average I_{CA} for each CA pin between V_{DS}=0.7V and 2.0V

I_{CA_MAX}: the max I_{CA} of each CA pin between V_{DS}=0.7V and 2.0V

I_{CA_MIN}: the min I_{CA} of each CA pin between V_{DS}=0.7V and 2.0V

4. $$\%/dV_{DD}\,(\%/V) = \frac{I_{CA\_MAX} - I_{CA\_MIN}}{(5.5V - 4.5V) \times I_{CA\_AVG}} \times 100\%$$

Where:

I_{CA_AVG} : the average I_{CA} for each CA pin between V_{DD}=4.5V and 5.5V

I_{CA_MAX}: the max I_{CA} of each CA pin between V_{DD}=4.5V and 5.5V

I_{CA_MIN}: the min I_{CA} of each CA pin between V_{DD}=4.5V and 5.5V

V_{DS}=1V

5. Application condition of power supply: LED_$V_{DD} \geq V_{DD}$

A.C. Characteristics

V_{DD}=2.7V~5.5V, Ta=25°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{SYS}	System Clock	On-chip RC oscillator	2.1	2.4	2.7	MHz
f_{LED}	LED Frame Rate	Matrix-type1 (9×10 + 9×10)	—	882	—	Hz
		Matrix-type2 (12×12)	—	735	—	Hz
		Matrix-type3 (16×16)	—	551	—	Hz
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	—	—	—	100	mV
RR_{VDD}	V_{DD} Rise Rate to Ensure Power-on Reset	—	0.05	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} Stay at V_{POR} to Ensure Power- on reset	—	10	—	—	ms

A.C. Characteristics – SPI 3-wire Serial Bus

V_{DD}=2.7V~5.5V, Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
t_{CLK}	Clock Cycle Time	—		250	—	—	ns
t_{CW}	Clock Pulse Width	—		100	—	—	ns
t_{DS}	Data Setup Time	—		50	—	—	ns
t_{HS}	Data Hold Time	—		50	—	—	ns
t_{CSW}	"H" CSB Pulse Width	—		100	—	—	ns
t_{CSL}	CSB Setup Time (CSB↓ – CLK↓)	—		50	—	—	ns
t_{CSH}	CS Hold Time (CLK↑ – CSB↑)	—		4	—	—	µs
t_{PD}	Data Output Delay Time (CLK – DIO)	C_O=15pF	t_{PD}=10 to 90%	—	—	350	ns
			t_{PD}=10 to 10%				

A.C. Characteristics – I²C Serial Bus

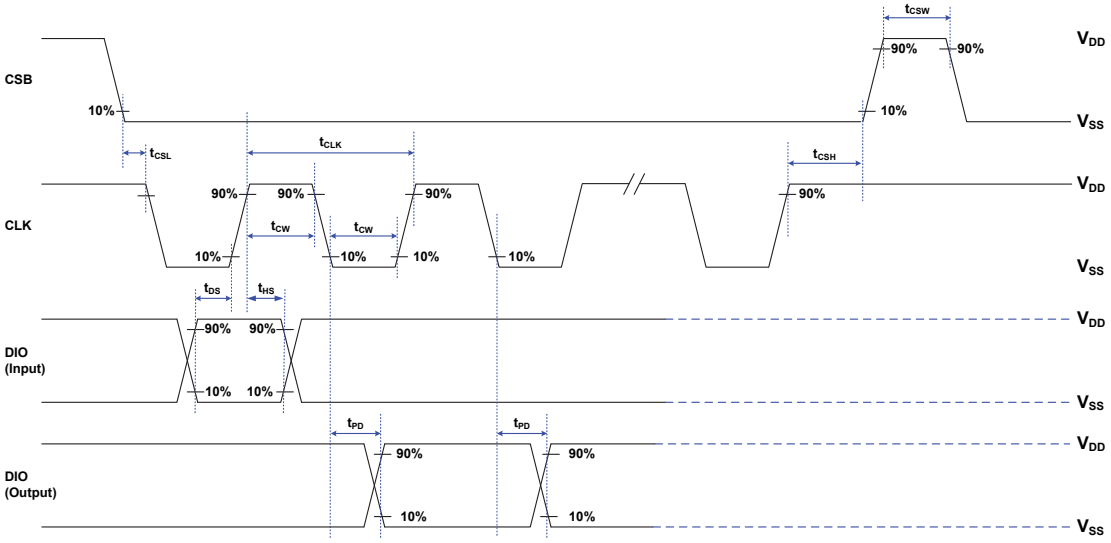
Ta=25°C

Symbol	Parameter	Conditions	V_{DD}=2.4V~5.5V		V_{DD}=3.0V~5.5V		Unit
			Min.	Max.	Min.	Max.	
f_{SCL}	Clock Frequency	—	—	100	—	400	kHz
t_{BUF}	Bus Free Time	Time in which the bus must be free before a new transmission can start	4.7	—	1.3	—	µs
$t_{HD:STA}$	Start Condition Hold Time	After this period, the first clock pulse is generated	4.0	—	0.6	—	µs
t_{LOW}	SCL Low Time	—	4.7	—	1.3	—	µs
t_{HIGH}	SCL High Time	—	4.0	—	0.6	—	µs
$t_{SU:STA}$	Start Condition Setup Time	Only relevant for repeated START condition	4.7	—	0.6	—	µs
$t_{HD:DAT}$	Data Hold Time	—	0	—	0	—	ns
$t_{SU:DAT}$	Data Setup Time	—	250	—	100	—	ns
t_R Note	SDA and SCL Rise Time	—	—	1.0	—	0.3	µs
t_F Note	SDA and SCL Fall Time	—	—	0.3	—	0.3	µs
$t_{SU:STO}$	Stop Condition Setup Time	—	4.0	—	0.6	—	µs
t_{AA}	Output Valid from Clock	—	—	3.5	—	0.9	µs
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	20	—	20	ns

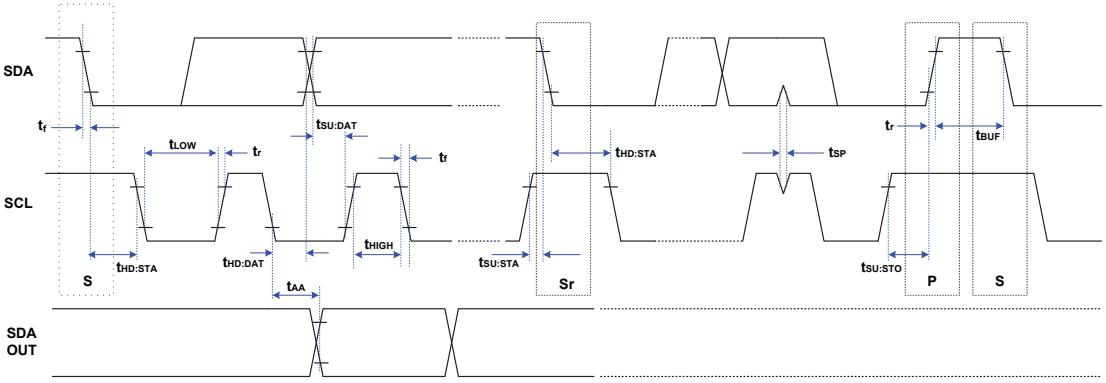
Note: These parameters are periodically sampled but not 100% tested.

Timing Diagrams

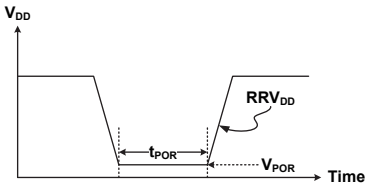
SPI 3-wire Serial Bus Timing



I²C Bus Timing



Power on Reset Timing



Note: 1. If the conditions of Reset timing are not satisfied in power On/Off sequence, the internal Power on Reset (POR) circuit will not operate normally.
2. If it is difficult to meet power on reset timing conditions, please execute software reset command after Power on.

Functional Description

Power-on Reset

After power is applied the device will be initialised by an internal power-on reset circuit. The internal circuit status after initialisation is as follows:

- All registers are set to their default value, but the contents of the DDRAM are not affected
- System Oscillator will be off
- All CA outputs and SYNC pin status will be high impedance
- The LED display will be in an off state

Data transfers on the I²C-bus or SPI 3-wire serial bus should be avoided for 1ms following a power-on to allow the reset initialisation operation to complete.

LED Driver

The HT16D33A/HT16D33B is a 256 pattern LED driver which can be configured as 9×10×2 or 12×12 or 16×16 pattern by using the Configuration Mode command. This feature makes the HT16D33A/HT16D33B suitable for multiple LED applications.

System Oscillator

The internal logic and the LED drive signals of the HT16D33A/HT16D33B are timed by the integrated RC oscillator.

The System Clock frequency determines the LED frame frequency. A clock signal must always be supplied to the device. Removing the clock may freeze the device if the standby mode command is executed. At initial system power on, the system oscillator is in the stop state.

Driver Outputs

The LED driver offers a 16×16 LED Matrix with 1/16 cycle rate. The required lines to driver all 256 LEDs are reduced to 16 by using the cross-plexing feature optimizing space on the PCB. The driver output signals are generated in accordance with the data resident in the display latch, Each CA pin (CA0~CA19) can be switched to VSS via the internal current sink (“low”), to VDD (“high”) or not connected (“high-Z, HI-Z”).

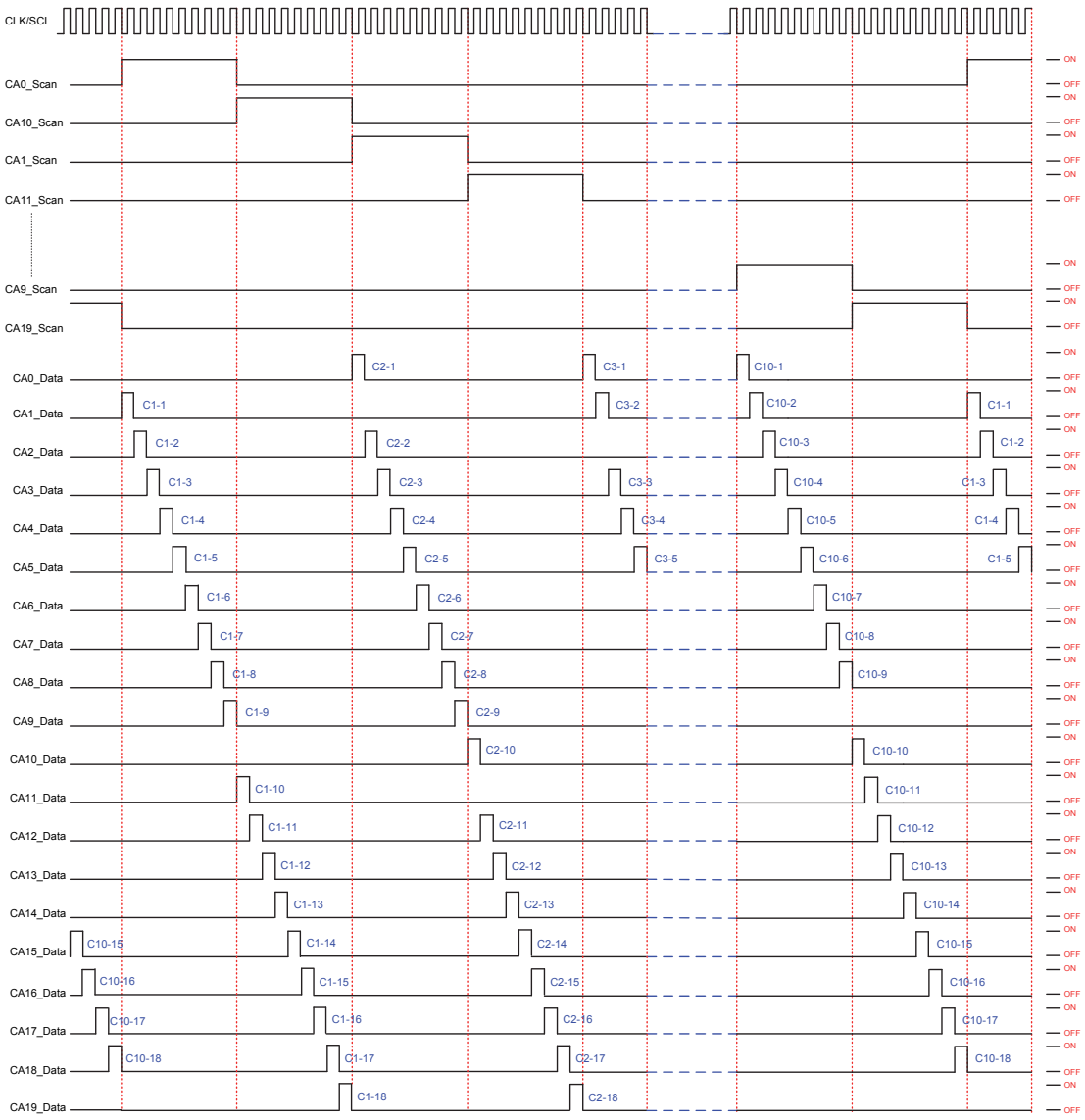
Address Pointer

The addressing mechanism for the display RAM is implemented using the address pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialisation of the address pointer using the Address pointer command.

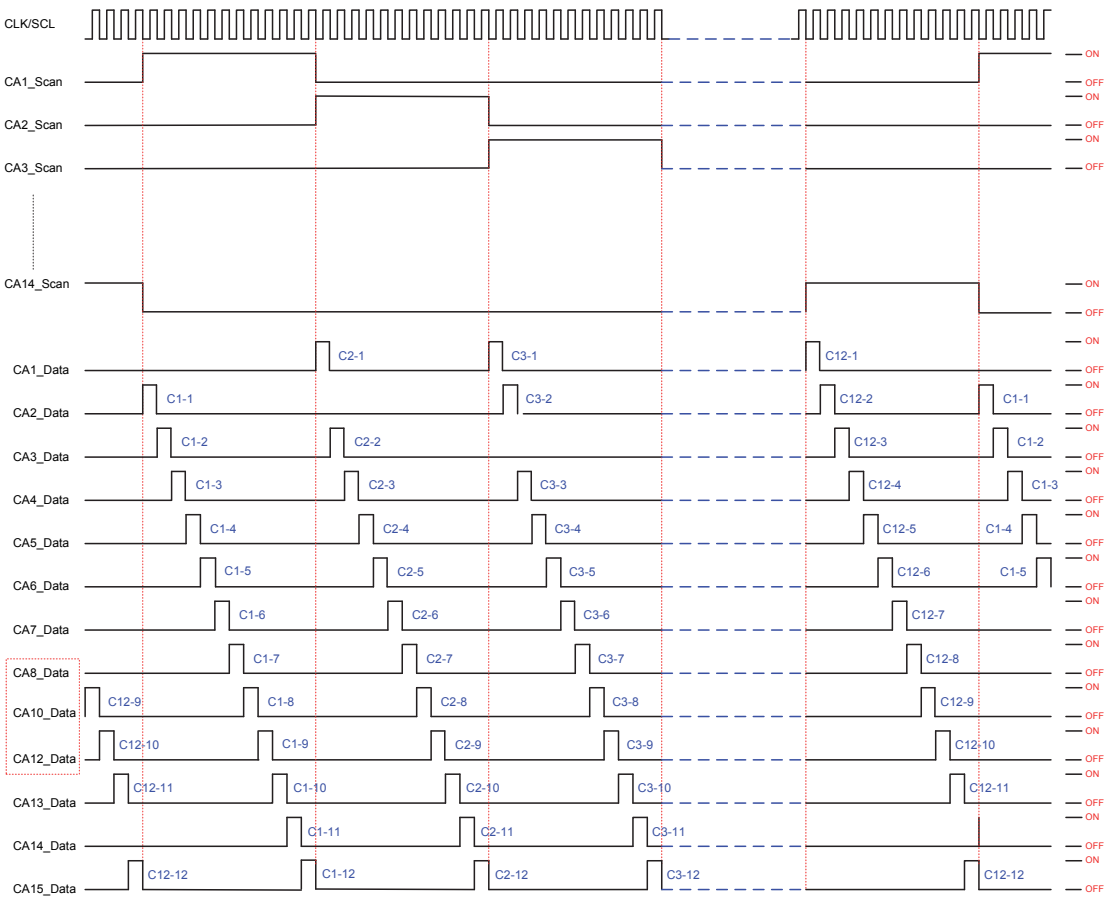
Open/Short Detection Function

These devices include open /short detection function that the open/short condition of the LED can be detected. It is recommended to implement the detection before using the devices for actual applications.

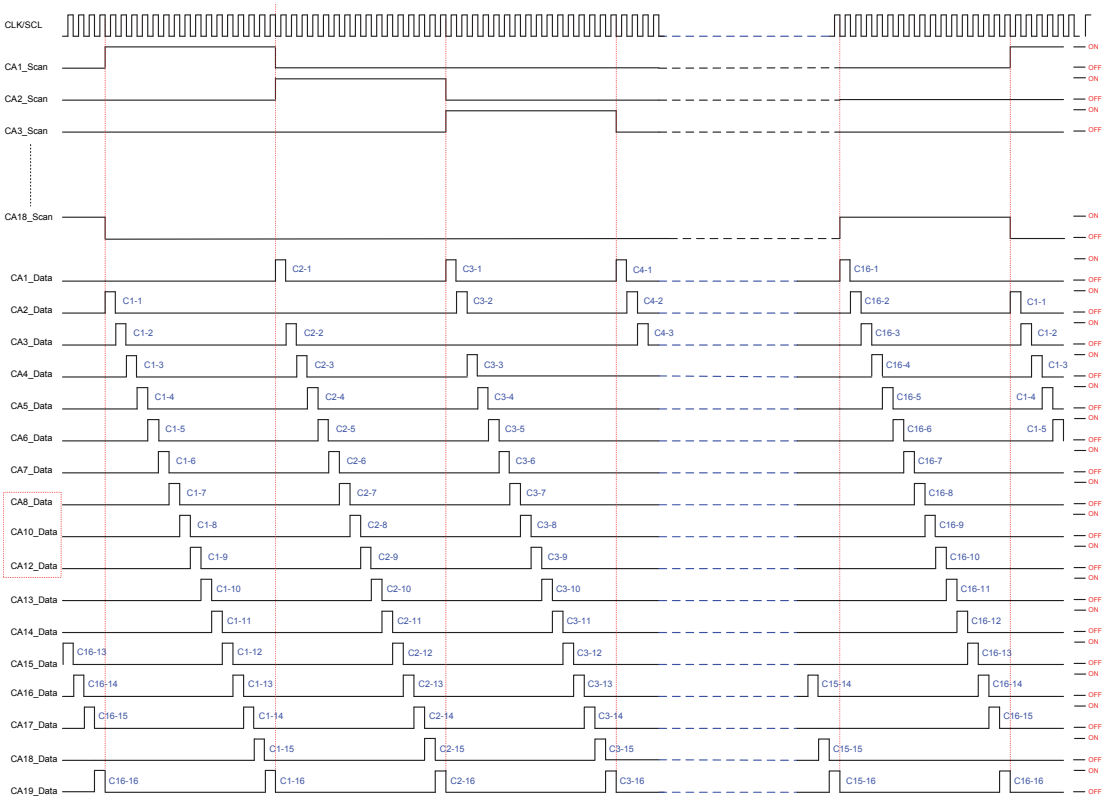
Matrix-type1: 9×10 + 9×10



Matrix-type2: 12×12



Matrix-type3: 16×16



- When Open/Short detection is enabled and input CLK/SCL clock is input, the detection starts. The CAn detection time is equal to the input CLK/SCL clock pulse width. The CAn_Scan will scan for one time (from CA1_Scan to CA16_Scan). During CAn_Scan scanning period, all the CAx_Data except the corresponding CAn_Scan will be scanned. (E.g. when CA1_Scan turns on, CA2_Data to CA17_Data will scan but CA1_Data will be skipped.) As shown above, individual LED is checked for open or short condition during the scan.
- During the CAn_Scan active period, output CAn terminal pin voltages will be compared with two reference voltages to determine whether LED is open or short. Open or short condition of each LED can be read back by reading short detection data register and open detection data register.
- LED is detected as "OPEN" state when the detected constant current output voltage at IO is over LED_V_{SS} + 0.5V. And it is only valid when the corresponding bit in Open Data RAM is set as '1'.
- LED is detected as 'SHORT' state when the detected constant current output voltage at IO is under LED_V_{DD} - 0.5V. And it is only valid if the corresponding bit in Short Data RAM is set as '1'.

Over Temperature Protection

The device includes thermal protection circuitry. When the junction temperatures exceed a certain detection temperature the temperature protection circuit is activated. The TSDF flag bit is set to "1", the display will be off and the direct pins will be turned off.

When the chip junction temperatures exceeds 150°C, the entire IC display is turned off and the direct pins will also be turned off along with the TSDF flag bit being set to "1". The device will resume operation (normal display) and turn on the direct pins and the TSDF flag bit will be cleared to "0" when the chip junction temperature falls below 125°C.

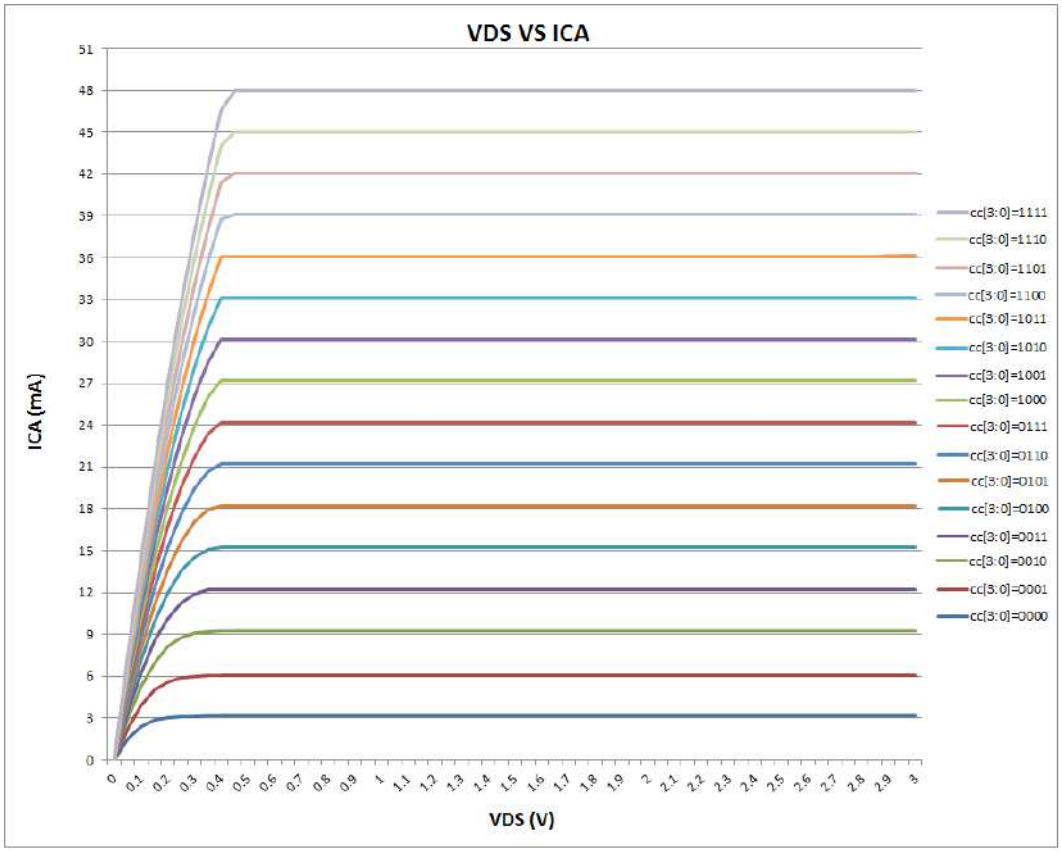
The temperature protection function has a detection temperature of about 150°C. But as the detection temperature function includes hysteresis, its release temperature is about 125°C (Design reference value).

Constant Current Output

The Constant current output of each CA pin output channel can be setup internally. The current scale range can be adjusted by using the Constant Current Ratio command. The maximum current variation between channels is less than ±3%. The characteristics curve of output stage in the saturation region is flat for which users can refer to the charts below. The output current remains constant regardless of the LED forward voltage (V_F) variations.

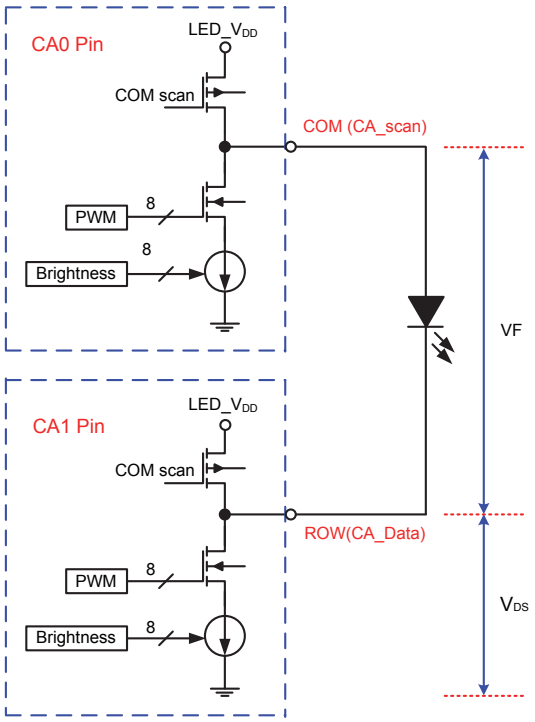
The output current (I_{CA}) scale range can be adjusted by using the Constant Current Ratio command. The maximum LED current is up to 48mA.

The default relationship between I_{CA} and Constant Current Ratio command set value is shown in the following figure.



Load Supply Voltage – LED_V_{DD}

The device can be operated satisfactorily when V_{DS} lies in a range of 0.7V to 2.0V. It is recommended to use a low supply voltage for LED_V_{DD} to reduce the V_{DS} value which will reduce both the power consumption and subsequent device temperature.



Display Data RAM – DDRAM

In the Binary Mode, the display RAM is a static 32×8-bit RAM in which the LED data is stored. A logic "1" in the RAM bit-map indicates an "on" state of the corresponding LED ROW. Similarly a logic "0" indicates an "off" state. There is a one-to-one correspondence between the display memory addresses and the CA pin outputs, and between the individual bits of a RAM word and the column outputs.

The following shows the mapping from the RAM to the LED pattern.

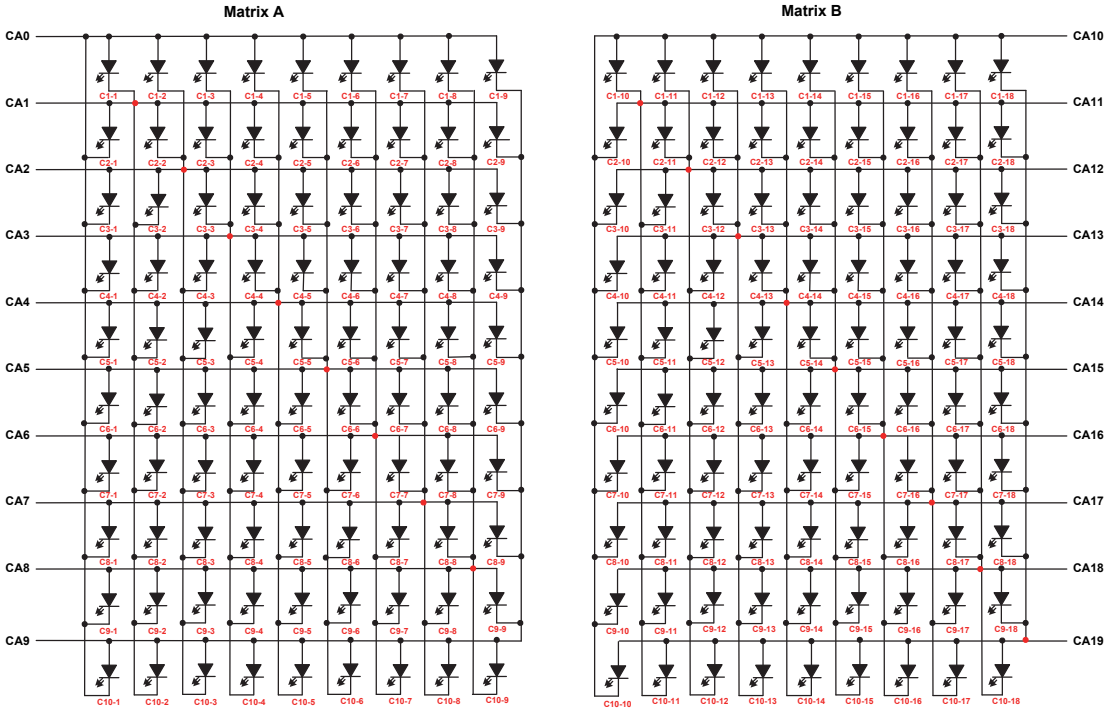
- **Matrix-type1: 9×10 + 9×10**

Data Bit								Address
D7	D6	D5	D4	D3	D2	D1	D0	
C1-8	C1-7	C1-6	C1-5	C1-4	C1-3	C1-2	C1-1	00h
C1-16	C1-15	C1-14	C1-13	C1-12	C1-11	C1-10	C1-9	01h
x	x	x	x	x	x	C1-18	C1-17	02h
C2-8	C2-7	C2-6	C2-5	C2-4	C2-3	C2-2	C2-1	03h
C2-16	C2-15	C2-14	C2-13	C2-12	C2-11	C2-10	C2-9	04h
x	x	x	x	x	x	C2-18	C2-17	05h
C3-8	C3-7	C3-6	C3-5	C3-4	C3-3	C3-2	C3-1	06h
C3-16	C3-15	C3-14	C3-13	C3-12	C3-11	C3-10	C3-9	07h
x	x	x	x	x	x	C3-18	C3-17	08h

Data Bit								Address
D7	D6	D5	D4	D3	D2	D1	D0	
C4-8	C4-7	C4-6	C4-5	C4-4	C4-3	C4-2	C4-1	09h
C4-16	C4-15	C4-14	C4-13	C4-12	C4-11	C4-10	C4-9	0Ah
x	x	x	x	x	x	C4-18	C4-17	0Bh
C5-8	C5-7	C5-6	C5-5	C5-4	C5-3	C5-2	C5-1	0Ch
C5-16	C5-15	C5-14	C5-13	C5-12	C5-11	C5-10	C5-9	0Dh
x	x	x	x	x	x	C5-18	C5-17	0Eh
C6-8	C6-7	C6-6	C6-5	C6-4	C6-3	C6-2	C6-1	0Fh
C6-16	C6-15	C6-14	C6-13	C6-12	C6-11	C6-10	C6-9	10h
x	x	x	x	x	x	C6-18	C6-17	11h
C7-8	C7-7	C7-6	C7-5	C7-4	C7-3	C7-2	C7-1	12h
C7-16	C7-15	C7-14	C7-13	C7-12	C7-11	C7-10	C7-9	13h
x	x	x	x	x	x	C7-18	C7-17	14h
C8-8	C8-7	C8-6	C8-5	C8-4	C8-3	C8-2	C8-1	15h
C8-16	C8-15	C8-14	C8-13	C8-12	C8-11	C8-10	C8-9	16h
x	x	x	x	x	x	C8-18	C8-17	17h
C9-8	C9-7	C9-6	C9-5	C9-4	C9-3	C9-2	C9-1	18h
C9-16	C9-15	C9-14	C9-13	C9-12	C9-11	C9-10	C9-9	19h
x	x	x	x	x	x	C9-18	C9-17	1Ah
C10-8	C10-7	C10-6	C10-5	C10-4	C10-3	C10-2	C10-1	1Bh
C10-16	C10-15	C10-14	C10-13	C10-12	C10-11	C10-10	C10-9	1Ch
x	x	x	x	x	x	C10-18	C10-17	1Dh

Note: The addresses will continuously increment automatically. The address will be wrapped around to address 00H when it exceeds the maximum address value of 1Dh.

The default relationship between RAM mapping and LED address is shown in the following figure.

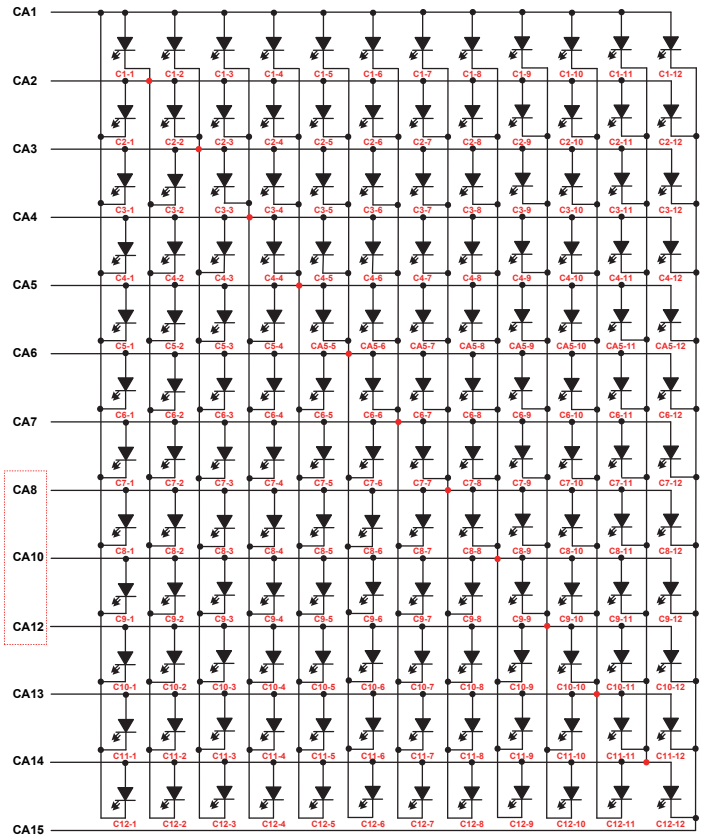


• **Matrix-type2: 12×12**

Data Bit								Address
D7	D6	D5	D4	D3	D2	D1	D0	
C1-8	C1-7	C1-6	C1-5	C1-4	C1-3	C1-2	C1-1	00h
C2-4	C2-3	C2-2	C2-1	C1-12	C1-11	C1-10	C1-9	01h
C2-12	C2-11	C2-10	C2-9	C2-8	C2-7	C2-6	C2-5	02h
C3-8	C3-7	C3-6	C3-5	C3-4	C3-3	C3-2	C3-1	03h
C4-4	C4-3	C4-2	C4-1	C3-12	C3-11	C3-10	C3-9	04h
C4-12	C4-11	C4-10	C4-9	C4-8	C4-7	C4-6	C4-5	05h
C5-8	C5-7	C5-6	C5-5	C5-4	C5-3	C5-2	C5-1	06h
C6-4	C6-3	C6-2	C6-1	C5-12	C5-11	C5-10	C5-9	07h
C6-12	C6-11	C6-10	C6-9	C6-8	C6-7	C6-6	C6-5	08h
C7-8	C7-7	C7-6	C7-5	C7-4	C7-3	C7-2	C7-1	09h
C8-4	C8-3	C8-2	C8-1	C7-12	C7-11	C7-10	C7-9	0Ah
C8-12	C8-11	C8-10	C8-9	C8-8	C8-7	C8-6	C8-5	0Bh
C9-8	C9-7	C9-6	C9-5	C9-4	C9-3	C9-2	C9-1	0Ch
C10-4	C10-3	C10-2	C10-1	C9-12	C9-11	C9-10	C9-9	0Dh
C10-12	C10-11	C10-10	C10-9	C10-8	C10-7	C10-6	C10-5	0Eh
C11-8	C11-7	C11-6	C11-5	C11-4	C11-3	C11-2	C11-1	0Fh
C12-4	C12-3	C12-2	C12-1	C11-12	C11-11	C11-10	C11-9	10h
C12-12	C12-11	C12-10	C12-9	C12-8	C12-7	C12-6	C12-5	11h

Note: The addresses will continuously increment automatically. The address will be wrapped around to address 00H when it exceeds the maximum address value of 11h.

The default relationship between RAM mapping and LED address is shown in the following figure.

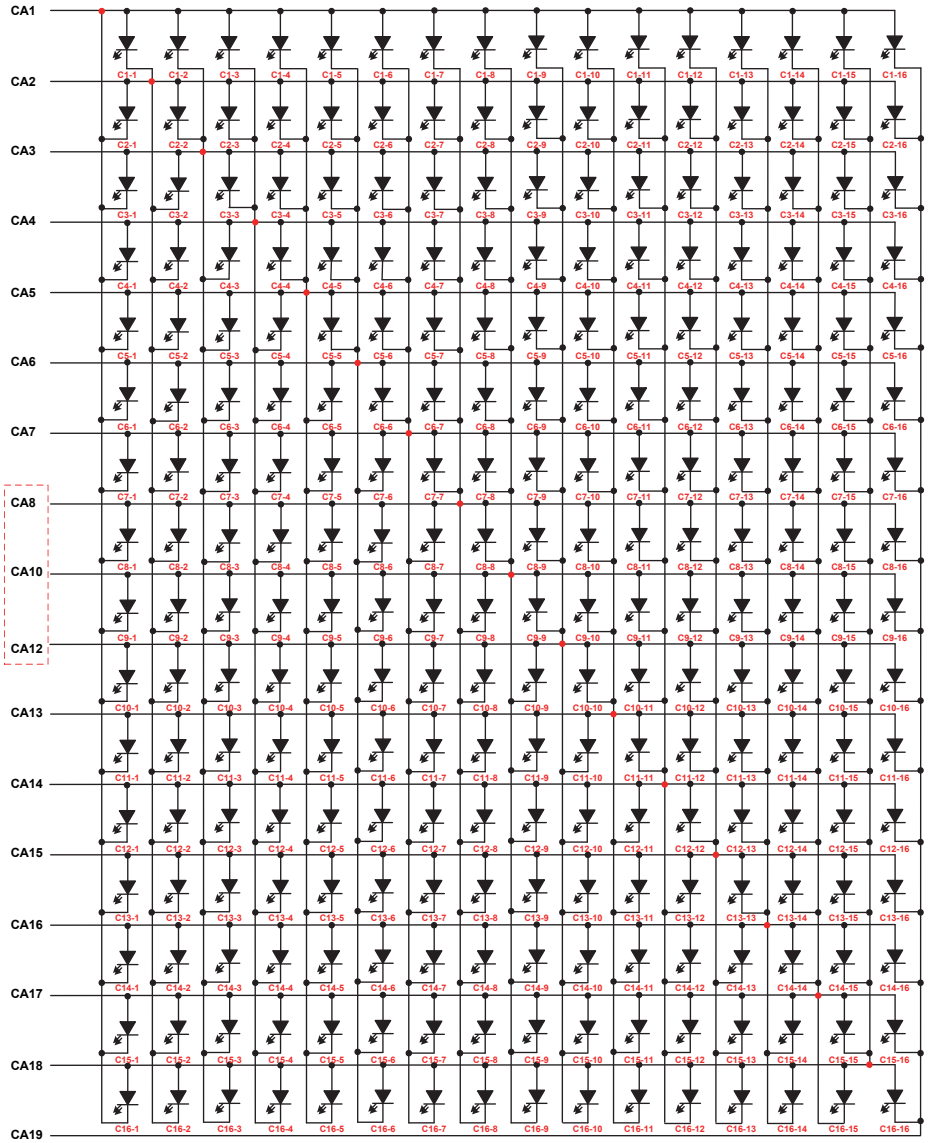


• **Matrix-type3: 16×16**

Data Bit								Address
D7	D6	D5	D4	D3	D2	D1	D0	
C1-8	C1-7	C1-6	C1-5	C1-4	C1-3	C1-2	C1-1	00h
C1-16	C1-15	C1-14	C1-13	C1-12	C1-11	C1-10	C1-9	01h
C2-8	C2-7	C2-6	C2-5	C2-4	C2-3	C2-2	C2-1	02h
C2-16	C2-15	C2-14	C2-13	C2-12	C2-11	C2-10	C2-9	03h
C3-8	C3-7	C3-6	C3-5	C3-4	C3-3	C3-2	C3-1	04h
C3-16	C3-15	C3-14	C3-13	C3-12	C3-11	C3-10	C3-9	05h
C4-8	C4-7	C4-6	C4-5	C4-4	C4-3	C4-2	C4-1	06h
C4-16	C4-15	C4-14	C4-13	C4-12	C4-11	C4-10	C4-9	07h
C5-8	C5-7	C5-6	C5-5	C5-4	C5-3	C5-2	C5-1	08h
C5-16	C5-15	C5-14	C5-13	C5-12	C5-11	C5-10	C5-9	09h
C6-8	C6-7	C6-6	C6-5	C6-4	C6-3	C6-2	C6-1	0Ah
C6-16	C6-15	C6-14	C6-13	C6-12	C6-11	C6-10	C6-9	0Bh
C7-8	C7-7	C7-6	C7-5	C7-4	C7-3	C7-2	C7-1	0Ch
C7-16	C7-15	C7-14	C7-13	C7-12	C7-11	C7-10	C7-9	0Dh
C8-8	C8-7	C8-6	C8-5	C8-4	C8-3	C8-2	C8-1	0Eh
C8-16	C8-15	C8-14	C8-13	C8-12	C8-11	C8-10	C8-9	0Fh
C9-8	C9-7	C9-6	C9-5	C9-4	C9-3	C9-2	C9-1	10h
C9-16	C9-15	C9-14	C9-13	C9-12	C9-11	C9-10	C9-9	11h
C10-8	C10-7	C10-6	C10-5	C10-4	C10-3	C10-2	C10-1	12h
C10-16	C10-15	C10-14	C10-13	C10-12	C10-11	C10-10	C10-9	13h
C11-8	C11-7	C11-6	C11-5	C11-4	C11-3	C11-2	C11-1	14h
C11-16	C11-15	C11-14	C11-13	C11-12	C11-11	C11-10	C11-9	15h
C12-8	C12-7	C12-6	C12-5	C12-4	C12-3	C12-2	C12-1	16h
C12-16	C12-15	C12-14	C12-13	C12-12	C12-11	C12-10	C12-9	17h
C13-8	C13-7	C13-6	C13-5	C13-4	C13-3	C13-2	C13-1	18h
C13-16	C13-15	C13-14	C13-13	C13-12	C13-11	C13-10	C13-9	19h
C14-8	C14-7	C14-6	C14-5	C14-4	C14-3	C14-2	C14-1	1Ah
C14-16	C14-15	C14-14	C14-13	C14-12	C14-11	C14-10	C14-9	1Bh
C15-8	C15-7	C15-6	C15-5	C15-4	C15-3	C15-2	C15-1	1Ch
C15-16	C15-15	C15-14	C15-13	C15-12	C15-11	C15-10	C15-9	1Dh
C16-8	C16-7	C16-6	C16-5	C16-4	C16-3	C16-2	C16-1	1Eh
C16-16	C16-15	C16-14	C16-13	C16-12	C16-11	C16-10	C16-9	1Fh

Note: The addresses will continuously increment automatically. The address will be wrapped around to address 00H when it exceeds the maximum address value of 1Fh.

The default relationship between RAM mapping and LED address is shown in the following figure.



In the Gray mode, the display RAM is a static 256×8-bit RAM in which the LED data is stored. A logic "1" in the RAM bit-map indicates an "on" state of the corresponding LED ROW. Similarly a logic "0" indicates an "off" state. There is a one-to-one correspondence between the display memory addresses and the CA pin outputs, and between the individual bits of a RAM word and the column outputs.

The following is a mapping from the RAM to the LED pattern:

- **Matrix-type1: 9×10 + 9×10**

Data Byte												Address
D7~D0	D7~D0	----	D7~D0	D7~D0	D7~D0	D7~D0	D7~D0	D7~D0	D7~D0	D7~D0	D7~D0	
0Fh (C1-16)	0Eh (C1-15)	----	08h (C1-9)	07h (C1-8)	06h (C1-7)	05h (C1-6)	04h (C1-5)	03h (C1-4)	02h (C1-3)	01h (C1-2)	00h (C1-1)	00h~0Fh
1Fh (C2-14)	1Eh (C2-13)	----	18h (C2-7)	17h (C2-6)	16h (C2-5)	15h (C2-4)	14h (C2-3)	13h (C2-2)	12h (C2-1)	11h (C1-18)	10h (C1-17)	10h~1Fh
2Fh (C3-12)	2Eh (C3-11)	----	28h (C3-5)	27h (C3-4)	26h (C3-3)	25h (C3-2)	24h (C3-1)	23h (C2-18)	22h (C2-17)	21h (C2-16)	20h (C2-15)	20h~2Fh
3Fh (C4-10)	3Eh (C4-9)	----	38h (C4-3)	37h (C4-2)	36h (C4-1)	35h (C3-18)	34h (C1-17)	33h (C3-16)	32h (C3-15)	31h (C3-14)	30h (C3-13)	30h~3Fh
4Fh (C5-8)	4Eh (C5-7)	----	48h (C5-1)	47h (C4-18)	46h (C4-17)	45h (C4-16)	44h (C4-15)	43h (C4-14)	42h (C4-13)	41h (C4-12)	40h (C4-11)	40h~4Fh
5Fh (C6-6)	5Eh (C6-5)	----	58h (C5-17)	57h (C5-16)	56h (C5-15)	57h (C5-16)	56h (C5-15)	53h (C5-12)	52h (C5-11)	51h (C5-10)	50h (C5-9)	50h~5Fh
6Fh (C7-4)	6Eh (C7-3)	----	68h (C6-15)	67h (C6-14)	66h (C6-13)	65h (C6-12)	64h (C6-11)	63h (C6-10)	62h (C6-9)	61h (C6-8)	60h (C6-7)	60h~6Fh
7Fh (C8-2)	7Eh (C8-1)	----	78h (C7-13)	77h (C7-12)	76h (C7-11)	75h (C7-10)	74h (C7-9)	73h (C7-8)	72h (C7-7)	71h (C7-6)	70h (C7-5)	70h~7Fh
8Fh (C818)	8Eh (C8-17)	----	88h (C8-11)	87h (C8-10)	86h (C8-9)	85h (C8-8)	84h (C8-7)	83h (C8-6)	82h (C8-5)	81h (C8-4)	80h (C8-3)	80h~8Fh
9Fh (C9-16)	9Eh (C9-15)	----	98h (C9-9)	97h (C9-8)	96h (C9-7)	95h (C9-6	94h (C9-5)	93h (C9-4)	92h (C9-3)	91h (C9-2)	90h (C9-1)	90h~9Fh
AFh (C10-14)	AEh (C10-13)	----	A8h (C10-7)	A7h (C10-6)	A6h (C10-5)	A5h (C10-4)	A4h (C10-3)	A3h (C10-2)	A2h (C10-1)	A1h (C9-18)	A0h (C9-17)	A0h~AFh
								B3h (C10-18)	B2h (C10-17)	B1h (C10-16)	B0h (C10-15)	B0h~B3h

Note: The addresses will continuously increment automatically. The address will be wrapped around to address 00H when it exceeds the maximum address value of B3h.

• **Matrix-type2: 12×12**

Data Byte									Address
D7~ D0	D7~ D0	D7~ D0	D7~ D0	-----	D7~ D0	D7~ D0	D7~ D0	D7~ D0	
0Bh (C1-12)	0Ah (C1-11)	09h (C1-10)	08h (C1-9)	-----	03h (C1-4)	02h (C1-3)	01h (C1-2)	00h (C1-1)	00h~0Bh
1Bh (C2-12)	1Ah (C2-11)	19h (C2-10)	18h (C2-9)	-----	13h (C2-4)	12h (C2-3)	11h (C2-2)	10h (C2-1)	10h~1Bh
2Bh (C3-12)	2Ah (C3-11)	29h (C3-10)	28h (C3-9)	-----	23h (C3-4)	22h (C3-3)	21h (C3-2)	20h (C3-1)	20h~2Bh
3Bh (C4-12)	3Ah (C4-11)	39h (C4-10)	38h (C4-9)	-----	33h (C4-4)	32h (C4-3)	31h (C4-2)	30h (C4-1)	30h~3Bh
4Bh (C5-12)	4Ah (C5-11)	49h (C5-10)	48h (C5-9)	-----	43h (C5-4)	42h (C5-3)	41h (C5-2)	40h (C5-1)	40h~4Bh
5Bh (C6-12)	5Ah (C6-11)	59h (C6-10)	58h (C6-9)	-----	53h (C6-4)	52h (C6-3)	51h (C6-2)	50h (C6-1)	50h~5Bh
6Bh (C7-12)	6Ah (C7-11)	69h (C7-10)	68h (C7-9)	-----	63h (C7-4)	62h (C7-3)	61h (C7-2)	60h (C7-1)	60h~6Bh
7Bh (C8-12)	7Ah (C8-11)	79h (C8-10)	78h (C8-9)	-----	73h (C8-4)	72h (C8-3)	71h (C8-2)	70h (C8-1)	70h~7Bh
8Bh (C9-12)	8Ah (C9-11)	89h (C9-10)	88h (C9-9)	-----	83h (C9-4)	82h (C9-3)	81h (C9-2)	80h (C9-1)	80h~8Bh
9Bh (C10-12)	9Ah (C10-11)	99h (C10-10)	98h (C10-9)	-----	93h (C10-4)	92h (C10-3)	91h (C10-2)	90h (C10-1)	90h~98h
ABh (C11-12)	AAh (C11-11)	A9h (C11-10)	A8h (C11-9)	-----	A3h (C11-4)	A2h (C11-3)	A1h (C11-2)	A0h (C11-1)	A0h~ABh
BBh (C12-12)	BAh (C12-11)	B9h (C12-10)	B8h (C12-9)	-----	B3h (C12-4)	B2h (C12-3)	B1h (C12-2)	B0h (C12-1)	B0h~BBh

Note: The addresses will continuously increment automatically. The address will be wrapped around to address 00H when it exceeds the maximum address value of BBh.

• **Matrix-type3: 16×16**

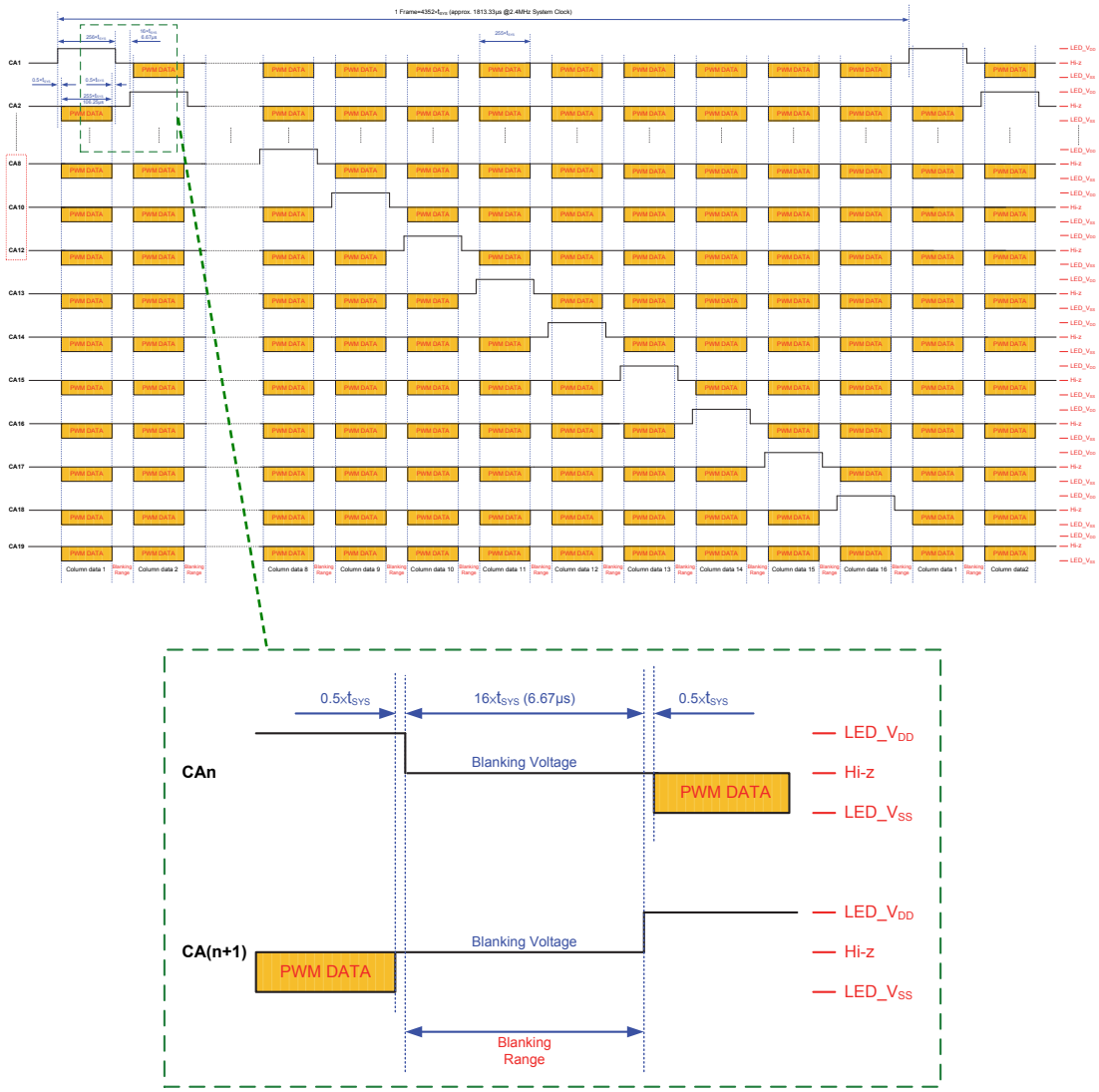
Data Byte									Address A[7:0]
D7~ D0	D7~ D0	D7~ D0	D7~ D0	-----	D7~ D0	D7~ D0	D7~ D0	D7~ D0	
0Fh (C1-16)	0Eh (C1-15)	0Dh (C1-14)	0Ch (C1-13)	-----	03h (C1-4)	02h (C1-3)	01h (C1-2)	00h (C1-1)	00h~0Fh
1Fh (C2-16)	1Eh (C2-15)	1Dh (C2-14)	1Ch (C2-13)	-----	13h (C2-4)	12h (C2-3)	11h (C2-2)	10h (C2-1)	10h~1Fh
2Fh (C3-16)	2Eh (C3-15)	2Dh (C3-14)	2Ch (C3-13)	-----	23h (C3-4)	22h (C3-3)	21h (C3-2)	20h (C3-1)	20h~2Fh
3Fh (C4-16)	3Eh (C4-15)	3Dh (C4-14)	3Ch (C4-13)	-----	33h (C4-4)	32h (C4-3)	31h (C4-2)	30h (C4-1)	30h~3Fh
4Fh (C5-16)	4Eh (C5-15)	4Dh (C5-14)	4Ch (C5-13)	-----	43h (C5-4)	42h (C5-3)	41h (C5-2)	40h (C5-1)	40h~4Fh
5Fh (C6-16)	5Eh (C6-15)	5Dh (C6-14)	5Ch (C6-13)	-----	53h (C6-4)	52h (C6-3)	51h (C6-2)	50h (C6-1)	50h~5Fh
6Fh (C7-16)	6Eh (C7-15)	6Dh (C7-14)	6Ch (C7-13)	-----	63h (C7-4)	62h (C7-3)	61h (C7-2)	60h (C7-1)	60h~6Fh
7Fh (C8-16)	7Eh (C8-15)	7Dh (C8-14)	7Ch (C8-13)	-----	73h (C8-4)	72h (C8-3)	71h (C8-2)	70h (C8-1)	70h~7Fh
8Fh (C9-16)	8Eh (C9-15)	8Dh (C9-14)	8Ch (C9-13)	-----	83h (C9-4)	82h (C9-3)	81h (C9-2)	80h (C9-1)	80h~8Fh
9Fh (C10-16)	9Eh (C10-15)	9Dh (C10-14)	9Ch (C10-13)	-----	93h (C10-4)	92h (C10-3)	91h (C10-2)	90h (C10-1)	90h~9Fh
AFh (C11-16)	AEh (C11-15)	ADh (C11-14)	ACh (C11-13)	-----	A3h (C11-4)	A2h (C11-3)	A1h (C11-2)	A0h (C11-1)	A0h~AFh
BFh (C12-16)	BEh (C12-15)	BDh (C12-14)	BCh (C12-13)	-----	B3h (C12-4)	B2h (C12-3)	B1h (C12-2)	B0h (C12-1)	B0h~BFh
CFh (C13-16)	CEh (C13-15)	CDh (C13-14)	CCh (C13-13)	-----	C3h (C13-4)	C2h (C13-3)	C1h (C13-2)	C0h (C13-1)	C0h~CFh
DFh (C14-16)	DEh (C14-15)	DDh (C14-14)	DCh (C14-13)	-----	D3h (C14-4)	D2h (C14-3)	D1h (C14-2)	D0h (C14-1)	D0h~DFh
EFh (C15-16)	EEh (C15-15)	EDh (C15-14)	ECh (C15-13)	-----	E3h (C15-4)	E2h (C15-3)	E1h (C15-2)	E0h (C15-1)	E0h~EFh
FFh (C16-16)	FEh (C16-15)	FDh (C16-14)	FCh (C16-13)	-----	F3h (C16-4)	F2h (C16-3)	F1h (C16-2)	F0h (C16-1)	F0h~FFh

Note: The addresses will continuously increment automatically. The address will be wrapped around to address 00H when it exceeds the maximum address value of FFh.

LED Driver Output Waveform

The device includes a 256 (16×16) pattern LED driver. This can be setup in a 16×16 format for the COM outputs. This feature allows the device to be used in multiple LED applications. The LED driver mode waveforms and scanning format is as follows:

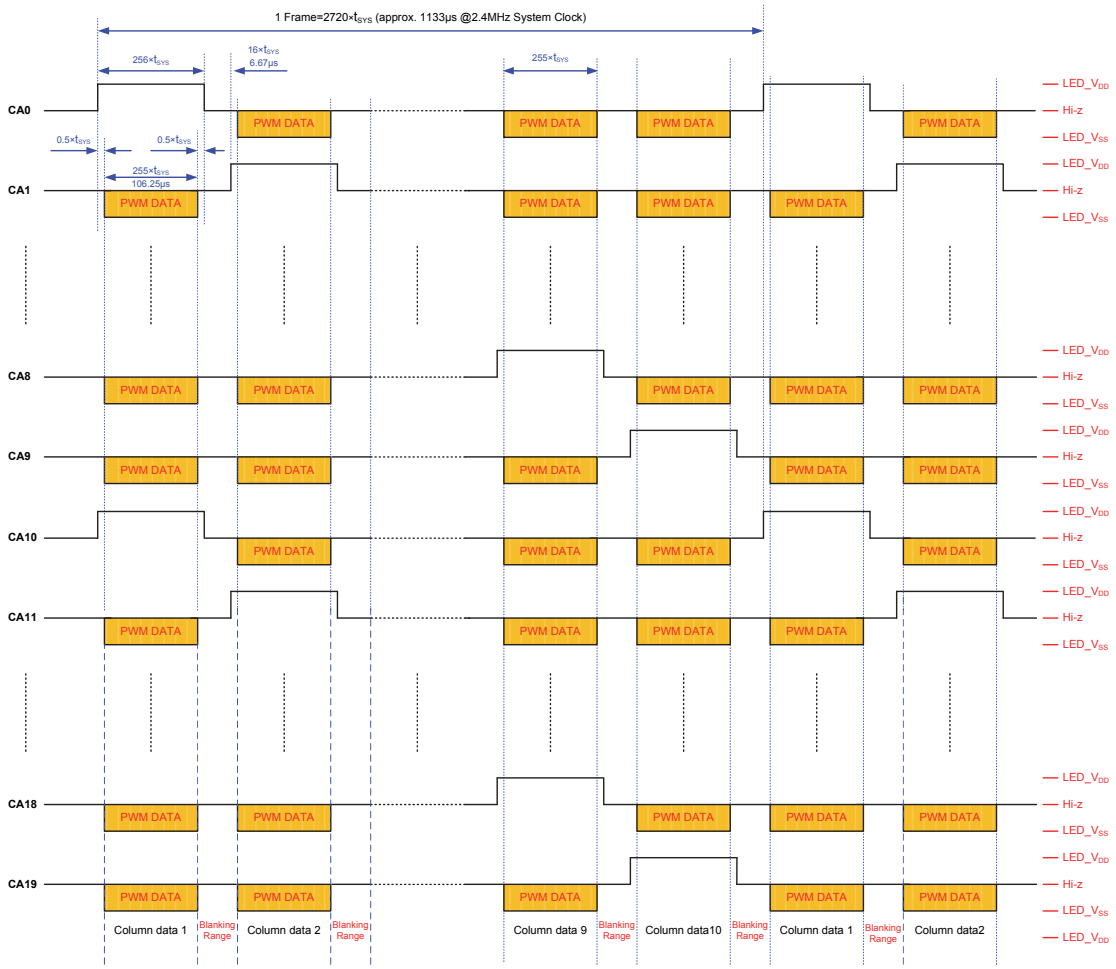
• 16×16 Driver Mode and Disable Discharge Function



Note: $t_{SYS} = 1/f_{SYS}$ (1/2.4MHz).

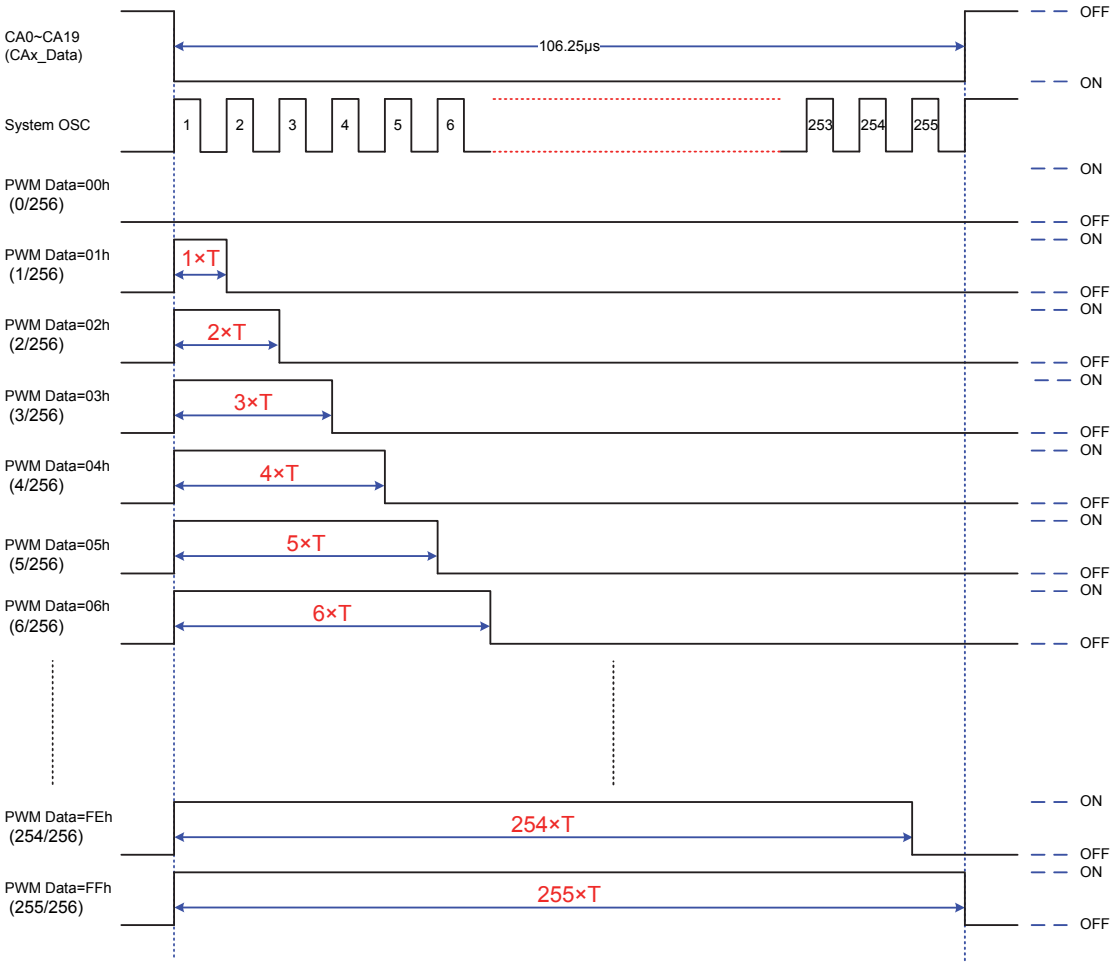
• 12×12 Driver Mode and Disable Discharge Function

• 9×10 + 9×10 Driver Mode and Disable Discharge Function



PWM Data Width Timing

The PWM Data width timings are shown in the accompanying diagram.



Note: $t_{SYS} = 1/f_{SYS}$ (1/2.4MHz).

Fade Data RAM

The Fade RAM is a static 128×8-bit RAM in which the mode function, delay time function and slope cycle time function data for each dot is stored. There is a one-to-one correspondence between the fade function memory addresses and the CA pin outputs and between the individual bits of a RAM word and the column outputs.

Write Dot Fade Data	W	1	0	0	0	0	0	1	0	82h	Write Fade RAM Data
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	RAM Address
	W	FS2	FT2_1	FT1_1	FT0_1	FS1	FT2_0	FT1_0	FT0_0	—	Set Parameters for Fade Mode FS: Blink or Fade Mode select FT: Blink or Fade cycle time set

FS1/FS2	Select	Remarks
0	Fade Mode	Default
1	Blink Mode	—

The cycle time set is setup as follows.

FT2_0/FT2_1	FT1_0/FT1_1	FT0_0/FT0_1	Fade T1 Time	Remarks
0	0	0	Off	Default
0	0	1	256 frames	1×256
0	1	0	512 frames	2×256
0	1	1	1024 frames	4×256
1	0	0	1536 frames	6×256
1	0	1	2048 frames	8×256
1	1	0	2560 frames	10×256
1	1	1	3072 frames	12×256

Note: 1. In the Binary Mode the Fade data setting for each dot RAM is invalid.
2. The setup time is based on OSC frequency.

Matrix Type	Pixel	1 Frame Time
Type1	(10×9) + (10×9)	[(256+16)×10]/2.4MHz≈1.133ms
Type2	12×12	[(256+16)×12]/2.4MHz≈1.36ms
Type3	16×16	[(256+16)×16]/2.4MHz≈1.813ms

The following shows a mapping from the Fade RAM to the LED pattern.

• Matrix-type1: 9×10 + 9×10

Data Byte											Address
D7~ D4	D3~D0	-----	D7~ D4	D3~D0	D7~ D4	D3~D0	D7~ D4	D3~D0	D7~ D4	D3~D0	
07h (C1-16)	07h (C1-15)	-----	03h (C1-8)	03h (C1-7)	02h (C1-6)	02h (C1-5)	01h (C1-4)	01h (C1-3)	00h (C1-2)	00h (C1-1)	00h~07h
XXXX	XXXX	-----	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	08h (C1-18)	08h (C1-17)	08h~0Fh
17h (C2-16)	17h (C2-15)	-----	13h (C2-8)	13h (C2-7)	12h (C2-6)	12h (C2-5)	11h (C2-4)	11h (C2-3)	10h (C2-2)	10h (C2-1)	10h~17h
XXXX	XXXX	-----	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	18h (C2-18)	18h (C2-17)	18h~1Fh
27h (C3-16)	27h (C3-15)	-----	23h (C3-8)	23h (C3-7)	22h (C3-6)	22h (C3-5)	21h (C3-4)	21h (C3-3)	20h (C3-2)	20h (C3-1)	20h~27h
XXXX	XXXX	-----	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	28h (C3-18)	28h (C3-17)	28h~2Fh
37h (C4-16)	37h (C4-15)	-----	33h (C4-8)	33h (C4-7)	32h (C4-6)	32h (C4-5)	31h (C4-4)	31h (C4-3)	30h (C4-2)	30h (C4-1)	30h~37h
XXXX	XXXX	-----	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	38h (C4-18)	38h (C4-17)	38h~3Fh

Data Byte											Address
D7~ D4	D3~D0	-----	D7~ D4	D3~D0	D7~ D4	D3~D0	D7~ D4	D3~D0	D7~ D4	D3~D0	
47h (C5-16)	47h (C5-15)	-----	43h (C5-8)	43h (C5-7)	42h (C5-6)	42h (C5-5)	41h (C5-4)	41h (C5-3)	40h (C5-2)	40h (C5-1)	40h~47h
XXXX	XXXX	-----	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	48h (C5-18)	48h (C5-17)	48h~4Fh
57h (C6-16)	57h (C6-15)	-----	53h (C6-8)	53h (C6-7)	52h (C6-6)	52h (C6-5)	51h (C6-4)	51h (C6-3)	50h (C6-2)	50h (C6-1)	50h~57h
XXXX	XXXX	-----	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	58h (C6-18)	58h (C6-17)	58h~5Fh
67h (C7-16)	67h (C7-15)	-----	63h (C7-8)	63h (C7-7)	62h (C7-6)	62h (C7-5)	61h (C7-4)	61h (C7-3)	60h (C7-2)	60h (C7-1)	60h~67h
XXXX	XXXX	-----	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	68h (C7-18)	68h (C7-17)	68h~6Fh
77h (C8-16)	77h (C8-15)	-----	73h (C8-8)	73h (C8-7)	72h (C8-6)	72h (C8-5)	71h (C8-4)	71h (C8-3)	70h (C8-2)	70h (C8-1)	70h~77h
XXXX	XXXX	-----	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	78h (C8-18)	78h (C8-17)	78h~7Fh
87h (C9-16)	87h (C9-15)	-----	83h (C9-8)	83h (C9-7)	82h (C9-6)	82h (C9-5)	81h (C9-4)	81h (C9-3)	80h (C9-2)	80h (C9-1)	80h~87h
XXXX	XXXX	-----	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	88h (C9-18)	88h (C9-17)	88h~8Fh
97h (C10-16)	97h (C10-15)	-----	93h (C10-8)	93h (C10-7)	92h (C10-6)	92h (C10-5)	91h (C10-4)	91h (C10-3)	90h (C10-2)	90h (C10-1)	90h~97h
XXXX	XXXX	-----	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	98h (C10-18)	98h (C10-17)	98h~9Fh

Note: Write 90 bytes data into the Fade RAM from the start address 00h. The addresses will continuously increment automatically. The address will be wrapped around to address 00h when it exceeds the maximum address value of 9Fh.

- **Matrix-type2: 12×12**

Data Byte									Address
D7~ D4	D3~D0	D7~ D4	D3~D0	-----	D7~ D4	D3~D0	D7~ D4	D3~D0	
05h (C1-12)	05h (C1-11)	04h (C1-10)	04h (C1-9)	-----	01h (C1-4)	01h (C1-3)	00h (C1-2)	00h (C1-1)	00h~05h
15h (C2-12)	15h (C2-11)	14h (C2-10)	14h (C2-9)	-----	11h (C2-4)	11h (C2-3)	10h (C2-2)	10h (C2-1)	10h~15h
25h (C3-12)	25h (C3-11)	24h (C3-10)	24h (C3-9)	-----	21h (C3-4)	21h (C3-3)	20h (C3-2)	20h (C3-1)	20h~25h
35h (C4-12)	35h (C4-11)	34h (C4-10)	34h (C4-9)	-----	31h (C4-4)	31h (C4-3)	30h (C4-2)	30h (C4-1)	30h~35h
45h (C5-12)	45h (C5-11)	44h (C5-10)	44h (C5-9)	-----	41h (C5-4)	41h (C5-3)	40h (C5-2)	40h (C5-1)	40h~45h
55h (C6-12)	55h (C6-11)	54h (C6-10)	54h (C6-9)	-----	51h (C6-4)	51h (C6-3)	50h (C6-2)	50h (C6-1)	50h~55h
65h (C7-12)	65h (C7-11)	64h (C7-10)	64h (C7-9)	-----	61h (C7-4)	61h (C7-3)	60h (C7-2)	60h (C7-1)	60h~65h
75h (C8-12)	75h (C8-11)	74h (C8-10)	74h (C8-9)	-----	71h (C8-4)	71h (C8-3)	70h (C8-2)	70h (C8-1)	70h~75h
85h (C9-12)	85h (C9-11)	84h (C9-10)	84h (C9-9)	-----	81h (C9-4)	81h (C9-3)	80h (C9-2)	80h (C9-1)	80h~85h
95h (C10-12)	95h (C10-11)	94h (C10-10)	94h (C10-9)	-----	91h (C10-4)	91h (C10-3)	90h (C10-2)	90h (C10-1)	90h~95h
A5h (C11-12)	A5h (C11-11)	A4h (C11-10)	A4h (C11-9)	-----	A1h (C11-4)	A1h (C11-3)	A0h (C11-2)	A0h (C11-1)	A0h~A5h
B5h (C12-12)	B5h (C12-11)	B4h (C12-10)	B4h (C12-9)	-----	B1h (C12-4)	B1h (C12-3)	B0h (C12-2)	B0h (C12-1)	B0h~B5h

Note: Write 72 bytes data into the Fade RAM from the start address 00h. The addresses will continuously increment automatically. The address will be wrapped around to address 00h when it exceeds the

maximum address value of B5h.

- **Matrix-type3: 16×16**

Data Byte									Address
D7~ D4	D3~D0	D7~ D4	D3~D0	-----	D7~ D4	D3~D0	D7~ D4	D3~D0	
07h (C1-16)	07h (C1-15)	06h (C1-14)	06h (C1-13)	-----	01h (C1-4)	01h (C1-3)	00h (C1-2)	00h (C1-1)	00h~07h
0Fh (C2-16)	0Fh (C2-15)	0Eh (C2-14)	0Eh (C2-13)	-----	09h (C2-4)	09h (C2-3)	08h (C2-2)	08h (C2-1)	08h~0Fh
17h (C3-16)	17h (C3-15)	16h (C3-14)	16h (C3-13)	-----	11h (C3-4)	11h (C3-3)	10h (C3-2)	10h (C3-1)	10h~17h
1Fh (C4-16)	1Fh (C4-15)	1Eh (C4-14)	1Eh (C4-13)	-----	19h (C4-4)	19h (C4-3)	18h (C4-2)	18h (C4-1)	18h~1Fh
27h (C5-16)	27h (C5-15)	26h (C5-14)	26h (C5-13)	-----	21h (C5-4)	21h (C5-3)	20h (C5-2)	20h (C5-1)	20h~27h
2Fh (C6-16)	2Fh (C6-15)	2Eh (C6-14)	2Eh (C6-13)	-----	29h (C6-4)	29h (C6-3)	28h (C6-2)	28h (C6-1)	28h~2Fh
37h (C7-16)	37h (C7-15)	36h (C7-14)	36h (C7-13)	-----	31h (C7-4)	31h (C7-3)	30h (C7-2)	30h (C7-1)	30h~37h
3Fh (C8-16)	3Fh (C8-15)	3Eh (C8-14)	3Eh (C8-13)	-----	39h (C8-4)	39h (C8-3)	38h (C8-2)	38h (C8-1)	38h~3Fh
47h (C9-16)	47h (C9-15)	46h (C9-14)	46h (C9-13)	-----	41h (C9-4)	41h (C9-3)	40h (C9-2)	40h (C9-1)	40h~47h
4Fh (C10-16)	4Fh (C10-15)	4Eh (C10-14)	4Eh (C10-13)	-----	49h (C10-4)	49h (C10-3)	48h (C10-2)	48h (C10-1)	48h~4Fh
57h (C11-16)	57h (C11-15)	56h (C11-14)	56h (C11-13)	-----	51h (C11-4)	51h (C11-3)	50h (C11-2)	50h (C11-1)	50h~57h
5Fh (C12-16)	5Fh (C12-15)	5Eh (C12-14)	5Eh (C12-13)	-----	59h (C12-4)	59h (C12-3)	58h (C12-2)	58h (C12-1)	58h~5Fh
67h (C13-16)	67h (C13-15)	66h (C13-14)	66h (C13-13)	-----	61h (C13-4)	61h (C13-3)	60h (C13-2)	60h (C13-1)	60h~67h
6Fh (C14-16)	6Fh (C14-15)	6Eh (C14-14)	6Eh (C14-13)	-----	69h (C14-4)	69h (C14-3)	68h (C14-2)	68h (C14-1)	68h~6Fh
77h (C15-16)	77h (C15-15)	76h (C15-14)	76h (C15-13)	-----	71h (C15-4)	71h (C15-3)	70h (C15-2)	70h (C15-1)	70h~77h
7Fh (C16-16)	7Fh (C16-15)	7Eh (C16-14)	7Eh (C16-13)	-----	79h (C16-4)	79h (C16-3)	78h (C16-2)	78h (C16-1)	78h~7Fh

Note: Write 128 bytes data into the Fade RAM from the start address 00h. The addresses will continuously increment automatically. The address will be wrapped around to address 00h when it exceeds the maximum address value of 7Fh.

FT2	FT1	FT0	Fade T1 Time
0	0	0	OFF
0	0	1	256 frames
0	1	0	512 frames
0	1	1	1024 frames
1	0	0	1536 frames
1	0	1	2048 frames
1	1	0	2560 frames
1	1	1	3072 frames

LED On/Off Control RAM Data

The LED on/off RAM is static 32×8-bits RAM which stores LED masking data. Logic "1" in the RAM bit-map indicates the "LED Control on" state of the corresponding LED ROW; similarly, logic 0 indicates the 'LED Control off' state.

There is a one-to-one correspondence between the LED on/off Control memory addresses and the CA pin outputs, and between the individual bits of a RAM word and the column outputs.

The following is a mapping from the LED on/off Control RAM to the LED pattern:

• Matrix-type1: 9×10 + 9×10

Data Bit								Address
D7	D6	D5	D4	D3	D2	D1	D0	
C1-8	C1-7	C1-6	C1-5	C1-4	C1-3	C1-2	C1-1	00h
C1-16	C1-15	C1-14	C1-13	C1-12	C1-11	C1-10	C1-9	01h
X	X	X	X	X	X	C1-18	C1-17	02h
C2-8	C2-7	C2-6	C2-5	C2-4	C2-3	C2-2	C2-1	03h
C2-16	C2-15	C2-14	C2-13	C2-12	C2-11	C2-10	C2-9	04h
X	X	X	X	X	X	C2-18	C2-17	05h
C3-8	C3-7	C3-6	C3-5	C3-4	C3-3	C3-2	C3-1	06h
C3-16	C3-15	C3-14	C3-13	C3-12	C3-11	C3-10	C3-9	07h
X	X	X	X	X	X	C3-18	C3-17	08h
C4-8	C4-7	C4-6	C4-5	C4-4	C4-3	C4-2	C4-1	09h
C4-16	C4-15	C4-14	C4-13	C4-12	C4-11	C4-10	C4-9	0Ah
X	X	X	X	X	X	C4-18	C4-17	0Bh
C5-8	C5-7	C5-6	C5-5	C5-4	C5-3	C5-2	C5-1	0Ch
C5-16	C5-15	C5-14	C5-13	C5-12	C5-11	C5-10	C5-9	0Dh
X	X	X	X	X	X	C5-18	C5-17	0Eh
C6-8	C6-7	C6-6	C6-5	C6-4	C6-3	C6-2	C6-1	0Fh
C6-16	C6-15	C6-14	C6-13	C6-12	C6-11	C6-10	C6-9	10h
X	X	X	X	X	X	C6-18	C6-17	11h
C7-8	C7-7	C7-6	C7-5	C7-4	C7-3	C7-2	C7-1	12h
C7-16	C7-15	C7-14	C7-13	C7-12	C7-11	C7-10	C7-9	13h
X	X	X	X	X	X	C7-18	C7-17	14h
C8-8	C8-7	C8-6	C8-5	C8-4	C8-3	C8-2	C8-1	15h
C8-16	C8-15	C8-14	C8-13	C8-12	C8-11	C8-10	C8-9	16h
X	X	X	X	X	X	C8-18	C8-17	17h
C9-8	C9-7	C9-6	C9-5	C9-4	C9-3	C9-2	C9-1	18h
C9-16	C9-15	C9-14	C9-13	C9-12	C9-11	C9-10	C9-9	19h
X	X	X	X	X	X	C9-18	C9-17	1Ah
C10-8	C10-7	C10-6	C10-5	C10-4	C10-3	C10-2	C10-1	1Bh
C10-16	C10-15	C10-14	C10-13	C10-12	C10-11	C10-10	C10-9	1Ch
X	X	X	X	X	X	C10-18	C10-17	1Dh

Note: 1. The addresses will continuously increment automatically. The address will be wrapped around to address 00h when it exceeds the maximum address value of 1Dh.
2. In the Binary Mode the LED on/off Control RAM function is invalid.

• **Matrix-type2: 12×12**

Data Bit								Address
D7	D6	D5	D4	D3	D2	D1	D0	
C1-8	C1-7	C1-6	C1-5	C1-4	C1-3	C1-2	C1-1	00h
C2-4	C2-3	C2-2	C2-1	C1-12	C1-11	C1-10	C1-9	01h
C2-12	C2-11	C2-10	C2-9	C2-8	C2-7	C2-6	C2-5	02h
C3-8	C3-7	C3-6	C3-5	C3-4	C3-3	C3-2	C3-1	03h
C4-4	C4-3	C4-2	C4-1	C3-12	C3-11	C3-10	C3-9	04h
C4-12	C4-11	C4-10	C4-9	C4-8	C4-7	C4-6	C4-5	05h
C5-8	C5-7	C5-6	C5-5	C5-4	C5-3	C5-2	C5-1	06h
C6-4	C6-3	C6-2	C6-1	C5-12	C5-11	C5-10	C5-9	07h
C6-12	C6-11	C6-10	C6-9	C6-8	C6-7	C6-6	C6-5	08h
C7-8	C7-7	C7-6	C7-5	C7-4	C7-3	C7-2	C7-1	09h
C8-4	C8-3	C8-2	C8-1	C7-12	C7-11	C7-10	C7-9	0Ah
C8-12	C8-11	C8-10	C8-9	C8-8	C8-7	C8-6	C8-5	0Bh
C9-8	C9-7	C9-6	C9-5	C9-4	C9-3	C9-2	C9-1	0Ch
C10-4	C10-3	C10-2	C10-1	C9-12	C9-11	C9-10	C9-9	0Dh
C10-12	C10-11	C10-10	C10-9	C10-8	C10-7	C10-6	C10-5	0Eh
C11-8	C11-7	C11-6	C11-5	C11-4	C11-3	C11-2	C11-1	0Fh
C12-4	C12-3	C12-2	C12-1	C11-12	C11-11	C11-10	C11-9	10h
C12-12	C12-11	C12-10	C12-9	C12-8	C12-7	C12-6	C12-5	11h

Note: 1. The addresses will continuously increment automatically. The address will be wrapped around to address 00H when it exceeds the maximum address value of 11h.
2. In the Binary Mode, the LED on/off Control RAM function is invalid.

• **Matrix-type3: 16×16**

Data Bit								Address
D7	D6	D5	D4	D3	D2	D1	D0	
C1-8	C1-7	C1-6	C1-5	C1-4	C1-3	C1-2	C1-1	00h
C1-16	C1-15	C1-14	C1-13	C1-12	C1-11	C1-10	C1-9	01h
C2-8	C2-7	C2-6	C2-5	C2-4	C2-3	C2-2	C2-1	02h
C2-16	C2-15	C2-14	C2-13	C2-12	C2-11	C2-10	C2-9	03h
C3-8	C3-7	C3-6	C3-5	C3-4	C3-3	C3-2	C3-1	04h
C3-16	C3-15	C3-14	C3-13	C3-12	C3-11	C3-10	C3-9	05h
C4-8	C4-7	C4-6	C4-5	C4-4	C4-3	C4-2	C4-1	06h
C4-16	C4-15	C4-14	C4-13	C4-12	C4-11	C4-10	C4-9	07h
C5-8	C5-7	C5-6	C5-5	C5-4	C5-3	C5-2	C5-1	08h
C5-16	C5-15	C5-14	C5-13	C5-12	C5-11	C5-10	C5-9	09h
C6-8	C6-7	C6-6	C6-5	C6-4	C6-3	C6-2	C6-1	0Ah
C6-16	C6-15	C6-14	C6-13	C6-12	C6-11	C6-10	C6-9	0Bh
C7-8	C7-7	C7-6	C7-5	C7-4	C7-3	C7-2	C7-1	0Ch
C7-16	C7-15	C7-14	C7-13	C7-12	C7-11	C7-10	C7-9	0Dh
C8-8	C8-7	C8-6	C8-5	C8-4	C8-3	C8-2	C8-1	0Eh
C8-16	C8-15	C8-14	C8-13	C8-12	C8-11	C8-10	C8-9	0Fh
C9-8	C9-7	C9-6	C9-5	C9-4	C9-3	C9-2	C9-1	10h
C9-16	C9-15	C9-14	C9-13	C9-12	C9-11	C9-10	C9-9	11h
C10-8	C10-7	C10-6	C10-5	C10-4	C10-3	C10-2	C10-1	12h
C10-16	C10-15	C10-14	C10-13	C10-12	C10-11	C10-10	C10-9	13h

Data Bit								Address
D7	D6	D5	D4	D3	D2	D1	D0	
C11-8	C11-7	C11-6	C11-5	C11-4	C11-3	C11-2	C11-1	14h
C11-16	C11-15	C11-14	C11-13	C11-12	C11-11	C11-10	C11-9	15h
C12-8	C12-7	C12-6	C12-5	C12-4	C12-3	C12-2	C12-1	16h
C12-16	C12-15	C12-14	C12-13	C12-12	C12-11	C12-10	C12-9	17h
C13-8	C13-7	C13-6	C13-5	C13-4	C13-3	C13-2	C13-1	18h
C13-16	C13-15	C13-14	C13-13	C13-12	C13-11	C13-10	C13-9	19h
C14-8	C14-7	C14-6	C14-5	C14-4	C14-3	C14-2	C14-1	1Ah
C14-16	C14-15	C14-14	C14-13	C14-12	C14-11	C14-10	C14-9	1Bh
C15-8	C15-7	C15-6	C15-5	C15-4	C15-3	C15-2	C15-1	1Ch
C15-16	C15-15	C15-14	C15-13	C15-12	C15-11	C15-10	C15-9	1Dh
C16-8	C16-7	C16-6	C16-5	C16-4	C16-3	C16-2	C16-1	1Eh
C16-16	C16-15	C16-14	C16-13	C16-12	C16-11	C16-10	C16-9	1Fh

Note: 1. The addresses will continuously increment automatically. The address will be wrapped around to address 00H when it exceeds the maximum address value of 1Fh.
2. In the Binary Mode, the LED on/off Control RAM function is invalid.

Command Description

Command Table

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.	Description
RAM Page Address Command											
RAM Page Address Set	W	1	1	1	1	1	1	0	1	FDh	Set RAM response page select
	W	X	X	X	X	A3	A2	A1	A0	00h	Page RAM address
RAM R/W Command											
Write Display Data	W	1	0	0	0	0	0	0	0	80h	Write Display RAM Data
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	RAM Address
	W	D7	D6	D5	D4	D3	D2	D1	D0	—	Display Data
Read Display Data	W	1	0	0	0	0	0	0	1	81h	Read Display RAM
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	RAM Address
	R	0	0	0	0	0	0	0	0	00h	Dummy Byte
	R	D7	D6	D5	D4	D3	D2	D1	D0	—	Display Data
Write Dot Fade Data	W	1	0	0	0	0	0	1	0	82h	Write Fade RAM data
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	RAM Address
	W	FS2	FT2_1	FT1_1	FT0_1	FS1	FT2_0	FT1_0	FT0_0	—	Set Parameters for Fade Mode FS: Blink or Fade mode select FT: Blink or Fade cycle time set (T1)
Read Dot Fade Data	W	1	0	0	0	0	0	1	1	83h	Read Parameters of Fade RAM data
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	RAM Address
	R	0	0	0	0	0	0	0	0	00h	Dummy Byte
	R	FS1	FT2_1	FT1_1	FT0_1	FS0	FT2_0	FT1_0	FT0_0	—	Parameters of Fade Data
Write LED Control Data	W	1	0	0	0	0	1	0	0	84h	Write LED on/off control Data for each dot
	W	0	0	0	A4	A3	A2	A1	A0	00h	RAM Address
	W	D7	D6	D5	D4	D3	D2	D1	D0	—	LED on/off control data
Read LED Control Data	W	1	0	0	0	0	1	0	1	85h	Read LED on/off Status for each dot
	W	0	0	0	A4	A3	A2	A1	A0	00h	RAM Address
	R	0	0	0	0	0	0	0	0	00h	Dummy Byte
	R	D7	D6	D5	D4	D3	D2	D1	D0	—	LED On/Off Control Data

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.	Description
Function Command											
Picture Start Page Address	W	0	0	0	1	0	0	0	0	10h	Set start address for Picture Mode
	W	X	X	X	X	PFS3	PFS2	PFS1	PFS0	00h	
Movie Start Page Address	W	0	0	0	1	0	0	0	1	11h	Set start address for Movie Mode
	W	MEN	X	X	X	MFS3	MFS2	MFS1	MFS0	00h	
Movie Playing Length	W	0	0	0	1	0	0	1	0	12h	Number of pages played in a movie.
	W	X	X	X	X	MFL 3	MFL 2	MFL 1	MFL 0	01h	
Movie Cycles Time	W	0	0	0	1	0	0	1	1	13h	Number of loops played in a movie
	W	X	X	X	X	MCT3	MCT2	MCT1	MCT0	00h	
Movie Page Delay Time	W	0	0	0	1	0	1	0	0	14h	Delay time between two pages in a movie.
	W	X	X	MPD5	MPD4	MPD3	MPD2	MPD1	MPD0	04h	
Last Page	W	0	0	0	1	0	1	0	1	15h	The last page displayed in a movie (depending on the cycle time of loops played in a movie)
	W	X	X	X	X	MLP3	MLP2	MLP1	MLP0	00h	
Picture Scrolling Control	W	0	0	1	0	0	0	0	0	20h	Set scrolling function for Picture Mode SCEN: Scrolling SW on/off RL: Right or Left scrolling direction HSP0~4: Horizontal Speed
	W	SCEN	X	RL	HSP4	HSP3	HSP2	HSP1	HSP0	00h	
Display Mode	W	0	0	1	1	0	0	0	0	30h	Picture Display Mode or Movie Display Mode select
	W	X	X	X	X	X	X	X	MP	00h	
Configuration Mode	W	0	0	1	1	0	0	0	1	31h	Binary mode or gray mode select and embedded Matrix Type select
	W	BGS	X	X	X	X	X	MT1	MT0	01h	
Fade Function Control	W	0	0	1	1	0	0	1	0	32h	FFEN: Fade function enable/disable GMEN: Linear Intensity Mode or Gamma Intensity Mode select GFEN: Global or each dot display mode select FOT: Fade Out time FET: Extinguish time FLT: Light time
	W	FFEN	GMEN	GFEN	FOT	FET1	FET0	FLT1	FLT0	4Ah	
Global Fade Time	W	0	0	1	1	0	0	1	1	33h	Global Blinking/Fade period time set
	W	GFS	X	X	X	X	GFT2	GFT1	GFT0	00h	
Cascade Mode	W	0	0	1	1	0	1	0	0	34h	Master mode or Slave mode select
	W	X	X	X	X	X	X	MS1	MS0	00h	
System Control	W	0	0	1	1	0	1	0	1	35h	System Oscillator on/off and Display on/off control
	W	X	X	X	X	X	X	FON	DON	00h	
Constant Current Ratio	W	0	0	1	1	0	1	1	0	36h	Constant Current Ratio - 16 steps
	W	X	X	X	X	CC3	CC2	CC1	CC0	0Ah	
Global Brightness	W	0	0	1	1	0	1	1	1	37h	Luminance Control - 256 steps
	W	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	FFh	
Mode Control	W	0	0	1	1	1	0	0	0	38h	TSDEN: Thermal protect circuit on/off TSDS: Select auto control or user control display on/off function when the over temperature protection is enabled ODEN: OPEN Detection Test on/off SDEN: SHORT Detection Test on/off
	W	TSDEN	TSDS	X	X	X	X	OD EN	SD EN	00h	
Blanking Voltage Set	W	0	0	1	1	1	0	0	1	39h	Blanking Voltage Control – 16 steps
	W	VBEN	X	X	X	VB3	VB2	VB1	VB0	0Fh	
Soft Reset	W	1	1	0	0	1	1	0	0	CCh	Soft Reset Function
Read Register Status	W	0	1	1	1	0	0	0	0	70h	Read Internal Command Information
	R	D7	D6	D5	D4	D3	D2	D1	D0	—	Internal Command Information
Read Movie Frame Status	W	0	1	1	1	0	0	0	1	71h	Read Movie frame and status information
	R	MOF1	MOF0	X	X	MDF3	MDF2	MDF1	MDF0	00h	MDF: Actual displayed frame MOF: Play movie is finished
Read Movie Loop Status	W	0	1	1	1	0	0	1	0	72h	Read Movie loop operation and status information
	R	MOL1	MOL0	X	X	MLP3	MLP2	MLP1	MLP0	00h	MLP: Actual displayed loop times MOL: Play loop is finished

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.	Description
Read Function Flag	W	0	1	1	1	0	0	1	1	73h	Read Function parameters flag data
	R	CAF	X	X	X	X	X	X	TSDF	00h	TSDF: Over temperature limit is reached CAF: Indicate the 1st CA Scan waveform
Read Open Detection Data	W	0	1	1	1	0	1	0	0	74h	Read LED Matrix Open status address
	R	0	0	0	0	0	0	0	0	00h	Dummy byte
	R	D7	D6	D5	D4	D3	D2	D1	D0	00h	Detection data information
Read Short Detection Data	W	0	1	1	1	0	1	0	1	75h	Read LED Matrix Short status address
	R	0	0	0	0	0	0	0	0	00h	Dummy byte
	R	D7	D6	D5	D4	D3	D2	D1	D0	00h	Detection data information

Note: 1. X: Don't care
2. Def.: Power on reset default
3. It is not recommended to change between Master and Slave mode after a system enable
4. If programmed command data is not defined the function will not be affected

Software Reset

This command is set to initialise all functions

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Soft Reset	W	1	1	0	0	1	1	0	0	CCh

The internal circuit status after initialisation is as follows.

- All registers are set to their default value but the contents of the DDRAM are not affected
- System Oscillator is off
- All CA outputs are high impedance
- The LED display is in an off state

RAM Page Address Set

This command is to set the memory page address.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
RAM Page Address Set	W	1	1	1	1	1	1	0	1	FDh
	W	X	X	X	X	A3	A2	A1	A0	00h

A3	A2	A1	A0	RAM Page Address						Remarks
				Gray Mode			Binary Mode			
				Matrix Type1	Matrix Type2	Matrix Type3	Matrix Type1	Matrix Type2	Matrix Type3	
0	0	0	0	Page1	Page1	Page1	Page1	Page1	Page1	(Default)
0	0	0	1	Page2	Page2	Page2	Page2	Page2	Page2	—
0	0	1	0	—	—	—	Page3	Page3	Page3	—
0	0	1	1	—	—	—	Page4	Page4	Page4	—
0	1	0	0	—	—	—	Page5	Page5	Page5	—
0	1	0	1	—	—	—	Page6	Page6	Page6	—
0	1	1	0	—	—	—	Page7	Page7	Page7	—
0	1	1	1	—	—	—	Page8	Page8	Page8	—
1	0	0	0	—	—	—	Page9	Page9	Page9	—
1	0	0	1	—	—	—	Page10	Page10	Page10	—
1	0	1	0	—	—	—	Page11	Page11	Page11	—
1	0	1	1	—	—	—	Page12	Page12	Page12	—
1	1	0	0	—	—	—	—	Page13	Page13	—
1	1	0	1	—	—	—	—	Page14	Page14	—

A3	A2	A1	A0	RAM Page Address						Remarks
				Gray Mode			Binary Mode			
				Matrix Type1	Matrix Type2	Matrix Type3	Matrix Type1	Matrix Type2	Matrix Type3	
1	1	1	0	—	—	—	—	Page15	Page15	—
1	1	1	1	—	—	—	—	Page16	Page16	—

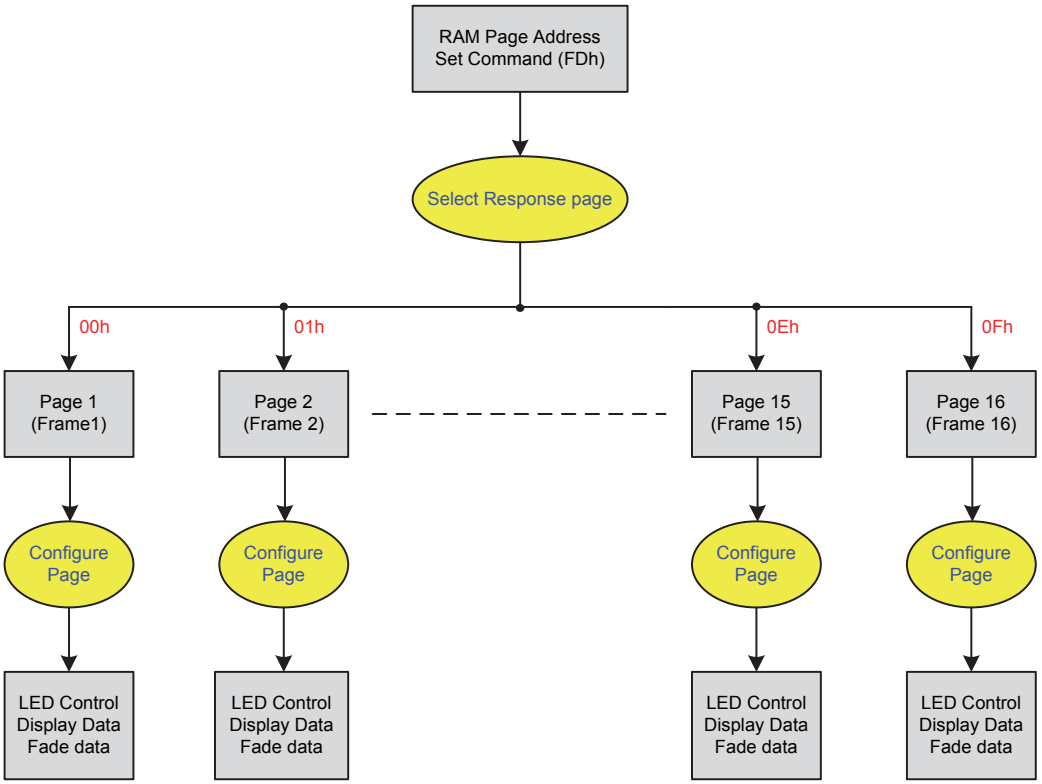
Note: 1. If programmed command data is not defined, the function will not be affected.

2. The three matrix types are shown below.

Matrix Type	Pixel
Type1	9×10 + 9×10
Type2	12×12
Type3	16×16

RAM Page Configure

User has to first configure the RAM Page Address Set Command (FDh), then follows is the data 00h~0Fh to select the Page No., and then users can configure the display data value and function in that Page No.



Picture Display Address

This command is to set the start display page in Picture Mode.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Picture Start Page Address	W	0	0	0	1	0	0	0	0	10h
	W	X	X	X	X	PFS3	PFS2	PFS1	PFS0	00h

PFS3	PFS2	PFS1	PFS0	RAM Page Address						Remarks
				Gray Mode			Binary Mode			
				Matrix Type1	Matrix Type2	Matrix Type3	Matrix Type1	Matrix Type2	Matrix Type3	
0	0	0	0	Page1	Page1	Page1	Page1	Page1	Page1	(Default)
0	0	0	1	Page2	Page2	Page2	Page2	Page2	Page2	—
0	0	1	0	—	—	—	Page3	Page3	Page3	—
0	0	1	1	—	—	—	Page4	Page4	Page4	—
0	1	0	0	—	—	—	Page5	Page5	Page5	—
0	1	0	1	—	—	—	Page6	Page6	Page6	—
0	1	1	0	—	—	—	Page7	Page7	Page7	—
0	1	1	1	—	—	—	Page8	Page8	Page8	—
1	0	0	0	—	—	—	Page9	Page9	Page9	—
1	0	0	1	—	—	—	Page10	Page10	Page10	—
1	0	1	0	—	—	—	Page11	Page11	Page11	—
1	0	1	1	—	—	—	Page12	Page12	Page12	—
1	1	0	0	—	—	—	—	Page13	Page13	—
1	1	0	1	—	—	—	—	Page14	Page14	—
1	1	1	0	—	—	—	—	Page15	Page15	—
1	1	1	1	—	—	—	—	Page16	Page16	—

Note: 1. If programmed command data is not defined, the function will not be affected.

2. The three matrix types are shown below.

Matrix Type	Pixel
Type1	9×10 + 9×10
Type2	12×12
Type3	16×16

Movie Display Start Address

This command is to set the start display page in Movie Mode.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Movie Start Page Address	W	0	0	0	1	0	0	0	1	11h
	W	MEN	X	X	X	MFS3	MFS2	MFS1	MFS0	00h

MEN	SW	Remarks
0	Movie disable	Default
1	Movie enable	—

MFS3	MFS2	MFS1	MFS0	RAM Page Address						Remarks
				Gray Mode			Binary Mode			
				Matrix Type1	Matrix Type2	Matrix Type3	Matrix Type1	Matrix Type2	Matrix Type3	
0	0	0	0	Page1	Page1	Page1	Page1	Page1	Page1	(Default)
0	0	0	1	Page2	Page2	Page2	Page2	Page2	Page2	—
0	0	1	0	—	—	—	Page3	Page3	Page3	—
0	0	1	1	—	—	—	Page4	Page4	Page4	—
0	1	0	0	—	—	—	Page5	Page5	Page5	—
0	1	0	1	—	—	—	Page6	Page6	Page6	—
0	1	1	0	—	—	—	Page7	Page7	Page7	—
0	1	1	1	—	—	—	Page8	Page8	Page8	—
1	0	0	0	—	—	—	Page9	Page9	Page9	—
1	0	0	1	—	—	—	Page10	Page10	Page10	—
1	0	1	0	—	—	—	Page11	Page11	Page11	—
1	0	1	1	—	—	—	Page12	Page12	Page12	—
1	1	0	0	—	—	—	—	Page13	Page13	—
1	1	0	1	—	—	—	—	Page14	Page14	—
1	1	1	0	—	—	—	—	Page15	Page15	—
1	1	1	1	—	—	—	—	Page16	Page16	—

Note: 1. If programmed command data is not defined the function will not be affected.

2. The three matrix types are shown below.

Matrix Type	Pixel
Type1	9×10 + 9×10
Type2	12×12
Type3	16×16

Movie Playing Length

This command is to set the playing page length in movie mode.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Movie Playing Length	W	0	0	0	1	0	0	1	0	12h
	W	X	X	X	X	MFL3	MFL2	MFL1	MFL0	01h

MFL3	MFL2	MFL1	MFL0	RAM Page Address						Remarks
				Gray Mode			Binary Mode			
				Matrix Type1	Matrix Type2	Matrix Type3	Matrix Type1	Matrix Type2	Matrix Type3	
0	0	0	0	1 Page	1 Page	1 Page	1 Page	1 Page	1 Page	—
0	0	0	1	2 Page	2 Page	2 Page	2 Page	2 Page	2 Page	(Default)
0	0	1	0	—	—	—	3 Page	3 Page	3 Page	—
0	0	1	1	—	—	—	4 Page	4 Page	4 Page	—
0	1	0	0	—	—	—	5 Page	5 Page	5 Page	—
0	1	0	1	—	—	—	6 Page	6 Page	6 Page	—
0	1	1	0	—	—	—	7 Page	7 Page	7 Page	—
0	1	1	1	—	—	—	8 Page	8 Page	8 Page	—
1	0	0	0	—	—	—	9 Page	9 Page	9 Page	—
1	0	0	1	—	—	—	10 Page	10 Page	10 Page	—
1	0	1	0	—	—	—	11 Page	11 Page	11 Page	—
1	0	1	1	—	—	—	12 Page	12 Page	12 Page	—
1	1	0	0	—	—	—	—	13 Page	13 Page	—
1	1	0	1	—	—	—	—	14 Page	14 Page	—
1	1	1	0	—	—	—	—	15 Page	15 Page	—
1	1	1	1	—	—	—	—	16 Page	16 Page	—

Note: 1. If programmed command data is not defined, the function will not be affected.

2. The three matrix types are shown below.

Matrix Type	Pixel
Type1	9×10 + 9×10
Type2	12×12
Type3	16×16

Movie Cycle Time

This command is to set the number of loops played in one movie.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Movie Cycle Time	W	0	0	0	1	0	0	1	1	13h
	W	X	X	X	X	MCT3	MCT2	MCT1	MCT0	00h

MCT3	MCT2	MCT1	MCT0	Loops Playing Selection	Remarks
0	0	0	0	1 loop	Default
0	0	0	1	2 loops	—
0	0	1	0	3 loops	—
0	0	1	1	4 loops	—
0	1	0	0	5 loops	—
0	1	0	1	6 loops	—
0	1	1	0	7 loops	—
0	1	1	1	8 loops	—
1	X	X	X	Play movie endless	Needs to be set to 0~7 to stop the movie

Note: 1. If programmed command data is not defined, the function will not be affected.
2. To stop a movie in play movie endless mode, the movie cycles time command have to set to a value between 0000b to 0111b.

Movie Page Delay Time

This command is to set the delay time between two pages in a movie.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Movie Page Delay Time	W	0	0	0	1	0	1	0	0	14h
	W	X	X	MPD5	MPD4	MPD3	MPD2	MPD1	MPD0	04h

Movie page delay time = (MPD [5:0]+1)×8×1frame time

Movie page delay time = (1~64)×8×1frame time = (8~512)×1frame time

For example, when Matrix type1 is selected and MPD [5:0] = 4,

Movie page delay time = 5×8×1.133(ms) = 45.32ms

Matrix Types	Pixel	MPD [5:0]	1 Frame Time	Movie Page Delay Time
Type1	9×10 + 9×10	4	1.133ms	45.32ms
Type2	12×12	4	1.36ms	54.4ms
Type3	16×16	4	1.813ms	72.52ms

Note: 1. If programmed command data is not defined, the function will not be affected.
2. The setup time is based on OSC frequency.

Matrix Types	Pixel	1 Frame Time
Type1	9×10 + 9×10	((256+16)×10)/2.4MHz≈1.133ms
Type2	12×12	((256+16)×12)/2.4MHz≈1.36ms
Type3	16×16	((256+16)×16)/2.4MHz≈1.813ms

Last Page Set

This command is to set the last page displayed in a movie and the setting is also depending on the cycle time of loops played in a movie.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Last Page Set	W	0	0	0	1	0	1	0	1	15h
	W	X	X	X	X	MLP3	MLP2	MLP1	MLP0	00h

MLP3	MLP2	MLP1	MLP0	RAM Page Address						Remarks
				Gray Mode			Binary Mode			
				Matrix Type1	Matrix Type2	Matrix Type3	Matrix Type1	Matrix Type2	Matrix Type3	
0	0	0	0	Page1	Page1	Page1	Page1	Page1	Page1	(Default)
0	0	0	1	Page2	Page2	Page2	Page2	Page2	Page2	—
0	0	1	0	—	—	—	Page3	Page3	Page3	—
0	0	1	1	—	—	—	Page4	Page4	Page4	—
0	1	0	0	—	—	—	Page5	Page5	Page5	—
0	1	0	1	—	—	—	Page6	Page6	Page6	—
0	1	1	0	—	—	—	Page7	Page7	Page7	—
0	1	1	1	—	—	—	Page8	Page8	Page8	—
1	0	0	0	—	—	—	Page9	Page9	Page9	—
1	0	0	1	—	—	—	Page10	Page10	Page10	—
1	0	1	0	—	—	—	Page11	Page11	Page11	—
1	0	1	1	—	—	—	Page12	Page12	Page12	—
1	1	0	0	—	—	—	—	Page13	Page13	—
1	1	0	1	—	—	—	—	Page14	Page14	—
1	1	1	0	—	—	—	—	Page15	Page15	—
1	1	1	1	—	—	—	—	Page16	Page16	—

Note: 1. If programmed command data is not defined, the function will not be affected.

2. The three matrix types are shown below.

Matrix Type	Pixel
Type1	9×10 + 9×10
Type2	12×12
Type3	16×16

Picture Scrolling Control

This command is used to control the scrolling function on/off and picture scrolling direction.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Picture Scrolling Control	W	0	0	1	0	0	0	0	0	20h
	W	SCEN	X	RL	HSP4	HSP3	HSP2	HSP1	HSP0	00h

SCEN	Scrolling Function SW	Remarks
0	OFF	Default
1	ON	—

RL	Scrolling Direction	Remarks
0	Left	Default
1	Right	—

Horizontal Scrolling Speed = (HSP[4:0]+1)×32×1frame time

Horizontal Scrolling Speed = (1~32)×32×1frame time = (32~1024)×1frame time

For example, When type1of Matrix type is selected and HSP[4:0] = 3,

Horizontal Scroll Speed = 4×32×1.133(ms) = 145.024ms

Matrix Types	Pixel	HSP [4:0]	1 Frame Time	Picture Horizongtal Scrolling Speed
Type1	(9×10) + (9×10)	3	1.133ms	145.024ms
Type2	12×12	3	1.36ms	174.08ms
Type3	16×16	3	1.813ms	232.064ms

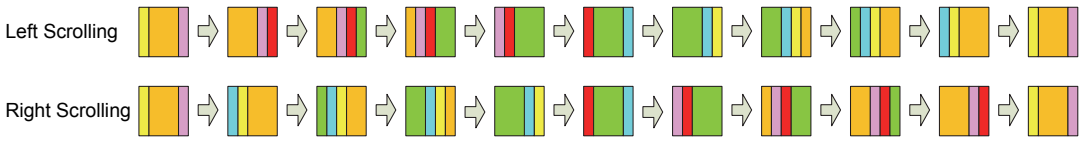
Note: 1. If programmed command data is not defined, the function will not be affected.
2. Single row horizontal scrolling.
3. When the scrolling mode is enabled, it is not recommended to execute the fade function and movie function.
4. The function is suitable for the Gray Mode only. In the Binary Mode, the scrolling function is invalid.
5. The setup time is based on OSC frequency.

Matrix Types	Pixel	1 Frame Time
Type1	9×10 + 9×10	((256+16)×10)/2.4MHz≈1.133ms
Type2	12×12	((256+16)×12)/2.4MHz≈1.36ms
Type3	16×16	((256+16)×16)/2.4MHz≈1.813ms

Example – Horizontal Scrolling Set

Set the display RAM data for each page as follows:

After the scrolling function is enabled, the status of left or right scrolling is as follows:



Display Mode

This command is used to set the LED matrix display mode.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Display Mode	W	0	0	1	1	0	0	0	0	30h
	W	X	X	X	X	X	X	X	MP	00h

MP	Display Mode	Remarks
0	Picture	Default
1	Movie	—

Note: If programmed command data is not defined, the function will not be affected.

Configuration Mode

The command is used to set the binary mode or Gray Scale mode and the embedded Matrix types.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Binary/Gray Select	W	0	0	1	1	0	0	0	1	31h
	W	BGS	X	X	X	X	X	MT1	MT0	01h

BGS	Select	Remarks
0	Gray	Default
1	Binary	—

MT1	MT0	Matrix Types	Pixel	Remarks
0	1	Type1	9×10 + 9×10	Default
1	0	Type2	12×12	—
1	1	Type3	16×16	—

Note: If programmed command data is not defined, the function will not be affected.

Fade Function Control

This command is used to control the fade function on/off, the display option. This command parameter is validated during the Timing 1 period of each frame when the command is set.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Fade Function Control	W	0	0	1	1	0	0	1	0	32h
	W	FFEN	GMEN	GFEN	FOT	FET1	FET0	FLT1	FLT0	4Ah

FFEN	Fade Function Control SW	Remarks
0	Disable	Default
1	Enable	—

GMEN	CA Output Option Selection	Remarks
0	Linear Intensity Mode	—
1	Gamma Intensity Mode	Default

GFEN	Display Option Selection	Remarks
0	Each Dot	Default
1	Global	—

FOT	Fade Out Time Control (T3)	Remarks
0	T1	Default
1	T1×2	—

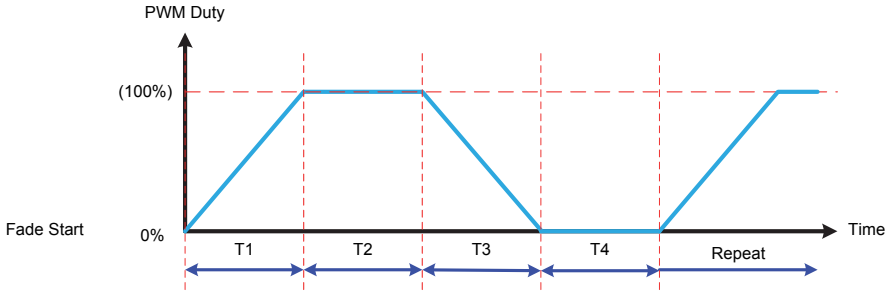
FET1	FET0	Extinguish Time Control (T4)	Remarks
0	0	T1×0.25	—
0	1	T1×0.5	—
1	0	T1	Default
1	1	T1×2	—

FLT1	FLT0	Light Time Control (T2)	Remarks
0	0	T1×0.25	—
0	1	T1×0.5	—
1	0	T1	Default
1	1	T1×2	—

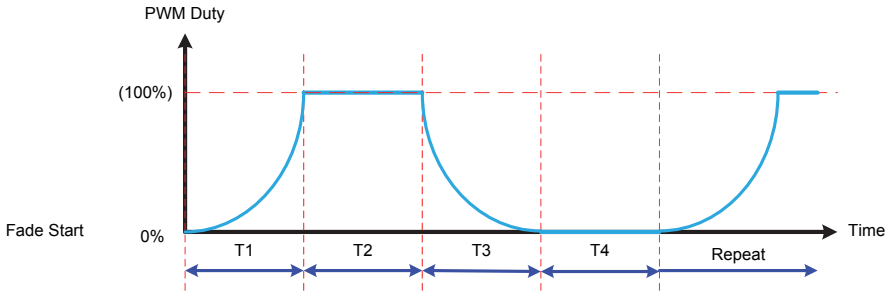
Note: 1. If programmed command data is not defined, the function will not be affected.
2. The T1 time is controlled by the Write Dot Fade Data Command of RAM R/W commands.
3. In the Binary Mode the Fade for each dot function is invalid.

Fade Function

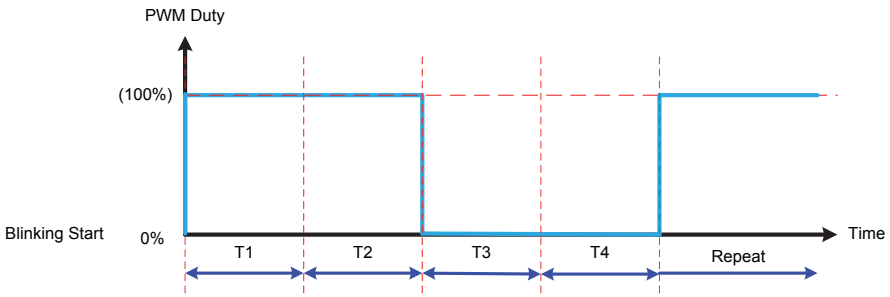
(1) Linear intensity mode



(2) Gamma intensity mode



Blinking Function



Global Fade Time

The device contains a versatile blinking function. The whole display can be made to blink or fade times selected by the global blinking/fade time command, this command parameter is validated by each timing 1 of frame when the command is set.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Global Fade Time	W	0	0	1	1	0	0	1	1	33h
	W	GFS	X	X	X	X	GFT2	GFT1	GFT0	00h

Note: The blinking times are integer multiples of the system frequency. The ratios between the system oscillator and the blinking times depend upon the mode, in which the device is operating.

GFS	Select	Remarks
0	Fade Mode	Default
1	Global Blink Mode	—

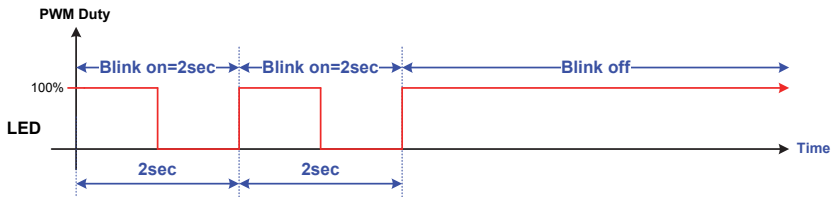
GFT2	GFT1	GFT0	Global Fade Time (T1)	Remarks
0	0	0	OFF	Default
0	0	1	256 frames	1×256
0	1	0	512 frames	2×256
0	1	1	1024 frames	4×256
1	0	0	1536 frames	6×256
1	0	1	2048 frames	8×256
1	1	0	2560 frames	10×256
1	1	1	3072 frames	12×256

Note: 1. If programmed command data is not defined, the function will not be affected.
2. The setup time is based on OSC frequency.

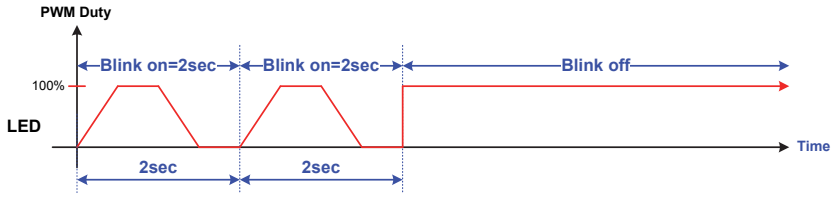
Matrix Types	Pixel	1 Frame Time
Type1	9×10 + 9×10	((256+16)×10)/2.4MHz≈1.133ms
Type2	12×12	((256+16)×12)/2.4MHz≈1.36ms
Type3	16×16	((256+16)×16)/2.4MHz≈1.813ms

Examples

- Blink Output Type – Blinking Time = 2sec



- Fade Output Type – Blinking Time = 2sec



Cascade Mode

This command will select master/slave mode and input clock source.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Cascade Mode	W	0	0	1	1	0	1	0	0	34h
	W	X	X	X	X	X	X	MS1	MS0	00h

MS1	MS0	SYNC pin Status	Remarks
0	0	High impedance	Default value, only single chip applications
0	1	Oscillator output mode	Master Mode
1	0	Oscillator input mode	Slave Mode
1	1	High impedance	—

Note: It is not recommended to change between MASTER and SLAVE mode after a system oscillator enable.

System Control

This command controls the system oscillator on/off and display on/off.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
System Control	W	0	0	1	1	0	1	0	1	35h
	W	X	X	X	X	X	X	FON	DON	00h

FON	DON	System Oscillator	LED Display	Remarks
0	X	Off	Off	1. Default 2. Standby mode 3. Temperature protection disable
1	0	On	Off	display off mode and enable internal system OSC
1	1	On	On	Normal display mode

Note: If programmed command data is not defined, the function will not be affected.

Constant Current Ratio

This command is used to select the constant current ratio according to the LED panel characteristics.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Constant Current Ratio	W	0	0	1	1	0	1	1	0	36h
	W	X	X	X	X	CC3	CC2	CC1	CC0	0Ah

CC3	CC2	CC1	CC0	Constant Current Ratio	Remarks
0	0	0	0	3mA	—
0	0	0	1	6mA	—
0	0	1	0	9mA	—
0	0	1	1	12mA	—
0	1	0	0	15mA	—
0	1	0	1	18mA	—
0	1	1	0	21mA	—
0	1	1	1	24mA	—
1	0	0	0	27mA	—
1	0	0	1	30mA	—
1	0	1	0	33mA	Default
1	0	1	1	36mA	—
1	1	0	0	39mA	—
1	1	0	1	42mA	—
1	1	1	0	45mA	—
1	1	1	1	48mA	—

Note: 1. If programmed command data is not defined, the function will not be affected.
2. The setup constant current ratio is based on CA_scan number.

Matrix Types	Pixel	1 Frame Time
Type1	9×10 + 9×10	((256+16)×10)/2.4MHz≈1.133ms
Type2	12×12	((256+16)×12)/2.4MHz≈1.36ms
Type3	16×16	((256+16)×16)/2.4MHz≈1.813ms

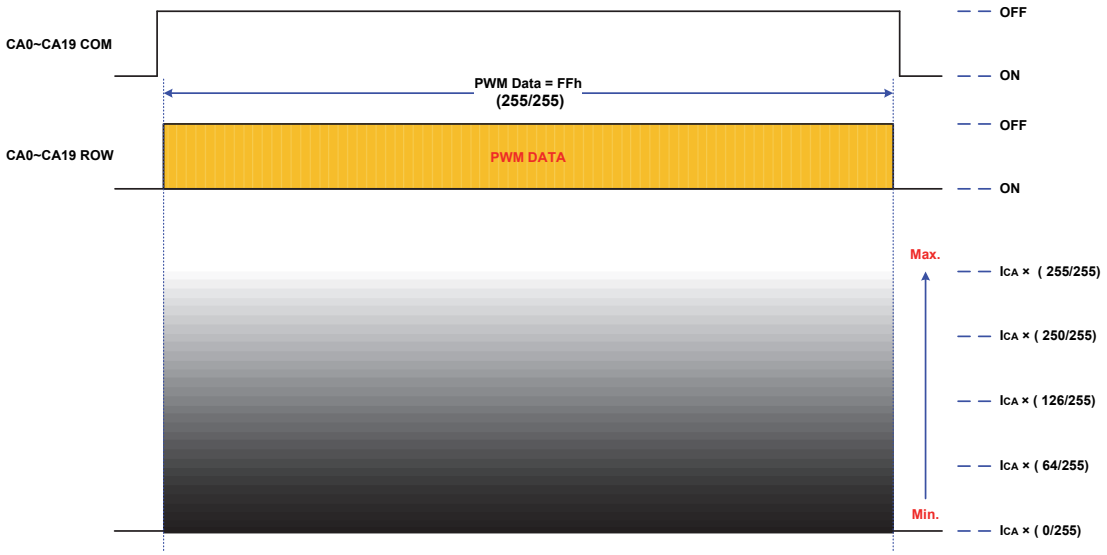
Brightness Control

This command is to control the 256-step PWM luminance control. It has a common setting for all dots by digital dimming duty adjustment.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Brightness control	W	0	0	1	1	0	1	1	1	37h
	W	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	FFh

BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	Digital Dimming Duty	Remarks
0	0	0	0	0	0	0	0	0/255	—
0	0	0	0	0	0	0	1	1/255	—
0	0	0	0	0	0	1	0	2/255	—
⋮								⋮	⋮
0	0	0	1	0	0	0	0	16/255	—
0	0	0	1	0	0	0	1	17/255	—
0	0	0	1	0	0	1	0	18/255	—
⋮								⋮	⋮
1	0	0	0	0	0	0	0	128/255	—
1	0	0	0	0	0	0	1	129/255	—
1	0	0	0	0	0	1	0	130/255	—
⋮								⋮	⋮
1	1	1	1	1	1	0	0	252/255	—
1	1	1	1	1	1	0	1	253/255	—
1	1	1	1	1	1	1	0	254/255	—
1	1	1	1	1	1	1	1	255/255	Default

Note: The luminance = Maximum constant current ratio set values (I_{CA}) × Brightness Digital Dimming Duty (set by BC[7:0]), as shown in the accompanying diagram.



Mode Control

This command is used to control the thermal shutdown circuit and open/short detection functions.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Mode Control	W	0	0	1	1	1	0	0	0	38h
	W	TSDEN	TSDS	X	X	X	X	ODEN	SDEN	00h

TSDEN	TSDS	Temperature Protection SW	Control Mode	Remarks
0	X	OFF	—	Default
1	0	ON	User Control	Users read TSDF flag to control the display on/off
1	1	ON	Auto Control	Auto control the display on/off

ODEN	Open Detection Start	Remarks
0	OFF (Cleared by H/W Automatically)	Default
1	ON (Auto detect)	—

SDEN	Short Detection Start	Remarks
0	OFF (Cleared by H/W Automatically)	Default
1	ON (Auto detect)	—

Note: 1. If the TSDS bit is “1”, the Temperature protection function will enter Auto control mode:

- When the chip junction temperatures exceeds 150°C, the entire IC display will be off.
- When the chip junction temperatures falls below 125°C.The device will resume operation with a normal display.

2. If the TSDS bit is “0”, the Temperature protection function will enter user control mode:
   - The TSDF flag bit will be read to determine if the IC display is off.
   - When the chip junction temperatures exceeds 150°C, the TSDF flag bit is set to “1”.
   - When the chip junction temperatures falls below 125°C, the TSDF flag bit is cleared to “0”.

3. Open/Short detection can be enabled through ODEN/SDEN bit setting.
   Firstly use the constant current ratio command to set the LED current. It is recommended to use 9mA for this test.
   And then enable the open/short detection. Lastly read the open/short detection data.
   - Once the ODEN/SDEN is set high to enable the detection function, all other operation modes are ignored and the system starts to re-run the LED matrix for the LED open short detection. And the ODEN/SDEN will be cleared to “0” by H/W automatically.
   - To implement open/short detection or not depends on the LED Control RAM settings. Any bit set as “0” in LED Control RAM means no open short detection will run at that corresponding LED location. Also, the corresponding bit in ODEN/SDEN bit will always be “0” after open short detection is completed.

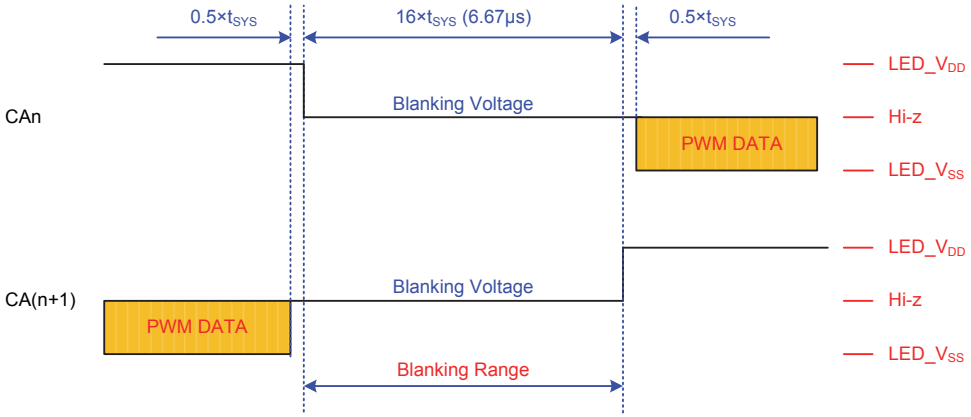
Blanking Control Voltage Setting

This command is used to control the blanking control voltage on/off function as well as setting the value of the blanking control voltage during the LED output blanking time.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Blanking Voltage Set	W	0	0	1	1	1	0	0	1	39h
	W	VBEN	X	X	X	VB3	VB2	VB1	VB0	0Fh

VBEN	Blanking Voltage Function SW	Remarks
0	OFF	Default
1	ON	—

VB3	VB2	VB1	VB0	Blanking Voltage (V)	Remarks
0	0	0	0	LED_V_{SS}	—
0	0	0	1	LED_V_{DD} × (1/15)	—
0	0	1	0	LED_V_{DD} × (2/15)	—
0	0	1	1	LED_V_{DD} × (3/15)	—
0	1	0	0	LED_V_{DD} × (4/15)	—
0	1	0	1	LED_V_{DD} × (5/15)	—
0	1	1	0	LED_V_{DD} × (6/15)	—
0	1	1	1	LED_V_{DD} × (7/15)	—
1	0	0	0	LED_V_{DD} × (8/15)	—
1	0	0	1	LED_V_{DD} × (9/15)	—
1	0	1	0	LED_V_{DD} × (10/15)	—
1	0	1	1	LED_V_{DD} × (11/15)	—
1	1	0	0	LED_V_{DD} × (12/15)	—
1	1	0	1	LED_V_{DD} × (13/15)	—
1	1	1	0	LED_V_{DD} × (14/15)	—
1	1	1	1	LED_V_{DD}	Default



Read Open Detection Data

The read open detection data format is as below.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Read Open Detection Data	W	0	1	1	1	0	1	0	0	74h
	R	Dummy Data								00h
	R	Read Data								—

Note: Each dot Detect time is equal to the input CLK pulse time.

- Matrix-type3: 16×16

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.	Remarks
1st	0	1	1	1	0	1	0	0	74h	Command
2nd	0	0	0	0	0	0	0	0	00h	Dummy
3rd	C1-1	C1-2	C1-3	C1-4	C1-5	C1-6	C1-7	C1-8	00h	Data
4th	C1-9	C1-10	C1-11	C1-12	C1-13	C1-14	C1-15	C1-16	00h	Data
---				---					---	---
33rd	C16-1	C16-2	C16-3	C16-4	C16-5	C16-6	C16-7	C16-8	00h	Data
34th	C16-9	C16-10	C16-11	C16-12	C16-13	C16-14	C16-15	C16-16	00h	Data

- Matrix-type2: 12×12

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.	Remarks
1st	0	1	1	1	0	1	0	0	74h	Command
2nd	0	0	0	0	0	0	0	0	00h	Dummy
3rd	C1-1	C1-2	C1-3	C1-4	C1-5	C1-6	C1-7	C1-8	00h	Data
4th	C1-9	C1-10	C1-11	C1-12	C2-1	C2-2	C2-3	C2-4	00h	Data
5th	C2-5	C2-6	C2-7	C2-8	C2-9	C2-10	C2-11	C2-12	00h	Data
---				---					---	---
18th	C11-1	C11-2	C11-3	C11-4	C11-5	C11-6	C11-7	C11-8	00h	Data
19th	C11-9	C11-10	C11-11	C11-12	C12-1	C12-2	C12-3	C12-4	00h	Data
20th	C12-5	C12-6	C12-7	C12-8	C12-9	C12-10	C12-11	C12-12	00h	Data

- Matrix-type1: 9×10 + 9×10

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.	Remarks
1st	0	1	1	1	0	1	0	0	74h	Command
2nd	0	0	0	0	0	0	0	0	00h	Dummy
3rd	C1-1	C1-2	C1-3	C1-4	C1-5	C1-6	C1-7	C1-8	00h	Data
4th	C1-9	C1-10	C1-11	C1-12	C1-13	C1-14	C1-15	C1-16	00h	Data
5th	C1-17	C1-18	C2-1	C2-2	C2-3	C2-4	C2-5	C2-6	00h	Data
---				---					---	---
23rd	C9-17	C9-18	C10-1	C10-2	C10-3	C10-4	C10-5	C10-6	00h	Data
24th	C10-7	C10-8	C10-9	C10-10	C10-11	C10-12	C10-13	C10-14	00h	Data
25th	C10-15	C10-16	C10-17	C10-18	C1-1	C1-2	C1-3	C1-4	00h	Data

Read Short Detection Data

The read short detection data format is as below.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Read Short Detection Data	W	0	1	1	1	0	1	0	1	75h
	R	Dummy Data								00h
	R	Read Data								—

Note: Each dot Detect time is equal to the input CLK pulse time.

- Matrix-type3: 16×16

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.	Remarks
1st	0	1	1	1	0	1	0	1	75h	Command
2nd	0	0	0	0	0	0	0	0	00h	Dummy
3rd	C1-1	C1-2	C1-3	C1-4	C1-5	C1-6	C1-7	C1-8	00h	Data
4th	C1-9	C1-10	C1-11	C1-12	C1-13	C1-14	C1-15	C1-16	00h	Data
---				---					---	---
33rd	C16-1	C16-2	C16-3	C16-4	C16-5	C16-6	C16-7	C16-8	00h	Data
34th	C16-9	C16-10	C16-11	C16-12	C16-13	C16-14	C16-15	C16-16	00h	Data

- Matrix-type2: 12×12

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.	Remarks
1st	0	1	1	1	0	1	0	1	75h	Command
2nd	0	0	0	0	0	0	0	0	00h	Dummy
3rd	C1-1	C1-2	C1-3	C1-4	C1-5	C1-6	C1-7	C1-8	00h	Data
4th	C1-9	C1-10	C1-11	C1-12	C2-1	C2-2	C2-3	C2-4	00h	Data
5th	C2-5	C2-6	C2-7	C2-8	C2-9	C2-10	C2-11	C2-12	00h	Data
---				---					---	---
18th	C11-1	C11-2	C11-3	C11-4	C11-5	C11-6	C11-7	C11-8	00h	Data
19th	C11-9	C11-10	C11-11	C11-12	C12-1	C12-2	C12-3	C12-4	00h	Data
20th	C12-5	C12-6	C12-7	C12-8	C12-9	C12-10	C12-11	C12-12	00h	Data

- Matrix-type1: 9×10+9×10

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.	Remarks
1st	0	1	1	1	0	1	0	1	75h	Command
2nd	0	0	0	0	0	0	0	0	00h	Dummy
3rd	C1-1	C1-2	C1-3	C1-4	C1-5	C1-6	C1-7	C1-8	00h	Data
4th	C1-9	C1-10	C1-11	C1-12	C1-13	C1-14	C1-15	C1-16	00h	Data
5th	C1-17	C1-18	C2-1	C2-2	C2-3	C2-4	C2-5	C2-6	00h	Data
---				---					---	---
23rd	C9-17	C9-18	C10-1	C10-2	C10-3	C10-4	C10-5	C10-6	00h	Data
24th	C10-7	C10-8	C10-9	C10-10	C10-11	C10-12	C10-13	C10-14	00h	Data
25th	C10-15	C10-16	C10-17	C10-18	C1-1	C1-2	C1-3	C1-4	00h	Data

Read Register Status

The command can be used to obtain the device internal status. The read register status format is as below.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Read Status	W	0	1	1	1	0	0	0	0	70h
	R	Read Data								—

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description	Def.
—	0	1	1	1	0	0	0	0	Read Register Status Command	70h
1st	X	X	X	X	X	X	X	MP	Picture /Movie display mode	00h
2nd	BGS	X	X	X	X	X	MT1	MT0	Binary/Gray mode and embedded Matrix types	01h
3rd	FFEN	GMEN	GFEN	FOT	FET1	FET0	FLT1	FLT0	FADE Parameters	4Ah
4th	GFS	X	X	X	X	GFT2	GFT1	GFT0	Global FADE time	00h
5th	X	X	X	X	X	X	MS1	MS0	Master or slave mode	00h
6th	X	X	X	X	X	X	FON	DON	Controls the system oscillator on/off and display on/off status	00h
7th	X	X	X	X	CC3	CC2	CC1	CC0	Constant current ratio	0Ah
8th	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	256 luminance steps	FFh
9th	TSDEN	TSDS	X	X	X	X	ODEN	SDEN	Thermal protect SW Open/short on/off SW	00h
10th	VBEN	X	X	X	VB3	VB2	VB1	VB0	16 blanking voltage steps	00h
11th	SCEN	X	RL	HSP4	HSP3	HSP2	HSP1	HSP0	Scrolling function status	00h
12th	X	X	X	X	PFS3	PFS2	PFS1	PFS0	Picture display address	00h
13th	MEN	X	X	X	MFS3	MFS2	MFS1	MFS0	Movie display first address	00h
14th	X	X	X	X	MFL3	MFL2	MFL1	MFL0	Movie display play length	01h
15th	X	X	X	X	MCT3	MCT2	MCT1	MCT0	Movie display play cycles time	00h
16th	X	X	MPD5	MPD4	MPD3	MPD2	MPD1	MPD0	Delay time between page changes in a movie	04h
17th	X	X	X	X	MLP3	MLP2	MLP1	MLP0	The Last Page in a movie	00h

Read Movie Frame Status

The read movie frame status format is as below.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Read Movie Frame Status	W	0	1	1	1	0	0	0	1	71h
	R	MOF1	MOF0	X	X	MDF3	MDF2	MDF1	MDF0	00h

MOF1	MOF0	Movie Operation Status	Remarks
0	X	No Movie	—
1	0	Movie is Playing	—
1	1	Movie is finished	—

MDF3	MDF2	MDF1	MDF0	RAM Page Address						Remarks
				Gray Mode			Binary Mode			
				Matrix Type1	Matrix Type2	Matrix Type3	Matrix Type1	Matrix Type2	Matrix Type3	
0	0	0	0	Page1	Page1	Page1	Page1	Page1	Page1	(Default)
0	0	0	1	Page2	Page2	Page2	Page2	Page2	Page2	—
0	0	1	0	—	—	—	Page3	Page3	Page3	—
0	0	1	1	—	—	—	Page4	Page4	Page4	—
0	1	0	0	—	—	—	Page5	Page5	Page5	—

MDF3	MDF2	MDF1	MDF0	RAM Page Address						Remarks
				Gray Mode			Binary Mode			
				Matrix Type1	Matrix Type2	Matrix Type3	Matrix Type1	Matrix Type2	Matrix Type3	
0	1	0	1	—	—	—	Page6	Page6	Page6	—
0	1	1	0	—	—	—	Page7	Page7	Page7	—
0	1	1	1	—	—	—	Page8	Page8	Page8	—
1	0	0	0	—	—	—	Page9	Page9	Page9	—
1	0	0	1	—	—	—	Page10	Page10	Page10	—
1	0	1	0	—	—	—	Page11	Page11	Page11	—
1	0	1	1	—	—	—	Page12	Page12	Page12	—
1	1	0	0	—	—	—	—	Page13	Page13	—
1	1	0	1	—	—	—	—	Page14	Page14	—
1	1	1	0	—	—	—	—	Page15	Page15	—
1	1	1	1	—	—	—	—	Page16	Page16	—

Note: 1. If programmed command data is not defined the function will not be affected.
2. The three matrix types are shown below.

Matrix Type	Pixel
Type1	9×10 + 9×10
Type2	12×12
Type3	16×16

Read Movie Loop Status

The read movie loop status format is as below.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Read Movie Loop Status	W	0	1	1	1	0	0	1	0	72h
	R	MOL1	MOL0	X	X	MLP3	MLP2	MLP1	MLP0	00h

MOL1	MOL0	Movie Operation Status	Remarks
0	X	No Movie	—
1	0	Loops are playing	—
1	1	Loop play is finished	—

MLP3	MLP2	MLP1	MLP0	Playing Loop	Remarks
0	0	0	0	Loop1	—
0	0	0	1	Loop2	—
0	0	1	0	Loop3	—
0	0	1	1	Loop4	—
0	1	0	0	Loop5	—
0	1	0	1	Loop6	—
0	1	1	0	Loop7	—
0	1	1	1	Loop8	—
1	X	X	X	Play movie endless	Playing Loop1~loop8 repeatedly

Read Function Flag

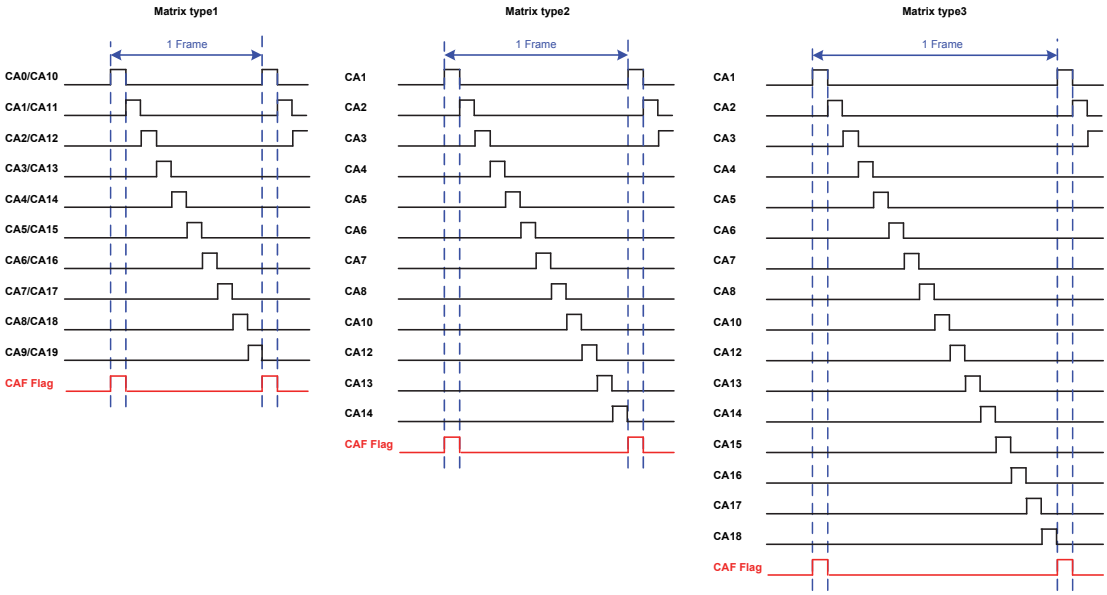
The read function flag format is as below.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Read Function Flag	W	0	1	1	1	0	0	1	1	73h
	R	CAF	X	X	X	X	X	X	TSDF	00h

CAF	Scanning Location	Remarks
0	Other CA	—
1	CA0/CA10	Matrix Type1
	CA1	Matrix Type2
	CA1	Matrix Type3

TSDF	Chip Junction Temperature	Remarks
0	< 125°C	Default When the chip junction temperature falls below 125°C, the TSDF flag bit is cleared to “0”.
1	> 150°C	When the chip junction temperature exceeds 150°C, the TSDF flag bit is set to “1”.

The relationship between the CAn scanning location and CAF flag is shown as follows.



Note: For the Matrix type 1, CAn means CA0 or CA10; For the Matrix type 2 and Matrix type 3, CAn means CA1.

SPI 3-wire Serial Interface

The HT16D33A device includes an SPI 3-wire serial interface.

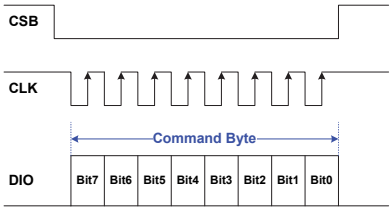
The CSB pin is used to identify the transmitted data. The transmission is controlled by the active low signal CSB. After the CSB falls to a low level, the data can start to be transferred. The data is transferred from the MSB of each byte (MSB First), and the data is shifted into a register at the rising edge of CLK. The input data is automatically loaded into a register for every 8 bits of input data. The sequence starts from the falling edge of the CSB signal.

For the read mode, when CSB is low the DIO pin will change into an output mode after sending a read command code and the start read address setup value. If the MCU sets the CSB signal to a high level after receiving the output data, the DIO pin will be changed into an input mode and the read mode cycle will terminate. For the read mode, the data is outputted from DIO pin at falling edge of CLK.

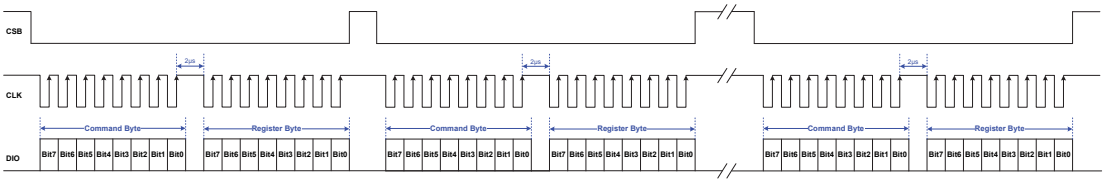
Write Operation

Command Byte Transfer

- **Single Command Byte**

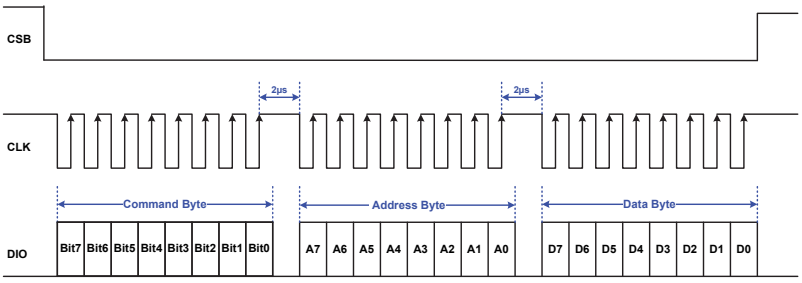


- **Compound Command Byte**



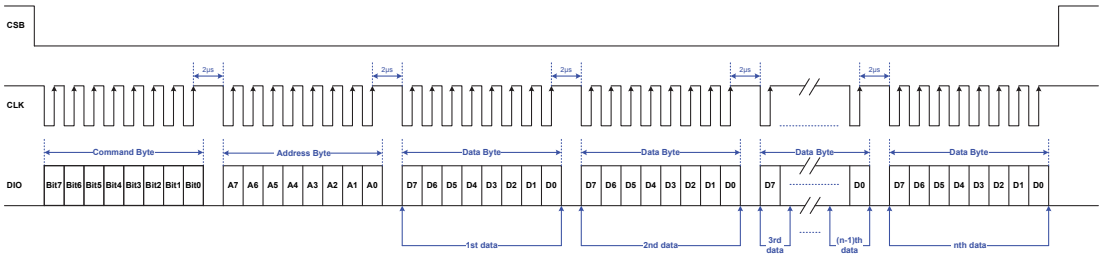
Data Byte Transfer

- **Single Write RAM Data Operation**



Note: If the input memory location value is greater than the limit value, the input memory location value will be invalid.

• **Pages Write RAM Data Operation**



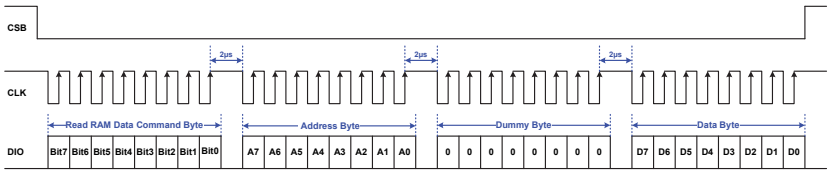
Note: If the memory location exceeds the limit value, the memory pointer will return to 00H. The Memory location limit values are shown as below.

Mode	Matrix-type	Memory Location Limit Value			Note (Matrix)
		Display Data	Fade Data	LED On/Off Control	
Binary	Type1	1Dh	No support function	No support function	9×10 + 9×10
	Type2	11h	No support function	No support function	12×12
	Type3	1Fh	No support function	No support function	16×16
Gray	Type1	B3h	9Fh	1Dh	9×10 + 9×10
	Type2	BBh	B5h	11h	12×12
	Type3	FFh	7Fh	1Fh	16×16

Read Operation

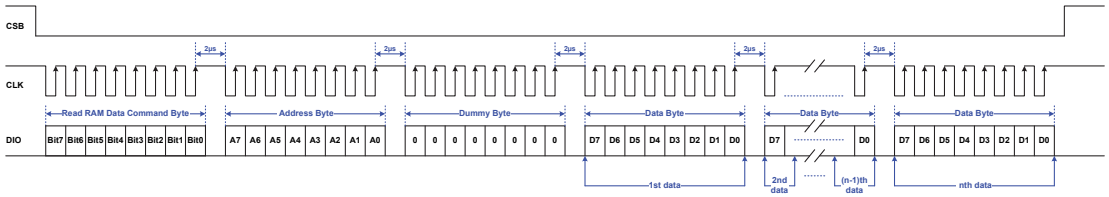
1. The data must be read in byte units.
2. It is recommended that the host controller should read in the data from the DIO line between the rising edge of the CLK line and the falling edge of the next CLK line.

• **Single Read RAM Data Operation**



Note: If the input memory location value is greater than the limit value, the input memory location value will be invalid.

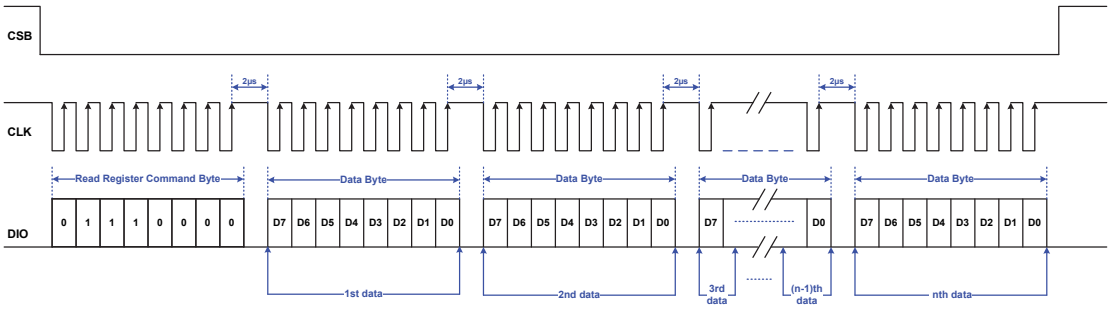
• **Page Read RAM Data Operation**



Note: If the memory location exceeds the limit value, the memory pointer will return to 00H. The Memory location limit values are shown as below.

Mode	Matrix-type	Memory Location Limit Value			Note (Matrix)
		Display Data	Fade Data	LED On/Off Control	
Binary	Type1	1Dh	No support function	No support function	9×10 + 9×10
	Type2	11h	No support function	No support function	12×12
	Type3	1Fh	No support function	No support function	16×16
Gray	Type1	B3h	9Fh	1Dh	9×10 + 9×10
	Type2	BBh	B5h	11h	12×12
	Type3	FFh	7Fh	1Fh	16×16

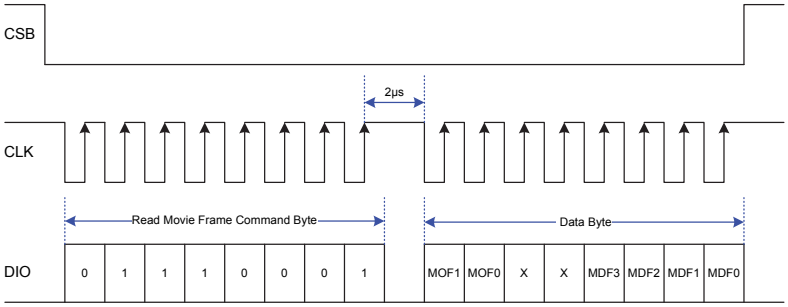
Read Register Status



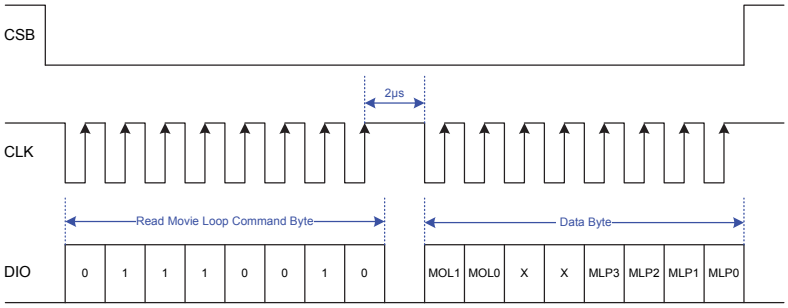
Note: 1. The display data must be read in byte units.

2. If the register location exceeds limit value, the register pointer will return to the first location. The register location limit value is 17th address.

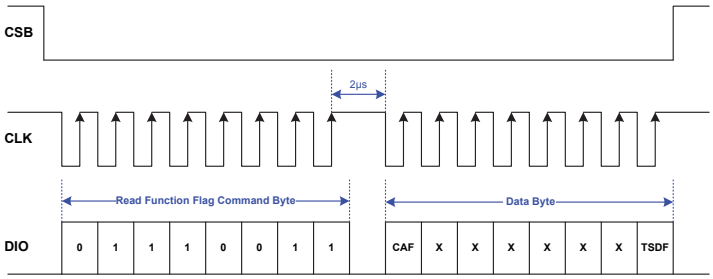
• Read Movie Frame Status



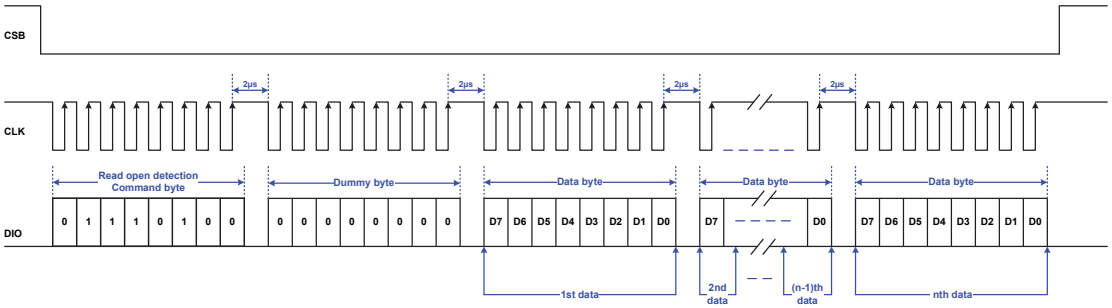
• Read Movie Loop Status



• **Read Function Flag**



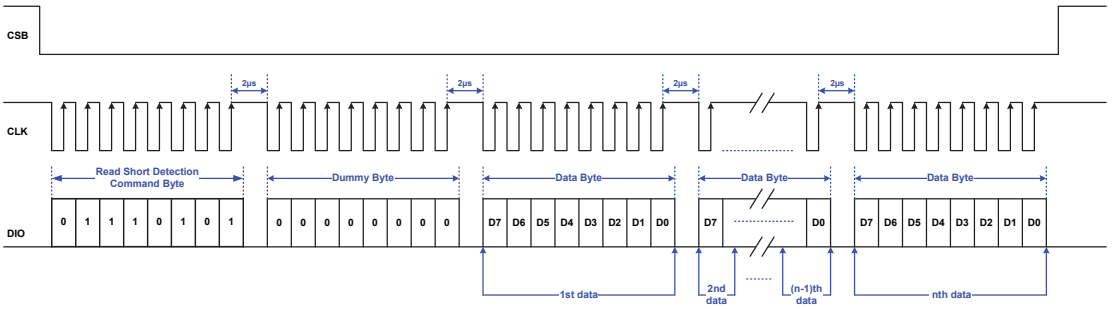
• **Read Open Detection Data**



Note: 1. The display data must be read in byte units.

2. Matrix type3 (16×16): If the register location exceeds limit value, the register pointer will return to the first location. The register location limit value is 32nd address.

• **Read Short Detection Data**



Note: 1. The display data must be read in byte units.

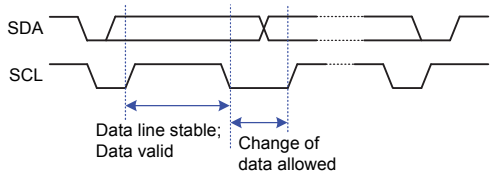
2. Matrix type3 (16×16): If the register location exceeds limit value, the register pointer will return to the first location. The register location limit value is 32nd address.

I²C Serial Interface

The HT16D33B device includes an I²C serial interface. The I²C bus is a bidirectional two-line communication link between different ICs or modules. The two lines of the interface are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to the positive supply via a pull-up resistor, typical 10kΩ for a frequency of 100kHz. When the bus is free both lines are high. The output stages of devices connected to the bus must have open-drain or open-collector types to implement the wired-AND function necessary for connection. Data transfer is initiated only when the bus is not busy.

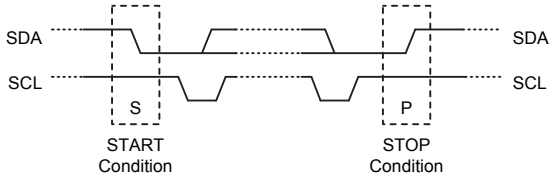
Data Validity

The data on the SDA line must be stable during the clock high period. The high or low state of the data line can only change when the clock signal on the SCL line is low as shown in the accompanying diagram.



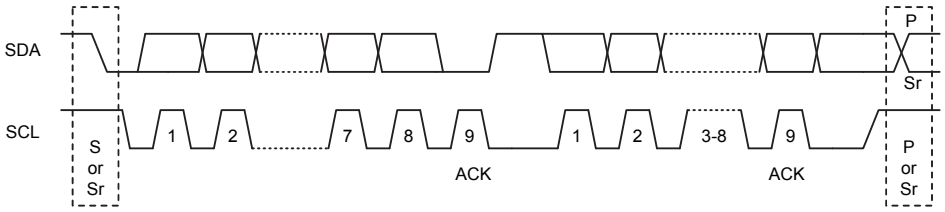
START and STOP Conditions

- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus remains busy if a repeated START (Sr) is generated instead of a STOP condition. The START(S) and repeated START (Sr) conditions are functionally identical.



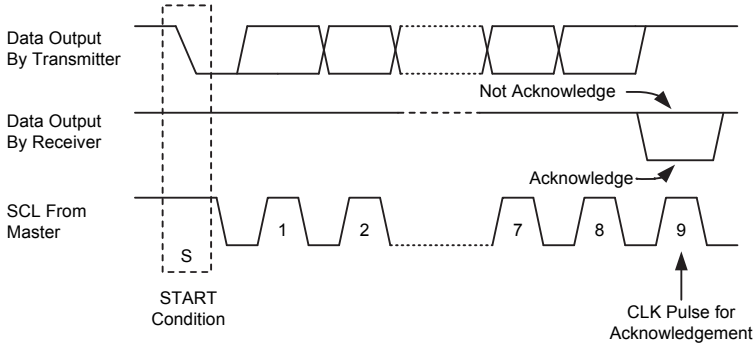
Byte Format

Every byte put on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.



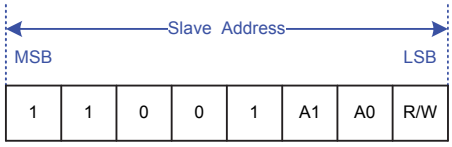
Acknowledge

- Each byte of eight bit length is followed by one acknowledge bit. This acknowledges bit is a low level placed on the bus by the receiver. The master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an Acknowledge, ACK, after the reception of each byte.
- The device that provides an Acknowledge must pull down the SDA line during the acknowledge clock pulse so that it remains at a stable low level during the high period of this clock pulse.
- A master receiver must signal an end of data to the slave by generating a not-acknowledge, NACK, bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse so as to not acknowledge. The master will generate a STOP or a repeated START condition.



Slave Addressing

- The device requires an 8-bit slave address word following a start condition to enable the device for a write operation. The device address word consist of a mandatory one, zero sequence for the first four most significant bits. Refer to the diagram showing the slave Address. This is common to all LED devices.
- The slave address byte is the first byte received following the START condition from the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines whether a read or write operation is to be performed. When the R/W bit is "1", then a read operation is selected. A "0" selects a write operation.
- When a slave address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an Acknowledge on the SDA line.
- The address bits are "1, 1, 0, 0, 1, A1, A0".

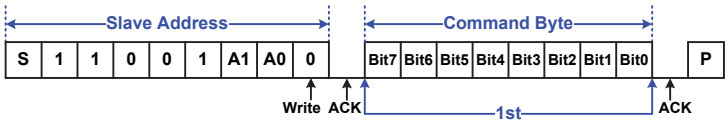


Note: 1. When the AD pin is connected to V_{SS} (GND), the [A1,A0] bits should be set to [0,0]
2. When the AD pin is connected to V_{DD}, the [A1,A0] bits should be set to [1,1]
3. When the AD pin is connected to the SCL, the [A1,A0] bits should be set to [0,1]
4. When the AD pin is connected to the SDA, the [A1,A0] bits should be set to [1,0]
5. Common address that all devices are responding on the slave address bits are "0,1,0,1,1,1,0"

Write Operation

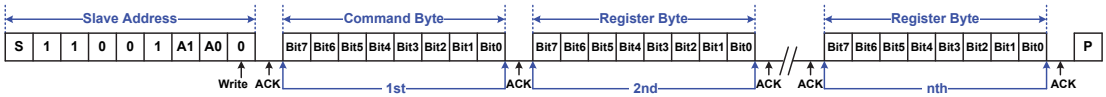
Single Command Byte

Byte write operation requires a START condition, slave address with R/W bit, a command (1st) and a STOP condition for single command byte.



Compound Command Byte

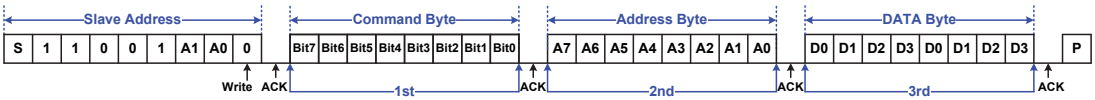
A byte write operation requires a START condition, a slave address with an R/W bit, a command (1st), one or more register byte command (2nd ~nth) and a STOP condition for compound command byte.



Note: If the input memory location value is greater than limit value, the input memory location value will invalid.

Single Write RAM Data Byte Operation

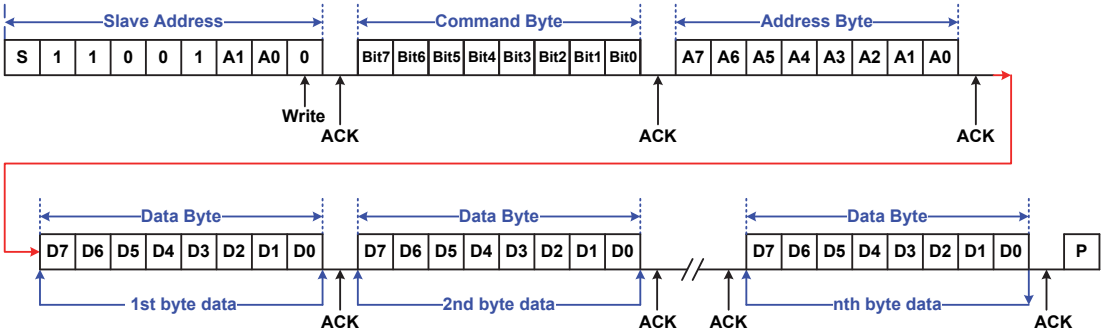
Following a START condition, the slave address with an R/W bit is placed on the bus. Then follows the display data address setting command code (1st) and the address point (An) is written to the address pointer (2nd) and then valid data and a STOP condition for a compound write single data byte.



Note: If the input memory location value is greater than limit value, the input memory location value will invalid.

Page Write RAM Data Operation

Following a START condition, the slave address with a R/W bit is placed on the bus along with the display data address setting command code (1st) and the address point (An) (2nd). The data to be written to the memory is next, after which the internal address pointer is incremented to the next address location on the reception of an acknowledge clock.



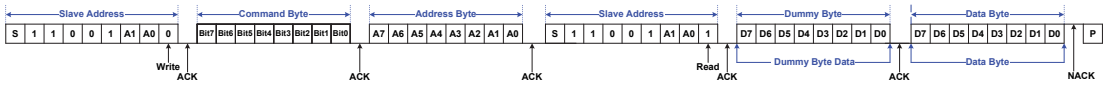
Note: If memory location exceeds limit value, the memory pointer will return to 00H. The Memory location limit values are shown as below:

Mode	Matrix-Type	Memory Location Limit Value			Note (Matrix)
		Display Data	Fade Data	LED On/Off Control	
Binary	Type1	1Dh	No support function	No support function	9×10 + 9×10
	Type2	11h	No support function	No support function	12×12
	Type3	1Fh	No support function	No support function	16×16
Gray	Type1	B3h	9Fh	1Dh	9×10 + 9×10
	Type2	BBh	B5h	11h	12×12
	Type3	FFh	7Fh	1Fh	16×16

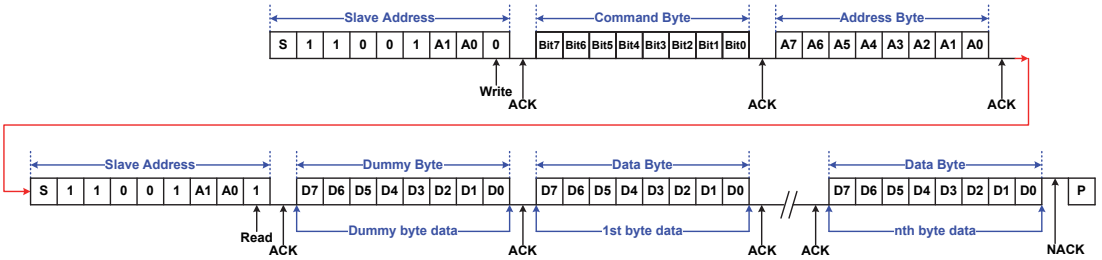
Read Operation

In this mode, the master reads the device data after setting the slave address. Following the R/W bit (= "0"), and the acknowledge bit, then follows the address setting command code (1st). After this is the address pointer (An) which is written to the address pointer (2nd). Next come the START condition and slave address, followed by an R/W bit (= "1"). The addressed data is then transmitted. The address pointer is only incremented on reception of an acknowledge clock. The device will place the data at address An+1 onto the bus. The master reads and acknowledges the new byte and the address pointer is incremented to "An+2". If only a read command is sent to the I^2C interface, then dummy data is transmitted. This cycle for reading consecutive addresses will continue until the master sends a NACK and STOP condition.

Single Read RAM Data Operation



Page Read RAM Data Operation



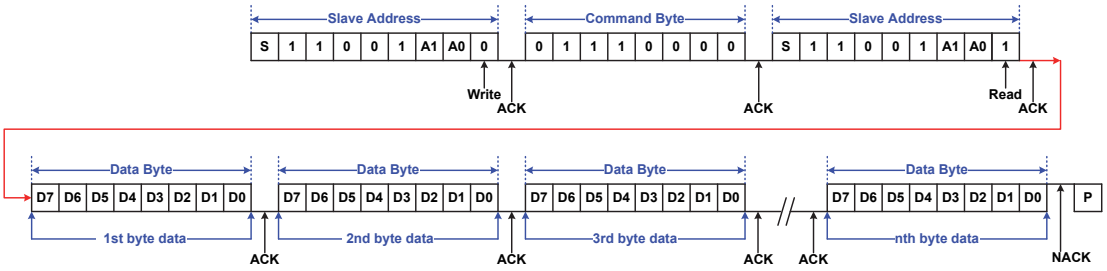
Note: 1. This cycle to read consecutive addresses will continue until the master sends a NACK and STOP condition.

2. If memory location exceeds limit value, the memory pointer will return to 00H. The Memory location limit values are shown as below.

Mode	Matrix-Type	Memory Location Limit Value			Note (Matrix)
		Display Data	Fade Data	LED On/Off Control	
Binary	Type1	1Dh	No support function	No support function	9×10 + 9×10
	Type2	11h	No support function	No support function	12×12
	Type3	1Fh	No support function	No support function	16×16
Gray	Type1	B3h	9Fh	1Dh	9×10 + 9×10
	Type2	BBh	B5h	11h	12×12
	Type3	FFh	7Fh	1Fh	16×16

Read Register Status

In this mode, the master reads the device data after setting the slave address. Following the R/W bit (= "0"), and the acknowledge bit, then follows the Read Register Status command code. Next is the START condition and slave address, followed by an R/W bit (= "1"). The addressed data is then transmitted.

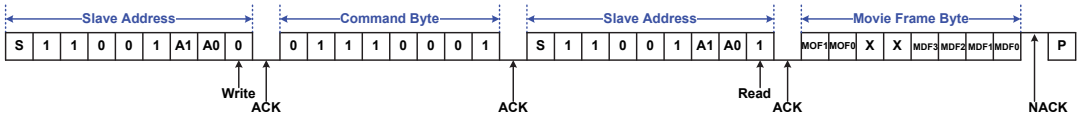


Note: 1. If register location exceeds limit value, the register pointer will return to 1st. The register location limit value is 17th address.

2. This cycle to read consecutive addresses will continue until the master sends a NACK and STOP condition.

Read Movie Frame Status

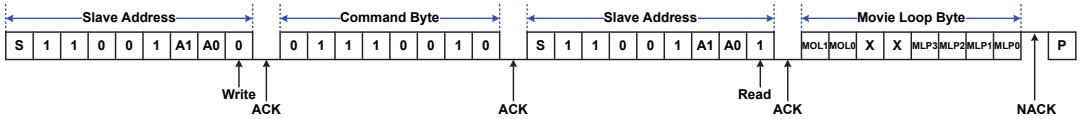
In this mode, the master reads the device data after setting the slave address. Following the R/W bit (= "0"), and the acknowledge bit, then follows the Read Movie Frame Status command code. Next is the START condition and slave address, followed by an R/W bit (= "1"). The addressed data is then transmitted.



Note: This cycle to read consecutive addresses will continue until the master sends a NACK and STOP condition.

Read Movie Loop Status

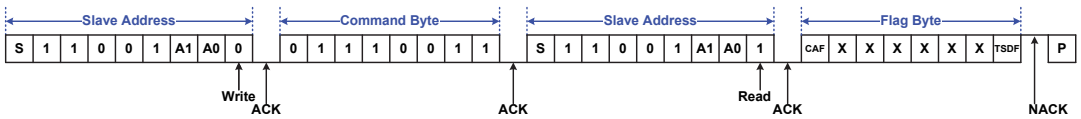
In this mode, the master reads the device data after setting the slave address. Following the R/W bit (= "0"), and the acknowledge bit, then follows the Read Movie Loop Status command code. Next is the START condition and slave address, followed by an R/W bit (= "1"). The addressed data is then transmitted.



Note: This cycle to read consecutive addresses will continue until the master sends a NACK and STOP condition.

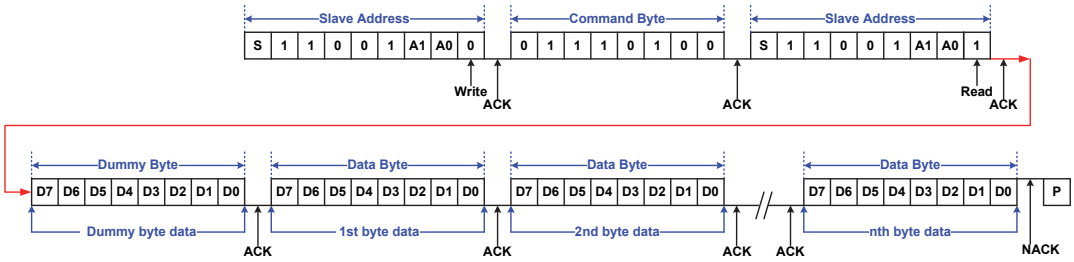
Read Function Flag Status

In this mode, the master reads the device data after setting the slave address. Following the R/W bit (="0"), and the acknowledge bit, then follows the Read Function Flag command code. Next is the START condition and slave address, followed by an R/W bit (="1"). The addressed data is then transmitted.



Note: This cycle to read consecutive addresses will continue until the master sends a NACK and STOP condition.

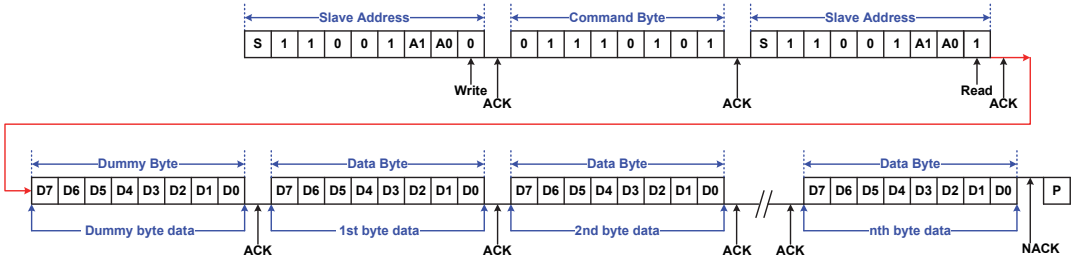
Read Open Detection Data



Note: 1. The display data must be read in byte units.

2. Matrix type3 (16×16): If register location exceeds limit value, the register pointer will return to 1st. The register location limit value is 32nd.

Read Short Detection Data



Note: 1. The display data must be read in byte units.

2. Matrix type3 (16×16): If register location exceeds the limit value, the register pointer will return to 1st. The register location limit value is 32nd.

Power Supply Sequence

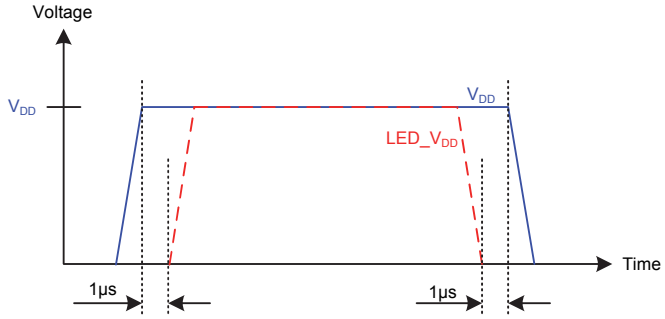
If the power is individually supplied on the LED_VDD and VDD pins, it is strongly recommended to follow the Holtek power supply sequence requirement.

If the power supply sequence requirement is not followed, it may result in malfunctions.

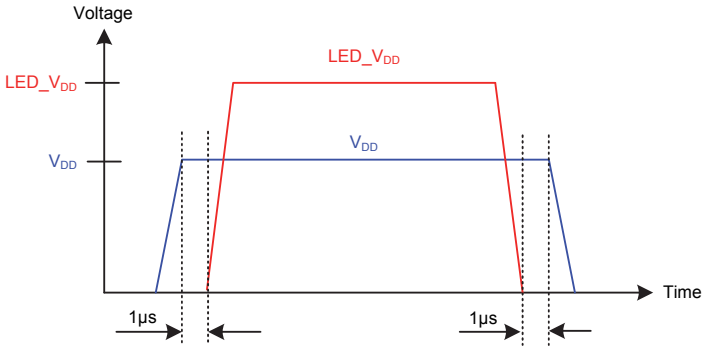
Holtek Power Supply Sequence Requirement

1. Power-on sequence:
   Turn on the logic power supply V_{DD} first and then turn on the LED driver power supply LED_V_{DD}.
2. Power-off sequence:
   Turn off the LED driver power supply LED_V_{DD} first and then turn off the logic power supply V_{DD}.
3. The Holtek Power Supply Sequence Requirement must be followed no matter whether the LED_V_{DD} voltage is higher than the V_{DD} voltage or not.

- When the LED_V_{DD} voltage is equal to V_{DD} voltage application:



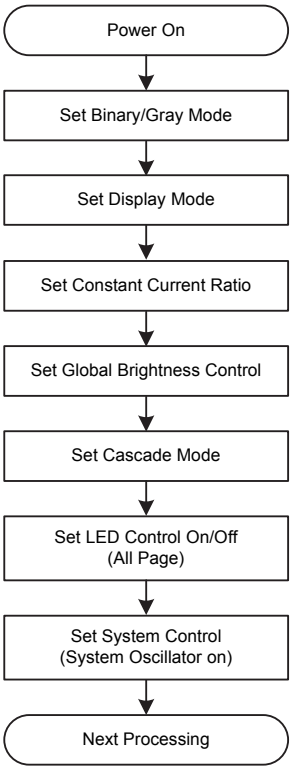
- When the LED_V_{DD} voltage is greater than the V_{DD} voltage application



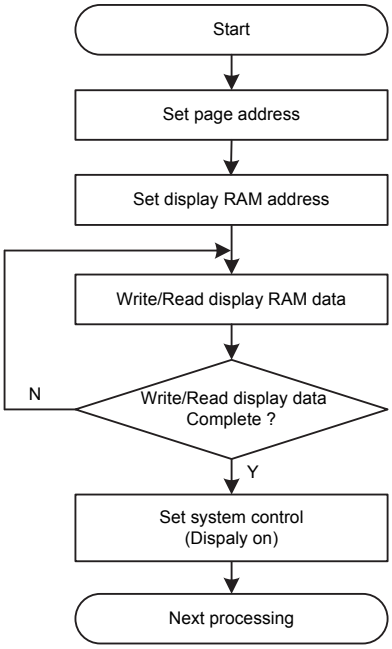
Operation Flow Charts

Access procedures are illustrated below by means of flowcharts.

• Initialisation



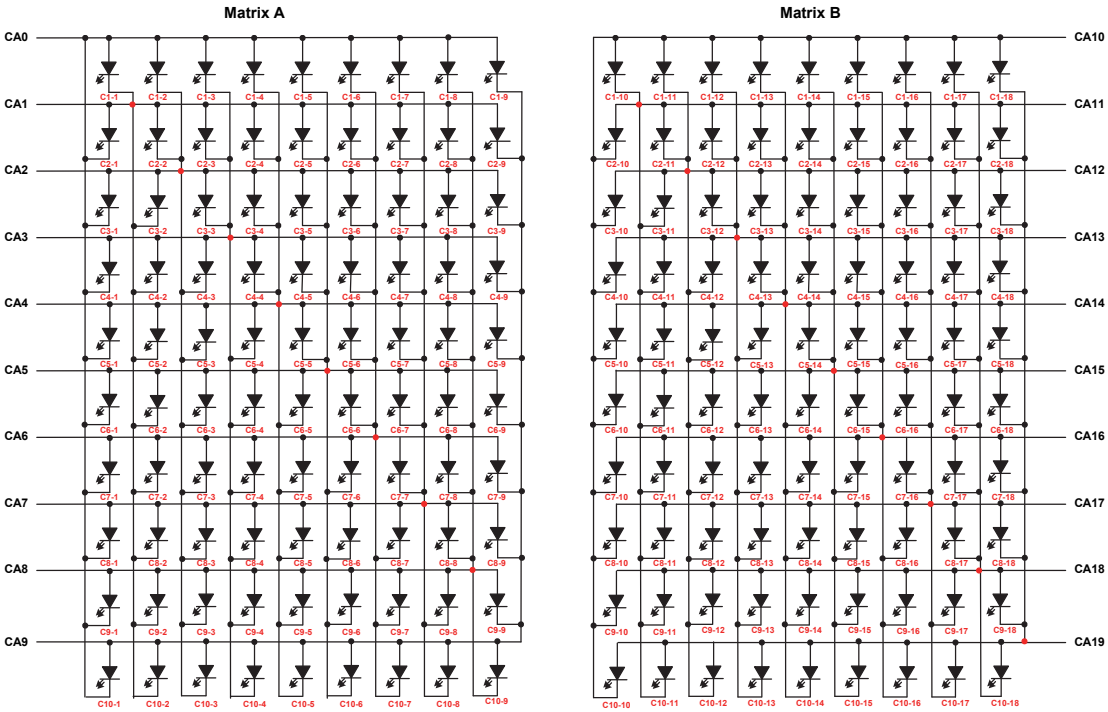
• Display Data Read/Write – Address Setting



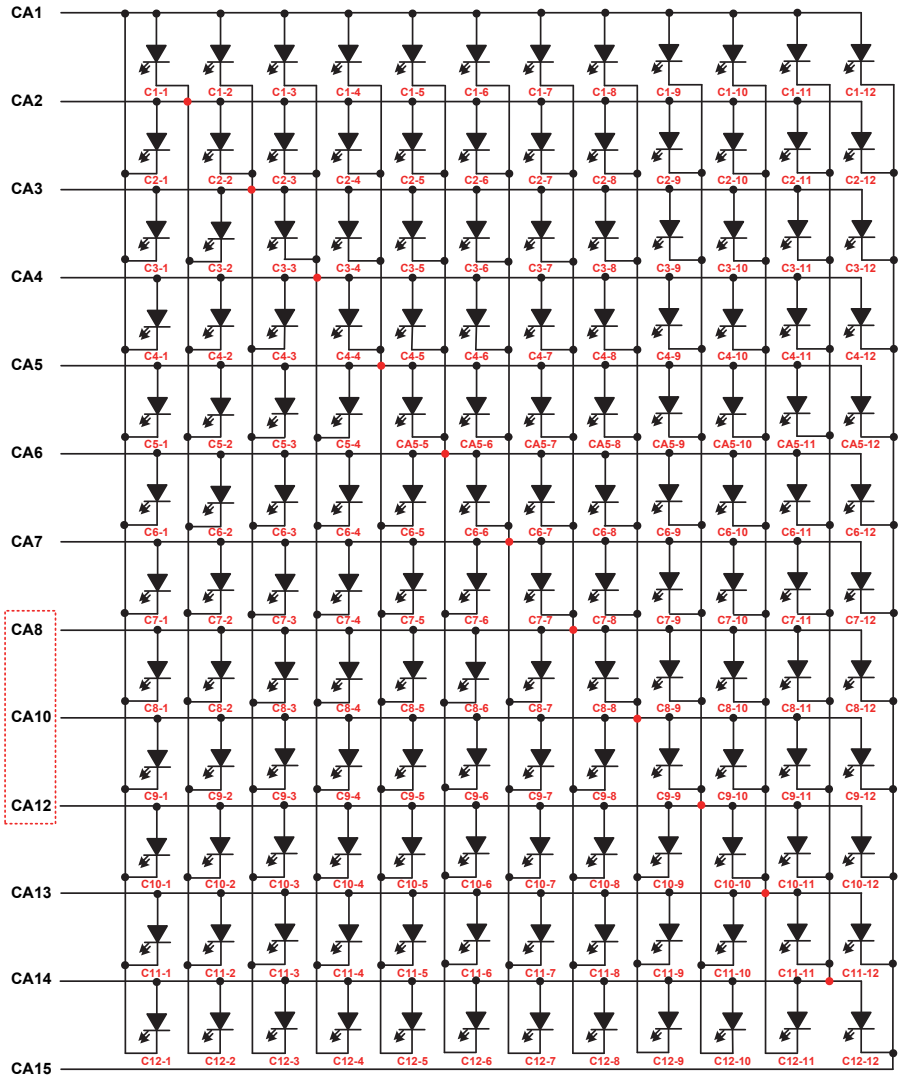
Application Circuits

LED Matrix Circuit

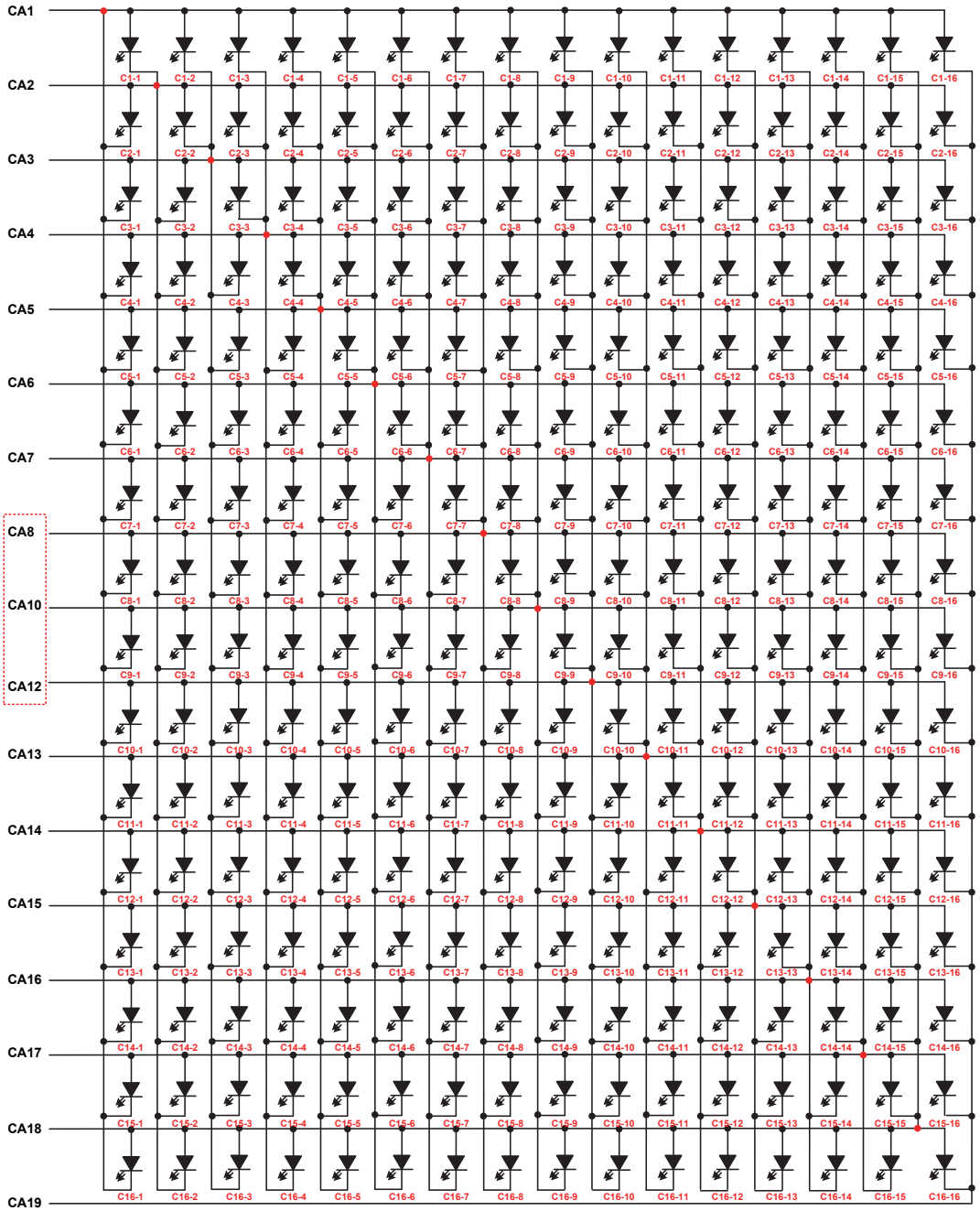
Matrix-type1: 9×10 + 9×10



Matrix-type2: 12×12

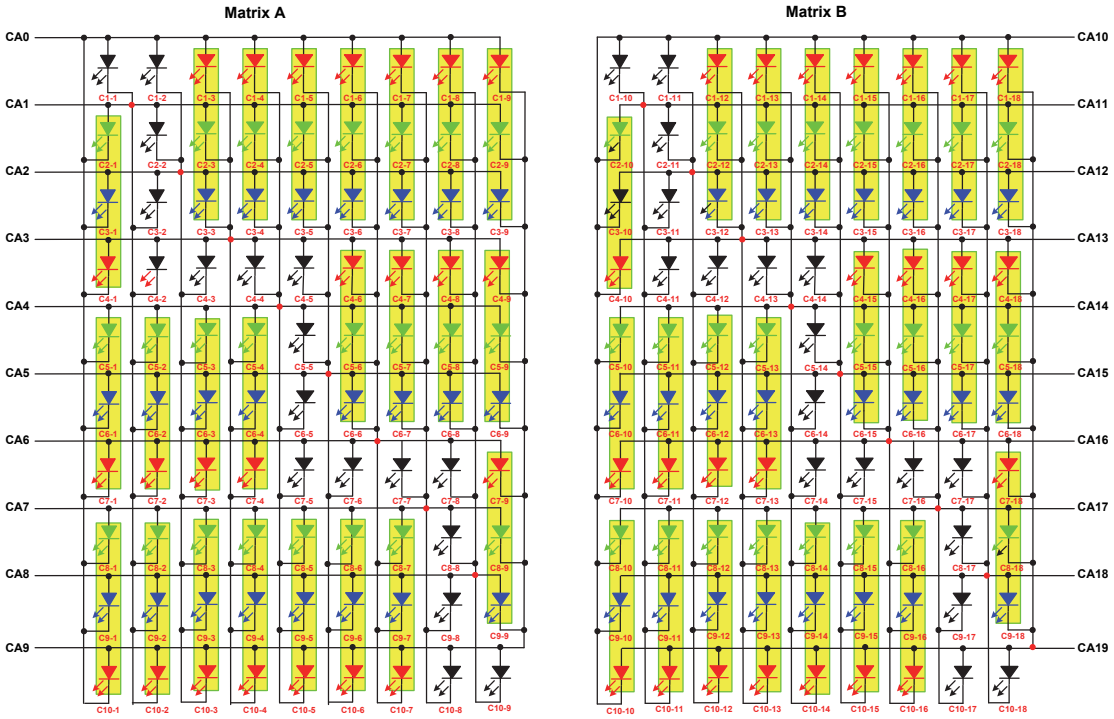


Matrix-type3: 16×16

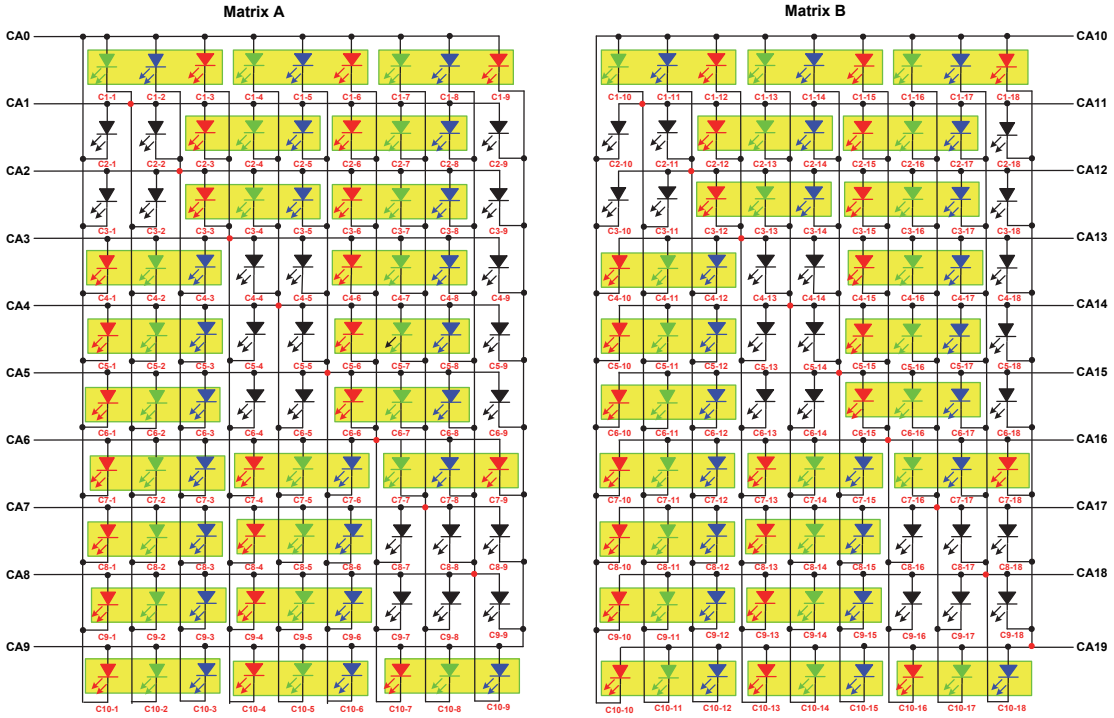


RGB LED Matrix Circuit

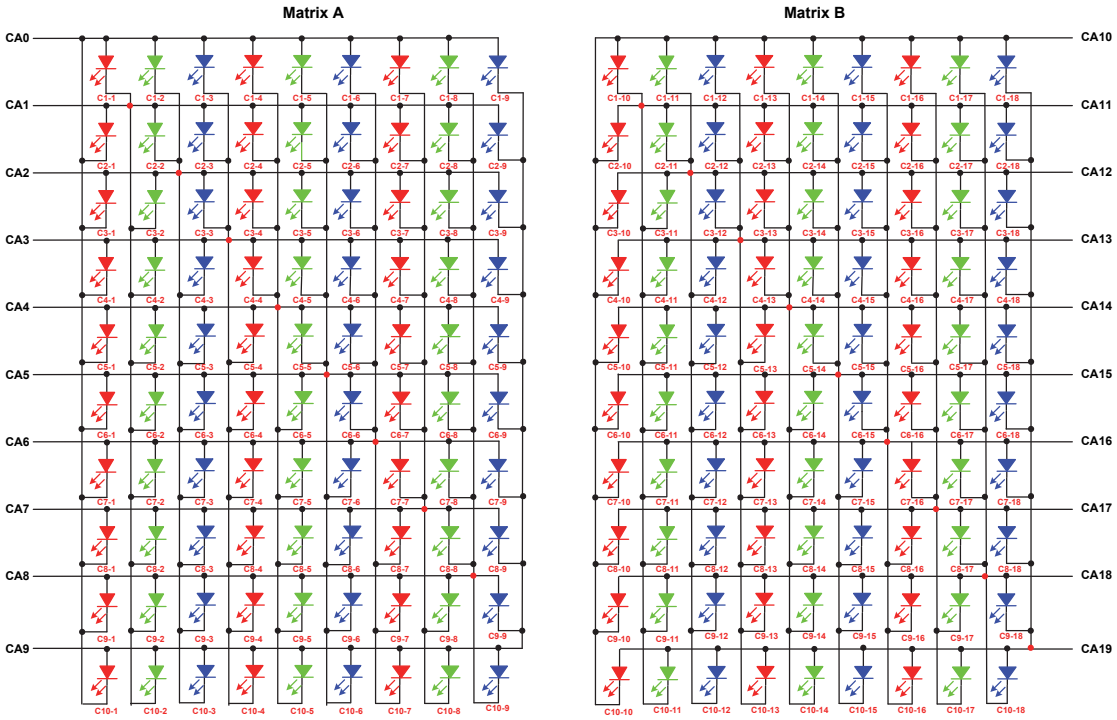
Matrix-type1: 9×10 + 9×10



Common Cathode RGBs Connection

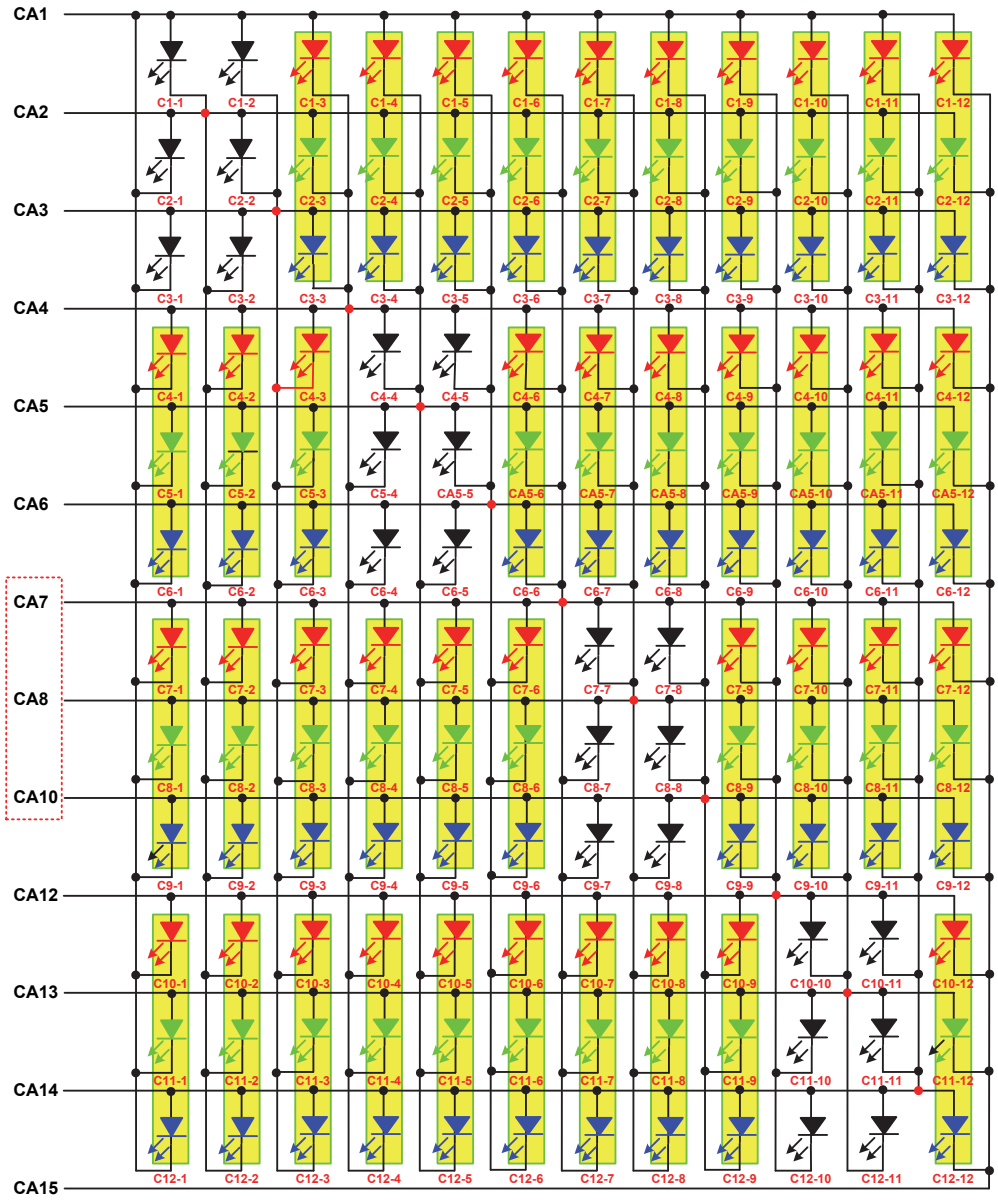


Common Anode RGBs Connection

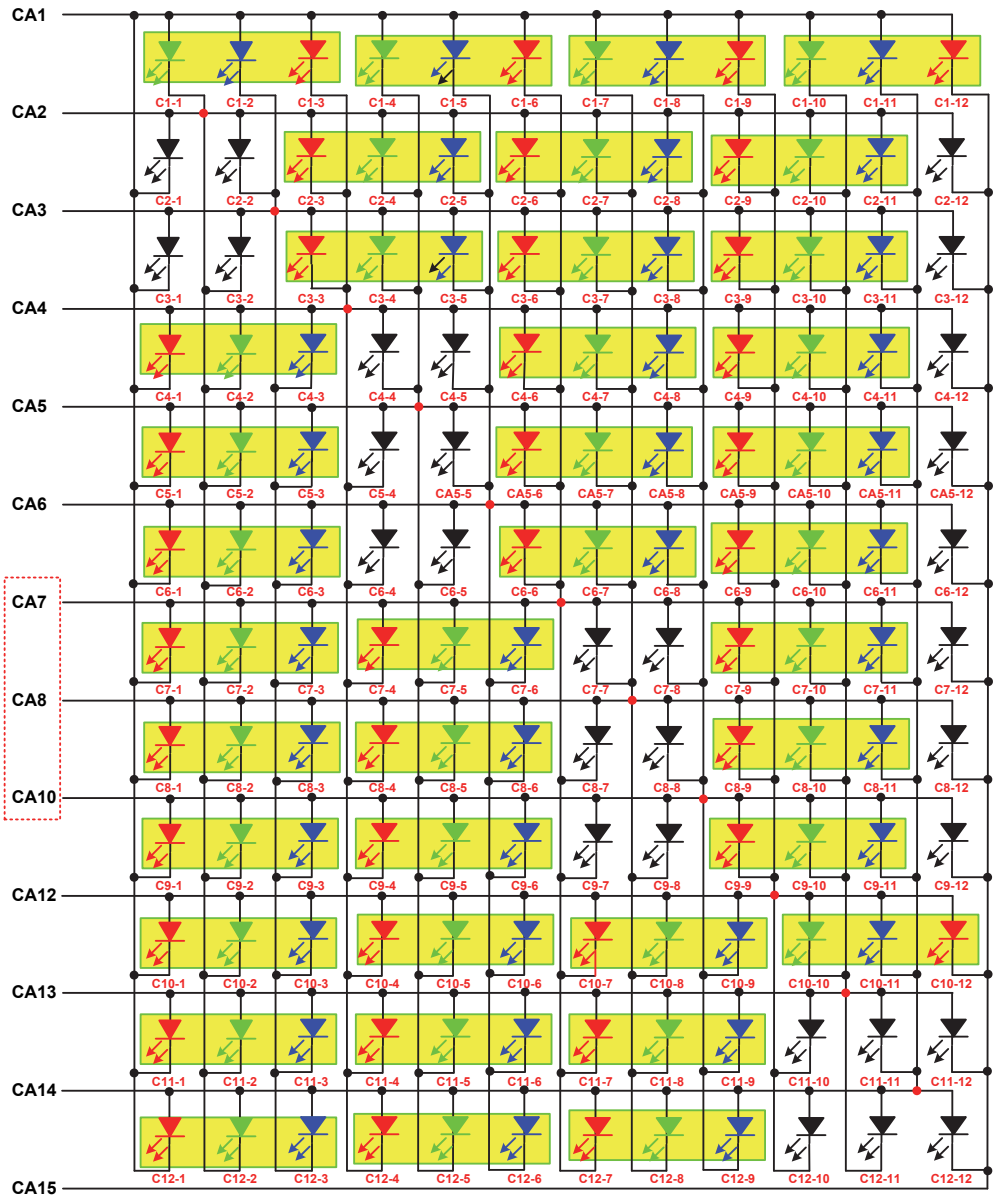


Respective RGBs Connection

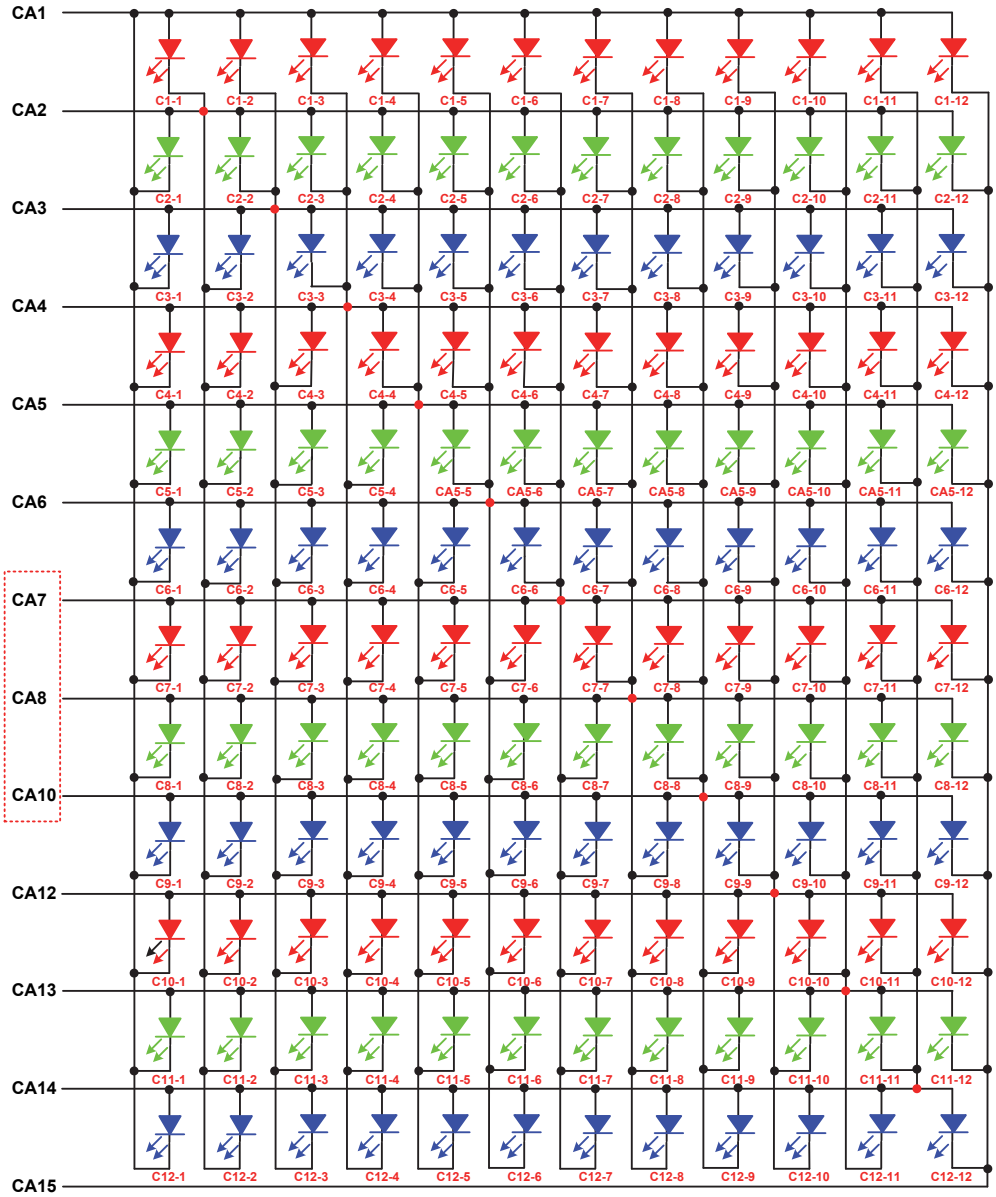
Matrix-type2: 12×12



Common Cathode RGBs Connection

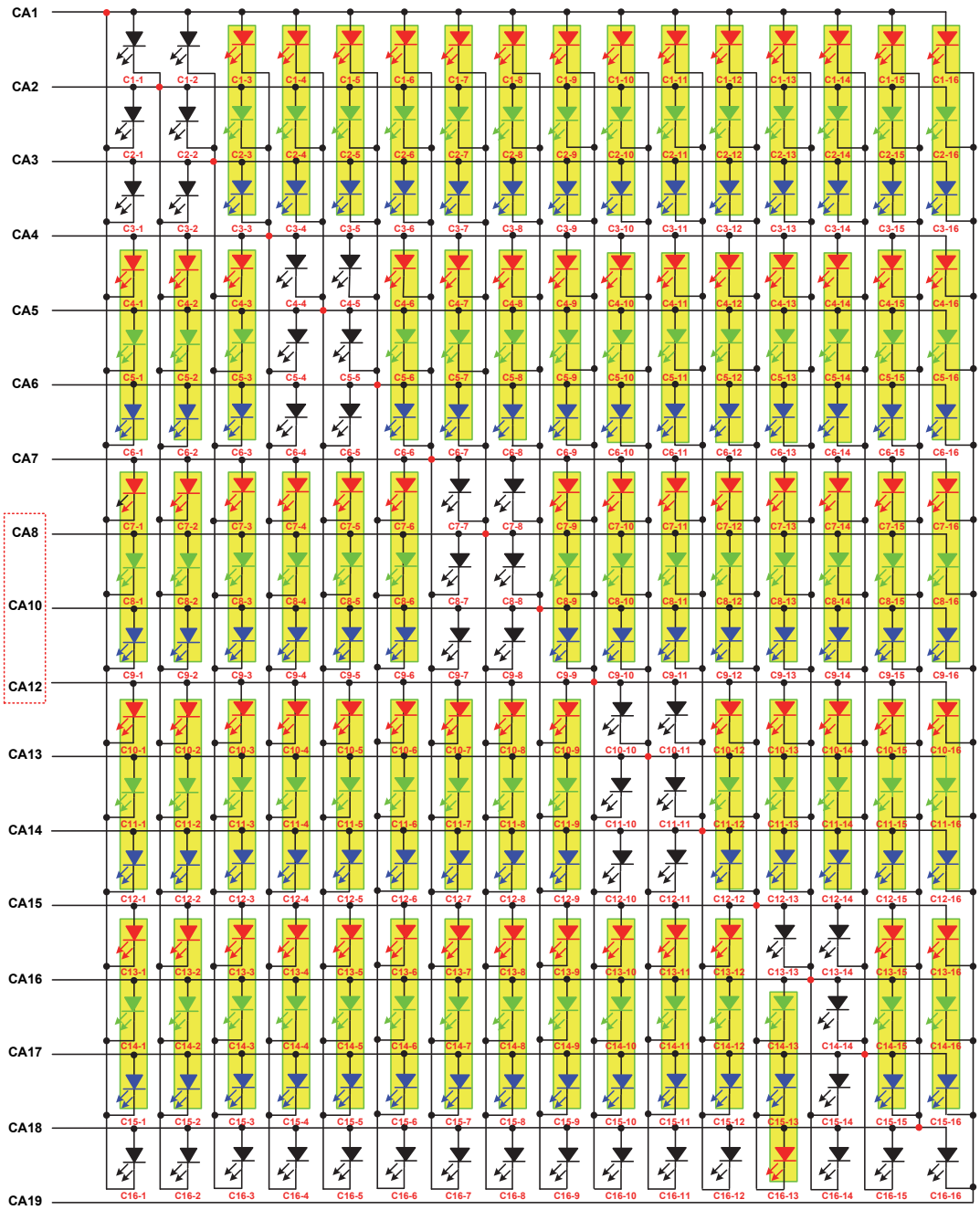


Common Anode RGBs Connection

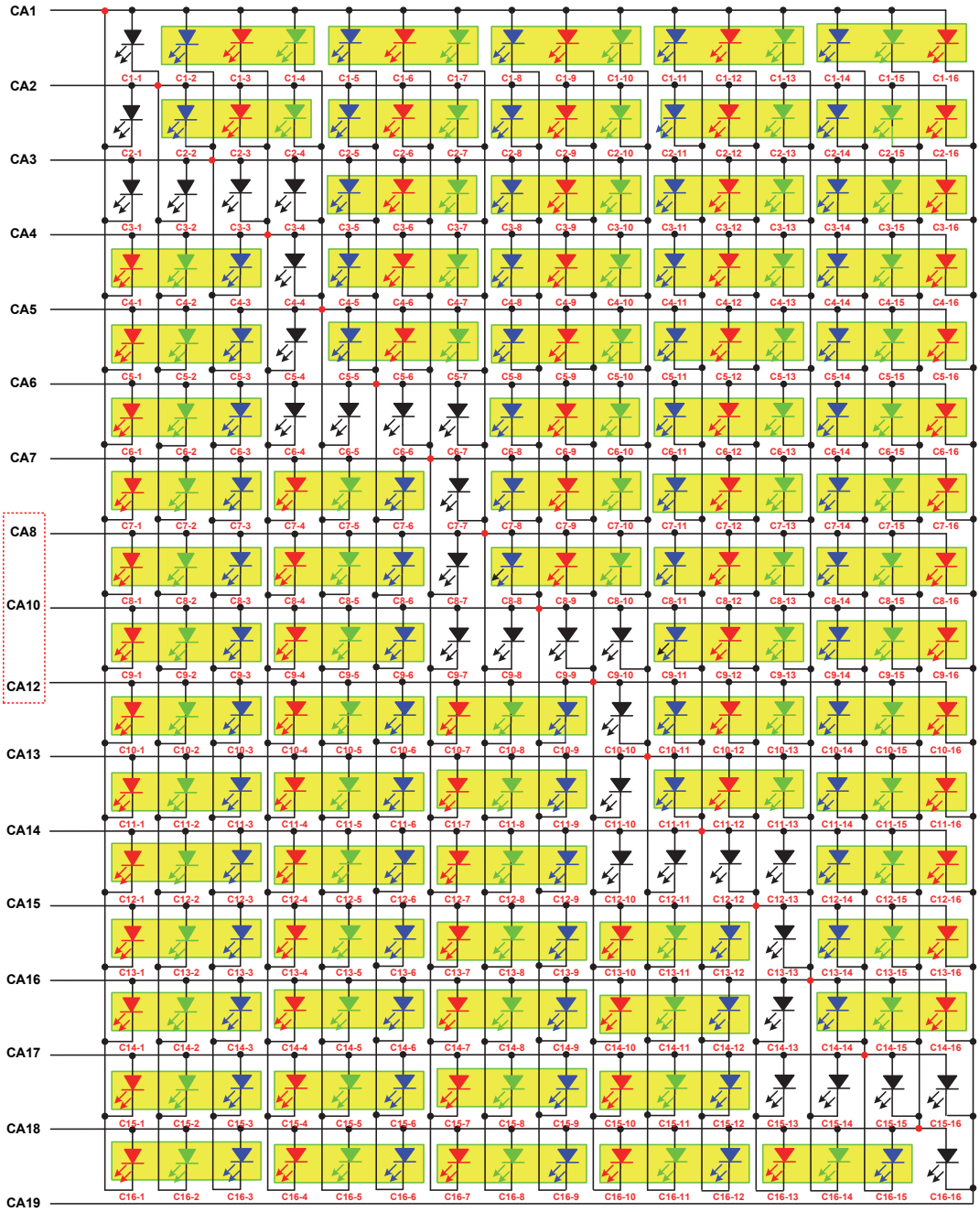


Respective RGBs Connection

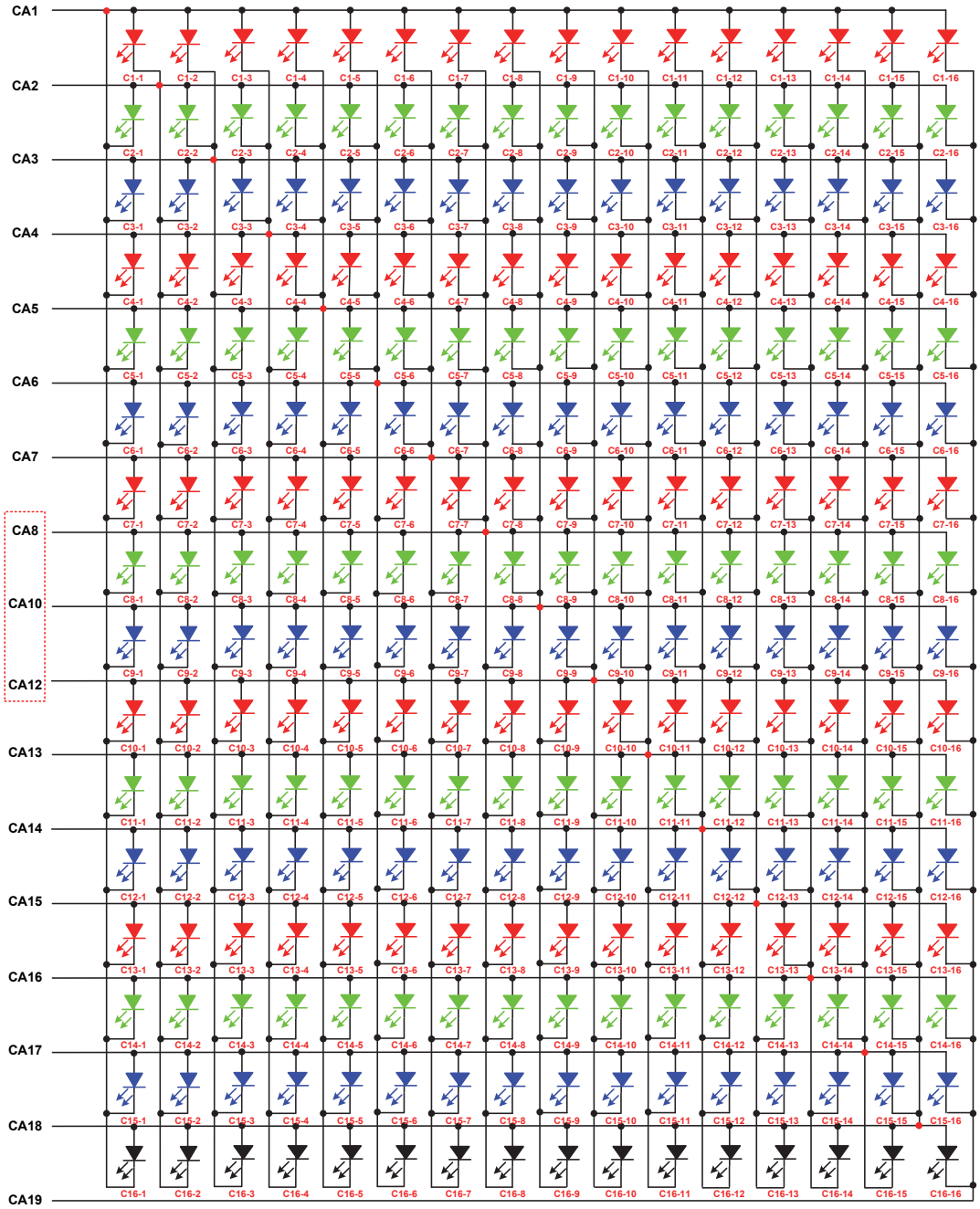
Matrix-type3: 16×16



Common Cathode RGBs Connection

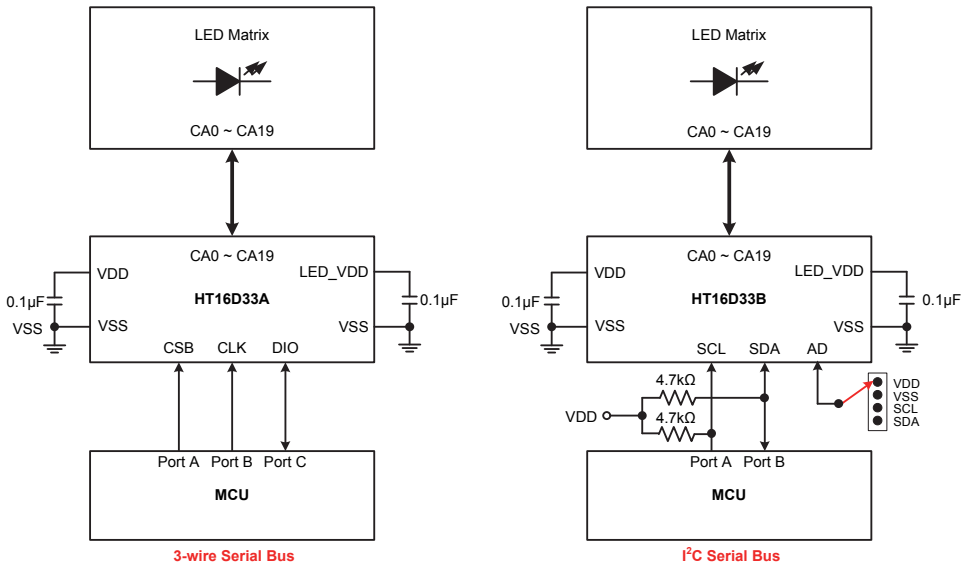


Common Anode RGBs Connection



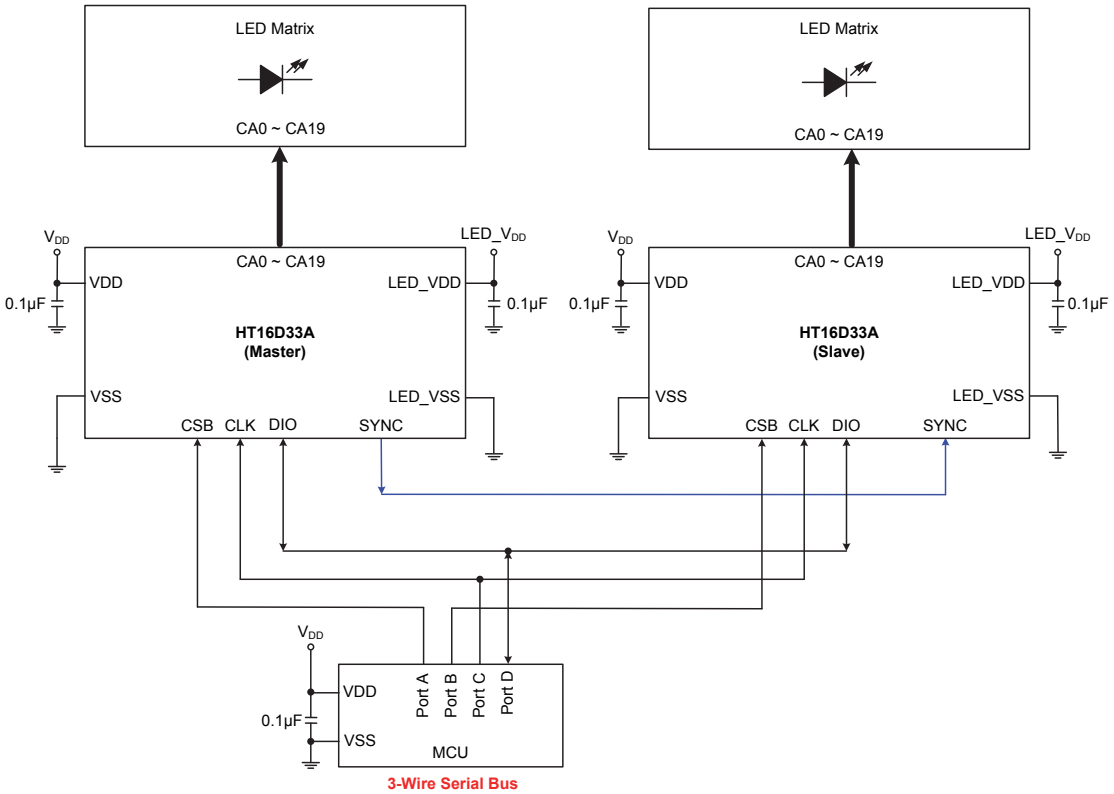
Respective RGBs Connection

Single LED IC Application



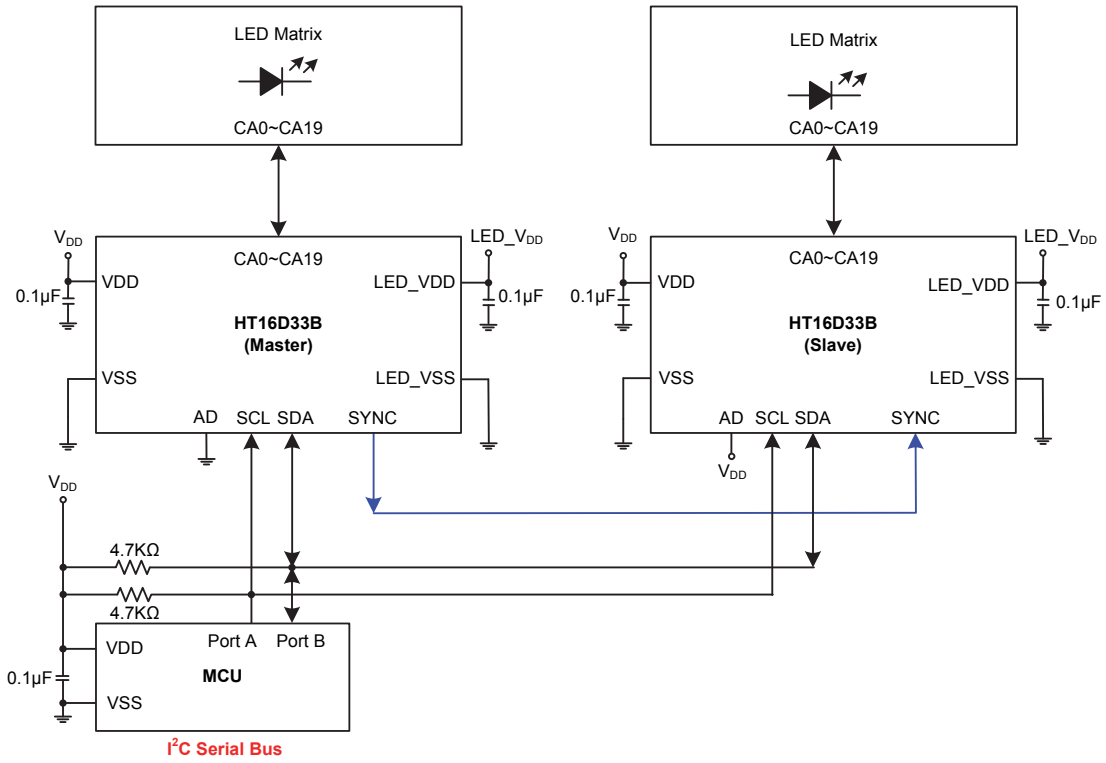
Cascade Function

LED Application Example – SPI 3-wire Serial Bus



Note: Cascading can also be implemented using software. Users must set the Master in the master mode and the Slave in the slave mode using commands. The CSB pin must be connected to the MCU individually for independent read and write.

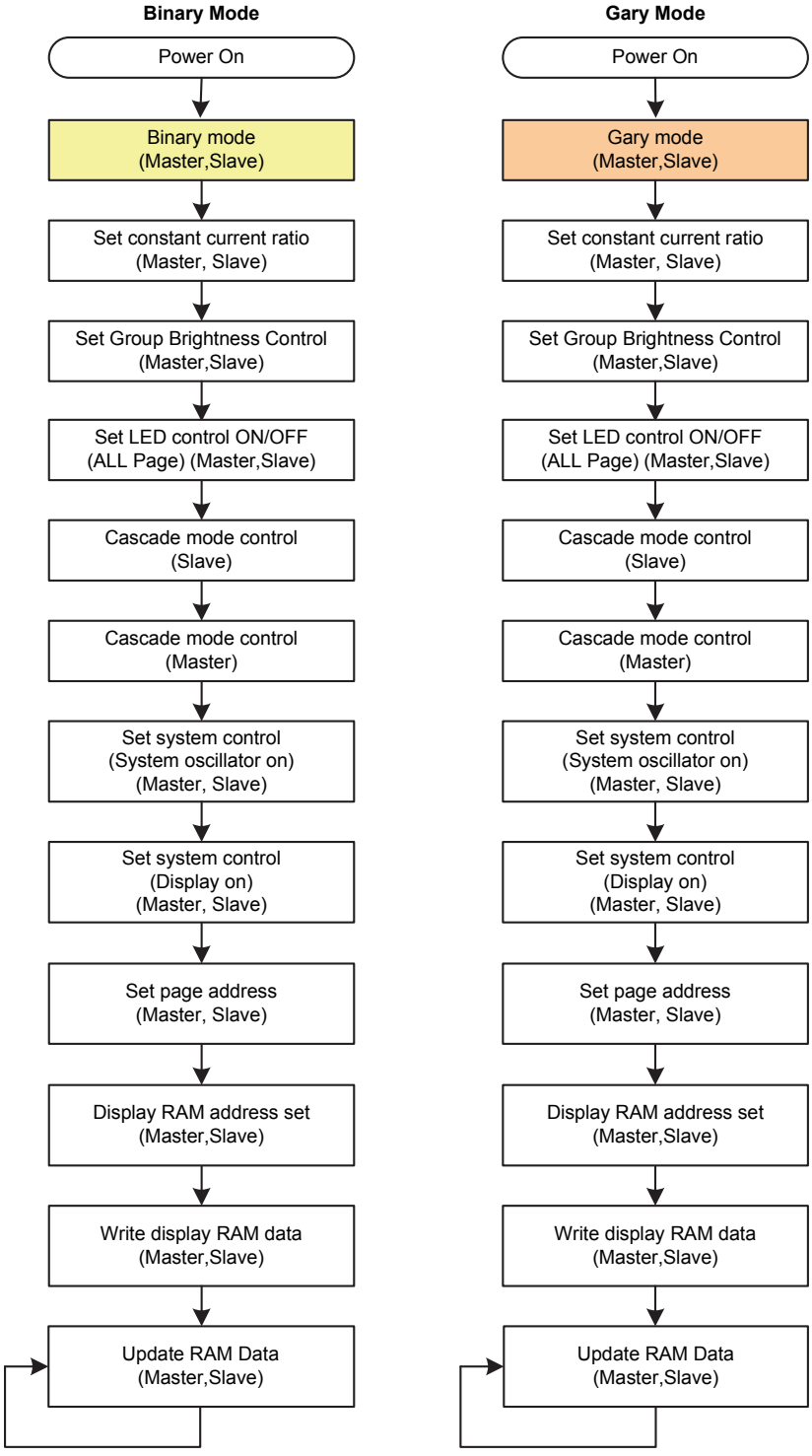
LED Application Example – I²C Serial Bus



Note: Cascading can also be implemented using software. Users must set the Master in the master mode and the Slave in the slave mode using commands. The CSB pin must be connected to the MCU individually for independent read and write.

Cascade Control Flow

Access procedures are illustrated below using flowcharts.



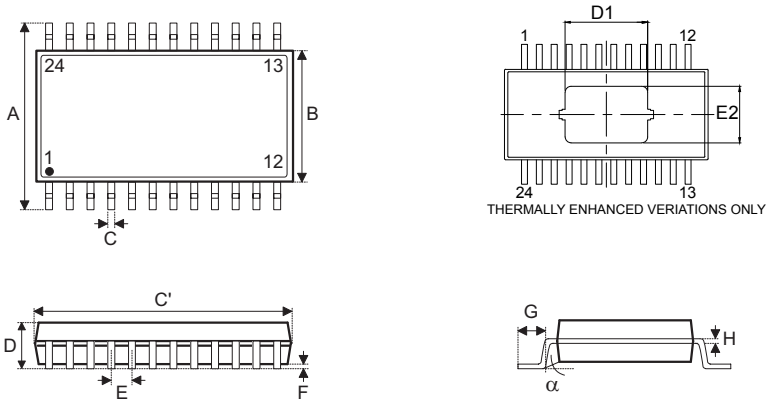
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

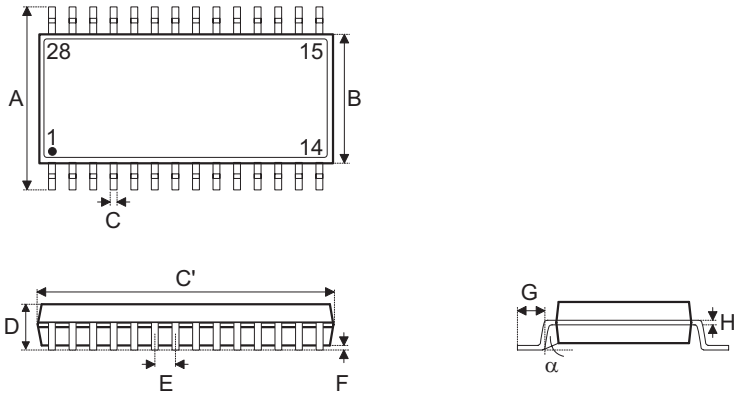
24-pin SSOP-EP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.008	—	0.012
C’	—	0.341 BSC	—
D	—	—	0.069
D1	—	0.140	—
E	—	0.025 BSC	—
E2	—	0.096	—
F	0.000	—	0.004
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions mm		
	Min.	Nom.	Max.
A	—	6.00 BSC	—
B	—	3.90 BSC	—
C	0.20	—	0.30
C’	—	8.66 BSC	—
D	—	—	1.75
D1	—	3.56	—
E	—	0.635 BSC	—
E2	—	2.44	—
F	0.00	—	0.10
G	0.41	—	1.27
H	0.10	—	0.25
α	0°	—	8°

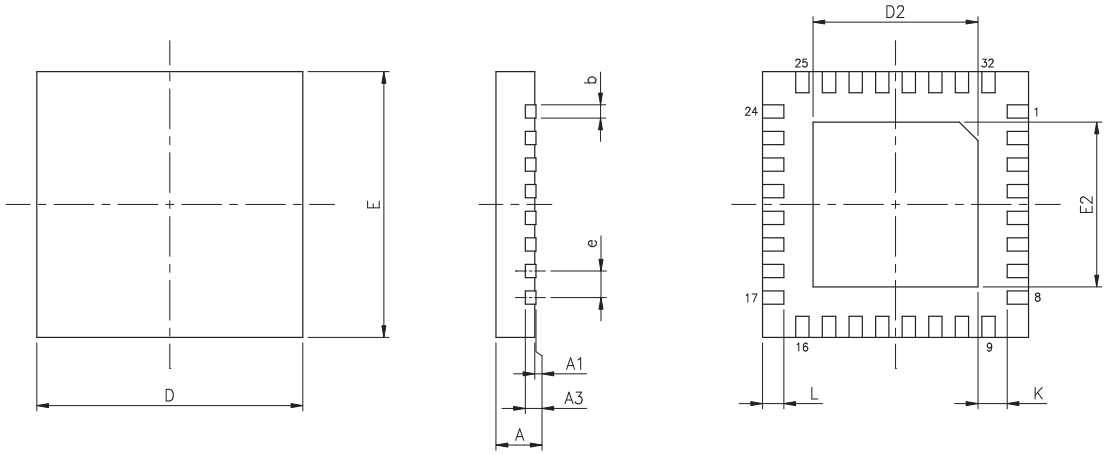
28-pin SSOP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.008	—	0.012
C’	—	0.390 BSC	—
D	—	—	0.069
E	—	0.025 BSC	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.0 BSC	—
B	—	3.9 BSC	—
C	0.20	—	0.30
C’	—	9.9 BSC	—
D	—	—	1.75
E	—	0.635 BSC	—
F	0.10	—	0.25
G	0.41	—	1.27
H	0.10	—	0.25
α	0°	—	8°

SAW Type 32-pin QFN (4mm×4mm×0.75mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.006	0.008	0.010
D	—	0.157 BSC	—
E	—	0.157 BSC	—
e	—	0.016 BSC	—
D2	0.104	0.106	0.108
E2	0.104	0.106	0.108
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A3	—	0.203 BSC	—
b	0.150	0.200	0.250
D	—	4.000 BSC	—
E	—	4.000 BSC	—
e	—	0.400 BSC	—
D2	2.650	2.700	2.750
E2	2.650	2.700	2.750
L	0.350	0.400	0.450
K	0.200	—	—

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