HOLTEK

8×9 Constant Current LED Driver

HT16D31A/HT16D31B

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Features

- Logic Operating Voltage: 2.7V~5.5V
- LED Driver Operating Voltage: 4.5V~5.5V
- LED Display: 9 combinations of output pins (CA0~CA8), 8 rows and 9 commons LED Matrix
- LED Data RAM1(Max.): 8 × 9 × 8 × (2) bits = (144) × 8 bits for Gray mode
- LED Data RAM2(Max.): 8 × 9 × 4 × (2) bits = (72) × 8 bits for Fade mode
- LED Data RAM3(Max.): 1 × 9 × 8 × (2) bits = (18) × 8 bits for LED On/Off Control
- Integrated 2.4MHz RC oscillator
- 2 frame memory for animations
- 256-level global brightness scale
- Binary scale mode or Gray scale mode
- Global blinking or fade function
- Automatic scroll function: left/right
- Internal Current Reference Control
- Support max. 48mA Sink Constant Current
- 16-level Maximum current setup selection
- Current matching to ±3%
- Over temperature protection circuit
- Open/short protection circuit for each dot
- I^2C-bus or SPI 3-wire Interface
- Cascade function for extend applications
- Package Types: 16-pin NSOP-EP/QFN

Applications

- Industrial control displays
- Mobile phones
- Traffic signboards and information displays
- Digital clocks, thermometers, counters, electronic meters
- Instrumentation readouts
- Other consumer applications
- LED displays

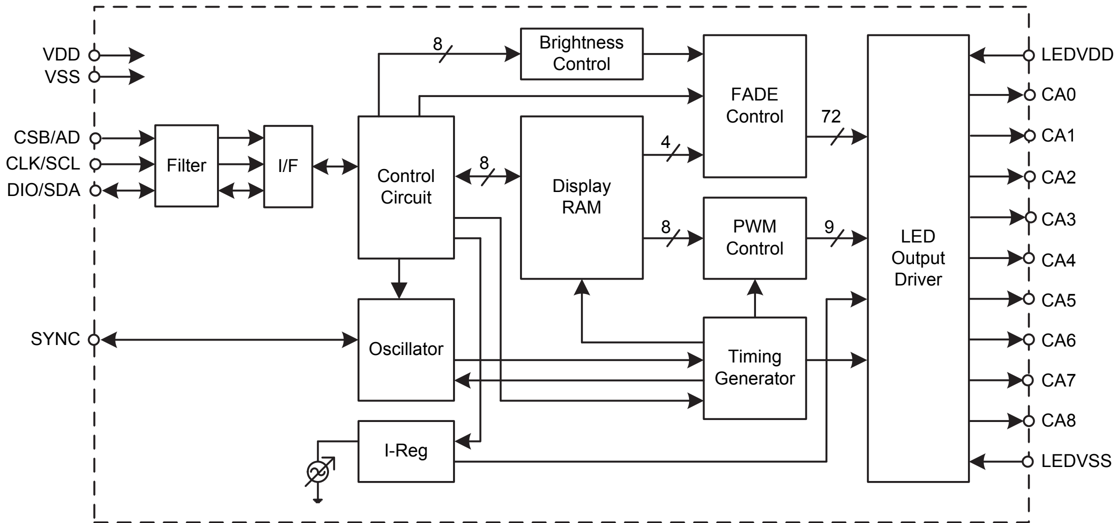
General Description

The HT16D31A and HT16D31B are high accuracy constant current and memory mapping LED display controller/drivers. The maximum display capacity of the devices is 72 patterns composed of 8 rows and 9 commons. The devices can generate a 256 step Gray Scale (PWM data) using software controlled PWM circuitry and 256 LED illumination levels using software controlled PWM circuitry. The devices provide constant current output control using software controlled for each row output terminal. A serial interface is provided to allow the devices to receive instructions for its command mode and data mode. Only three lines are required for device interfacing to a host controller. The display capacity can be easily extended by cascading the devices thus expanding its application possibilities. The devices are compatible with most microcontrollers offering easy interfacing via their two serial interfaces, an I^2C interface or an SPI 3-wire serial interface.

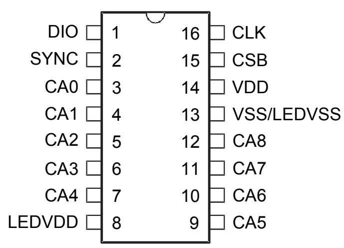
Selection Table

Part Number	Interface
HT16D31A	3-wire SPI
HT16D31B	I^{2}C

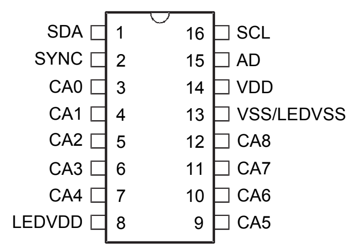
Block Diagram



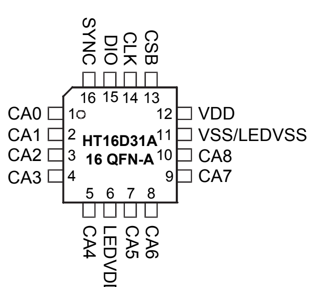
Pin Assignment

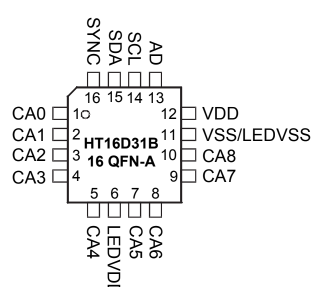


HT16D31A
16 NSOP-EP-A



HT16D31B
16 NSOP-EP-A

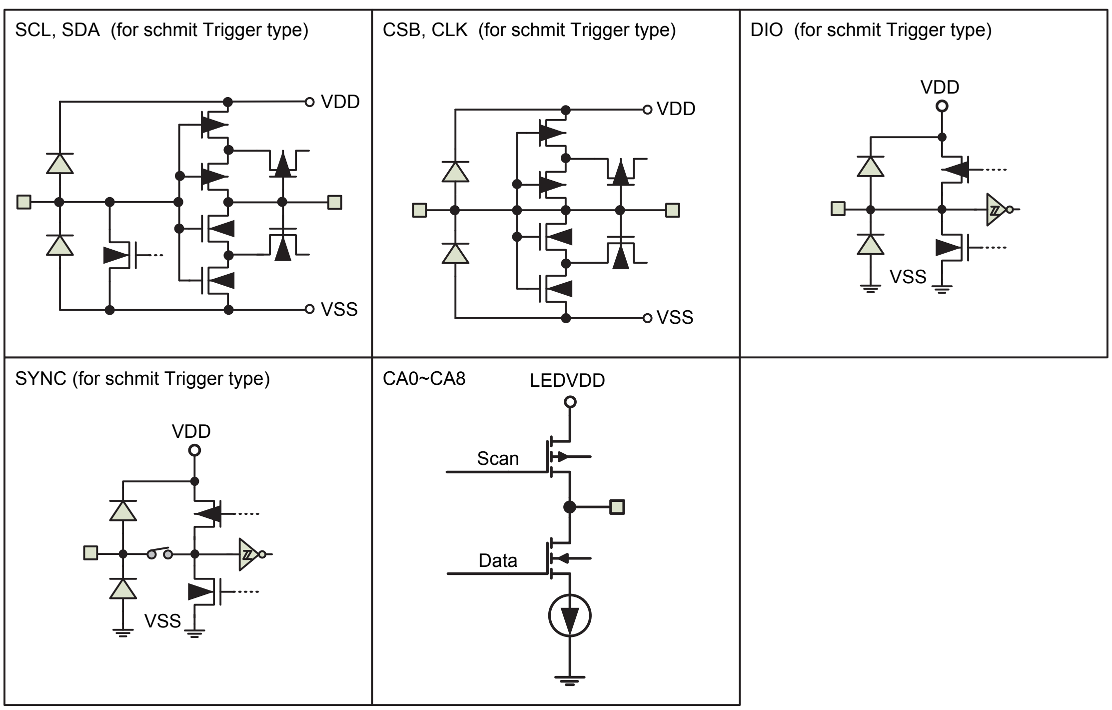




Pin Description

Pin Name	Type	Function
VDD	—	Positive power supply for logic circuits
VSS	—	Negative power supply for logic circuits, ground
LEDVDD	—	Positive power supply for driver circuit
LEDVSS	—	Negative power supply for driver circuit, ground
CSB/AD	I	I^{2}C interface device address data set input pin for I^{2}C interface Chip Select pin for SPI 3-wire Interface
CLK/SCL	I	Serial clock input pin Serial Clock (SCL) Input for I^{2}C interface Serial Clock (CLK) Input for SPI 3-wire Interface
DIO/SDA	I/O	Serial data input/output pin. Data is input to or comes out from the shift register at the clock rising edge. I^{2}C interface serial data (SDA) Input/Output – NMOS open-drain output SPI 3-wire serial interface serial data input/output – CMOS output
SYNC	I/O	Synchronization clock Input / output pin If the Master Mode command is programmed, the system clock is output on the SYNC pin. If the Slave Mode command is programmed, the system clock is input on the SYNC pin.
CA0~CA8	I/O	LED combinations of output pins. (Rows and Commons combo pins)

Approximate Internal Connections



Absolute Maximum Ratings

Supply Voltage .... V_{SS}-0.3V to V_{SS}+6.0V

Input Voltage .... V_{SS}-0.3V to V_{DD}+0.3V

Operating Temperature .... -40°C to 85°C

Storage Temperature .... -50°C to 125°C

Thermal Resistance (Rth) (16-pin QFN) .... 68°C/W

(16-pin NSOP-EP) .... 31°C/W

Max junction Temperature (Tj) .... 125°C

Power Dissipation (PD) (Ta=25°C) (16-pin QFN) 1.47W

(Ta=85°C) (16-pin QFN) 0.58W

(Ta=85°C) (16-pin NSOP-EP) 3.23W

(Ta=85°C) (16-pin NSOP-EP) 1.29W

CAn Output Current (Single pin) 100mA

Total Power Line Current (Ta=25°C) 1000mA

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

V_{DD}=5V, LED_V_{DD}=5V, Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Logic Supply Voltage	—	—	2.7	—	5.5	V
LED_V_{DD}	LED Supply Voltage	—	—	4.5	—	5.5	V
I_{STB}	Standby Current	5V	No load, Power down mode (System OSC off, LED display off)	—	1.0	2.0	μA
I_{DD}	Operating Current	5V	No load, LED on, Constant current ratio=33mA Internal RC OSC, Output all on	—	4.5	7.0	mA
I_{LED_VDD}	Operating Current	5V	No load, LED On, Constant current ratio=33mA Internal RC OSC, Output all on	—	2.1	3.5	mA
V_{IH}	Input High Voltage	5V	DIO, CLK, SDA, SCL, CSB, SYNC	0.7V_{DD}	—	5.0	V
V_{IL}	Input Low Voltage	5V	DIO, CLK, SDA, SCL, CSB, SYNC	0	—	0.3V_{DD}	V
I_{OH}	High Level Output Current	5V	V_{OH}=4.5V, SYNC, DIO	-10	-13	—	mA
I_{OL}	Low Level Output Current	5V	V_{OL}=0.5V, SYNC, DIO, SDA	18	25	—	mA
I_{CA_OH}	CAn Source Current	5V	Constant current ratio=33mA, V_{OH}=4.5V	270	330	—	mA
I_{CA_OL}	CAn Constant Current	5V	Constant current ratio=33mA, V_{DS}=0.7V~2V	—	33	—	mA
dI_{CA1} (1)	Bit Current Skew	5V	Constant current ratio=33mA, V_{DS}=1V	—	±3.0	±5.0	%
dI_{CA2} (2)	Channel Current Skew	5V	Constant current ratio=33mA, V_{DS}=1V	—	±3.0	±5.0	%
%/dV_{DS} (3)	Output Current vs. Output Voltage Regulation	5V	Constant current ratio=33mA, V_{DS} =0.7V~2.0V, V_{DD}=5.0V	—	±0.3	±0.5	%/V
%/dV_{DD} (4)	Output Current vs. Supply Voltage Regulation	—	Constant current ratio set=33mA, V_{DD}=4.5V~5.5V, V_{DS}=1.0V	—	—	±1.0	%/V

Note: 1. Bit Skew:

$$\text{Pin } dI_{CA1}(\%) = \frac{I_{CA\_(n+1)}(V_{DS}=1V) - I_{CA\_n}(V_{DS}=1V)}{I_{CA\_(n+1)}(V_{DS}=1V) + I_{CA\_n}(V_{DS}=1V)/2} \times 100\% \quad \text{(n: CA pin number)}$$

2. Channel Skew:

$$+dI_{CA2}(\%) = \frac{I_{CA\_MAX} - I_{CA\_AVG}}{I_{CA\_AVG}} \times 100\% \quad \text{(n: CA pin number)}$$

$$-dI_{CA2}(\%) = \frac{I_{CA\_MIN} - I_{CA\_AVG}}{I_{CA\_AVG}} \times 100\% \quad \text{(n: CA pin number)}$$

Where:

I_{CA_AVG}: the average I_{CA} for all CA pins on V_{DS}=1V

I_{CA_MAX}: the max I_{CA} of all CA pins on V_{DS}=1.0V

I_{CA_MIN}: the min I_{CA} of all CA pins on V_{DS}=1.0V

3. $$\%/dV_{DS}(\%/V) = \frac{I_{CA\_MAX} - I_{CA\_MIN}}{(2.0V - 0.7V) \times I_{CA\_AVG}} \times 100\%$$

Where:

I_{CA_AVG}: the average I_{CA} for each CA pins between V_{DS}=0.7V and 2.0V
I_{CA_MAX}: the max I_{CA} of each CA pins between V_{DS}=0.7V and 2.0V
I_{CA_MIN}: the min I_{CA} of each CA pins between V_{DS}=0.7V and 2.0V

4. $$\%/dV_{DD}(\%/V) = \frac{I_{CA\_MAX} - I_{CA\_MIN}}{(5.5V - 4.5V) \times I_{CA\_AVG}} \times 100\%$$

Where:

I_{CA_AVG} : the average I_{CA} for each CA pins between V_{DD}=4.5V and 5.5V

I_{CA_MAX}: the max I_{CA} of each CA pins between V_{DD}=4.5V and 5.5V

I_{CA_MIN}: the min I_{CA} of each CA pins between V_{DD}=4.5V and 5.5V

V_{DS}=1V

5. Application condition of power supply: $LED\_V_{DD} \geq V_{DD}$

A.C. Characteristics

V_{DD} = 2.7V~5.5V, Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS}	System Clock	—	On-chip RC oscillator	2.1	2.4	2.7	MHz
f_{LED}	LED Frame Rate	—	—	—	980	—	Hz
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	—	—	—	—	100	mV
RR_{VDD}	V_{DD} Rise Rate to Ensure Power-on Reset	—	—	0.05	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} Stay at V_{POR} to Ensure Power- on reset	—	—	10	—	—	ms

A.C. Characteristics – SPI 3-wire Serial Bus

V_{DD}=2.7V~5.5V, Ta=25°C

Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
		V_{DD}	Conditions					
t_{CLK}	Clock Cycle Time	—	—		250	—	—	ns
t_{CW}	Clock Pulse Width	—	—		100	—	—	ns
t_{DS}	Data Setup Time	—	—		50	—	—	ns
t_{HS}	Data Hold Time	—	—		50	—	—	ns
t_{CSW}	"H" CSB Pulse Width	—	—		100	—	—	ns
t_{CSL}	CSB Setup Time (CSB↓ – CLK↓)	—	—		50	—	—	ns
t_{CSH}	CS Hold Time (CLK↑ – CSB↑)	—	—		4	—	—	μs
t_{PD}	Data Output Delay Time (CLK – DIO)	—	C_O=15pF	t_{PD}=10 to 90% t_{PD}=10 to 10%	—	—	350	ns

A.C. Characteristics – I²C Serial Bus

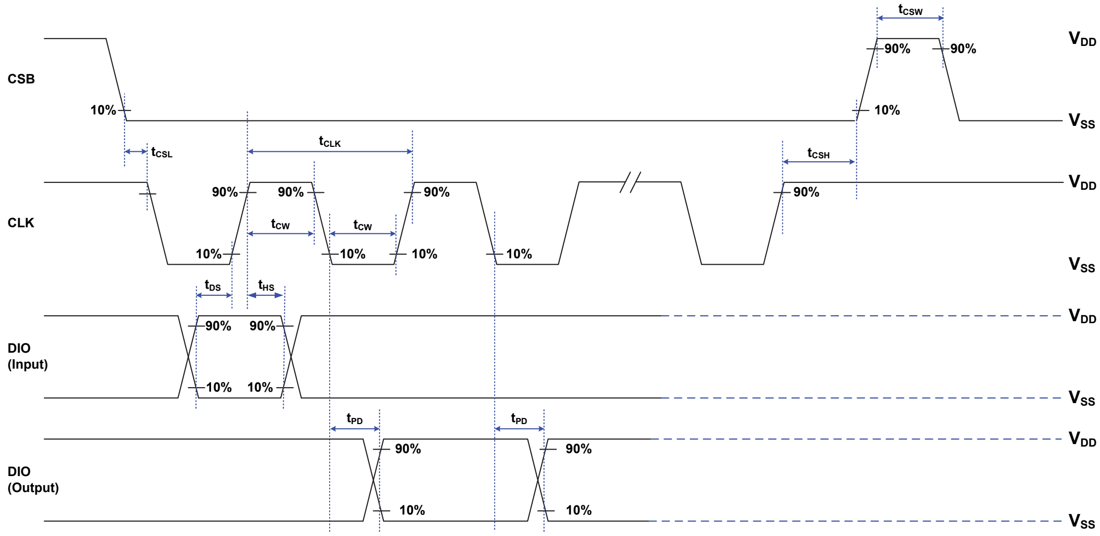
Ta=25°C

Symbol	Parameter	Conditions	V_{DD}=2.4V~5.5V		V_{DD}=3.0V~5.5V		Unit
			Min.	Max.	Min.	Max.	
f_{SCL}	Clock Frequency	—	—	100	—	400	kHz
t_{BUF}	Bus Free Time	Time in which the bus must be free before a new transmission can start	4.7	—	1.3	—	μs
$t_{HD:STA}$	Start Condition Hold Time	After this period, the first clock pulse is generated	4.0	—	0.6	—	μs
t_{LOW}	SCL Low Time	—	4.7	—	1.3	—	μs
t_{HIGH}	SCL High Time	—	4.0	—	0.6	—	μs
$t_{SU:STA}$	Start Condition Setup Time	Only relevant for repeated START condition	4.7	—	0.6	—	μs
$t_{HD:DAT}$	Data Hold Time	—	0	—	0	—	ns
$t_{SU:DAT}$	Data Setup Time	—	250	—	100	—	ns
t_R Note	SDA and SCL Rise Time	—	—	1.0	—	0.3	μs
t_F Note	SDA and SCL Fall Time	—	—	0.3	—	0.3	μs
$t_{SU:STO}$	Stop Condition Setup Time	—	4.0	—	0.6	—	μs
t_{AA}	Output Valid from Clock	—	—	3.5	—	0.9	μs
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	20	—	20	ns

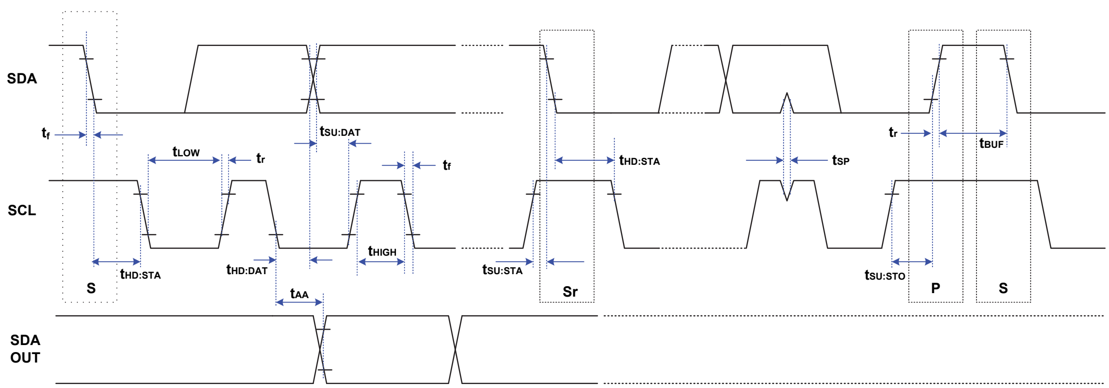
Note: These parameters are periodically sampled but not 100% tested.

Timing Diagrams

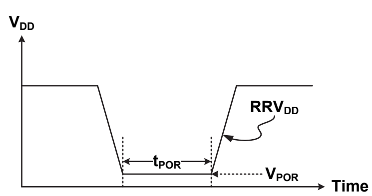
SPI 3-Wire Serial Bus Timing



I²C Bus Timing



Power on Reset Timing



Note: 1. If the conditions of Reset timing are not satisfied in power ON/OFF sequence, the internal Power on Reset (POR) circuit will not operate normally.
2. If it is difficult to meet power on reset timing conditions, please execute software reset command after Power on.

Functional Description

Power-on Reset

After power is applied the device will be initialised by an internal power-on reset circuit. The internal circuit status after initialisation is as follows:

- All registers are set to their default value but the contents of the DDRAM are not affected
- System Oscillator will be off
- All CA outputs and SYNC pin status will be high impedance
- The LED display will be in an off state

Data transfers on the I^2C-bus or SPI 3-wire serial bus should be avoided for 1ms following a power-on to allow the reset initialization operation to complete.

LED Driver

The HT16D31A/HT16D31B is a 72 pattern LED driver which can be configured as 8×9 pattern. This feature makes the HT16D31A/HT16D31B suitable for multiple LED applications.

System Oscillator

The internal logic and the LED drive signals of the HT16D31A/HT16D31B are timed by the integrated RC oscillator.

The System Clock frequency determines the LED frame frequency. A clock signal must always be supplied to the device; removing the clock may freeze the device if the standby mode command is executed. At initial system power on, the system oscillator is in the stop state.

Driver Outputs

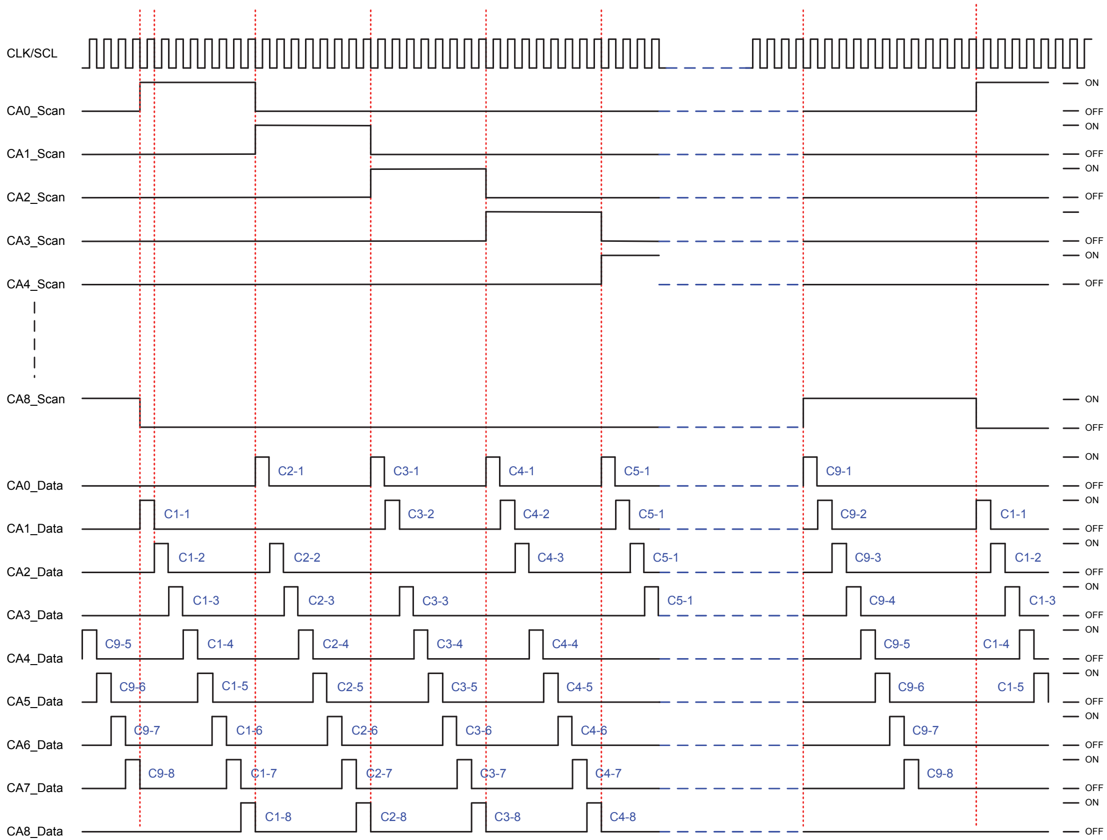
The LED driver offers an 8×9 LED Matrix with 1/9 cycle rate. The required lines to drive all 72 LEDs are reduced to 9 by using the cross-plexing feature optimizing space on the PCB. The driver output signals are generated in accordance with the data resident in the display latch. Each CA pin (CA0~CA8) can be switched to V_{SS} via the internal current sink (“low”), to V_{DD} (“high”) or not connected (“high-Z”).

Address Pointer

The addressing mechanism for the display RAM is implemented using the address pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialisation of the address pointer using the Address pointer command.

Open/Short Detection Function

These devices include open/short detection function that the open/short condition of the LED can be detected. It is recommended to implement the detection before using the devices for actual applications.



- When Open/Short detection is enabled and the CLK/SCL clock is input, the detection starts. The CAn detection time is equal to the input CLK/SCL clock pulse width. The CA1_Data~CA8_Data will start to be scanned in CA0_Scan time. Similarly in the CA1_Scan time, the CAn_Data (except CA1_Data) will be scanned. The whole scan operation will sequentially be implemented in the above way from CA1_Scan to CA8_Scan time. By this way, individual LED is checked for open or short condition during the scan.
- During the CAn_Scan active time, the CAn terminal pin voltages will be compared with two reference voltages to determine whether LED is open or short. Open or short condition of each LED can be read back by reading short detection data register or open detection data register.
- LED is detected as 'OPEN' state when the detected constant current output voltage is over LED_V_{SS}+0.5V. And it is only valid when the corresponding bit in Open Data RAM is set as "1".
- LED is detected as 'SHORT' state when the detected constant current output voltage is under LED_V_{DD}–0.5V. And it is only valid when the corresponding bit in Short Data RAM is set as "1".

Over Temperature Protection

The devices include thermal protection circuitry. When the junction temperatures exceed a certain detection temperature the temperature protection circuit is activated. The TSDF flag bit will be set to "1", the display will be off and the direct pins will be turned off.

When the chip junction temperature exceeds 150°C, the entire IC display is turned off and the direct pins will be turned off along with the TSDF flag bit being set to "1". The device will resume operation (normal display) and turn on the direct pins and the TSDF flag bit will be cleared to "0" when the chip junction temperature falls below 125°C.

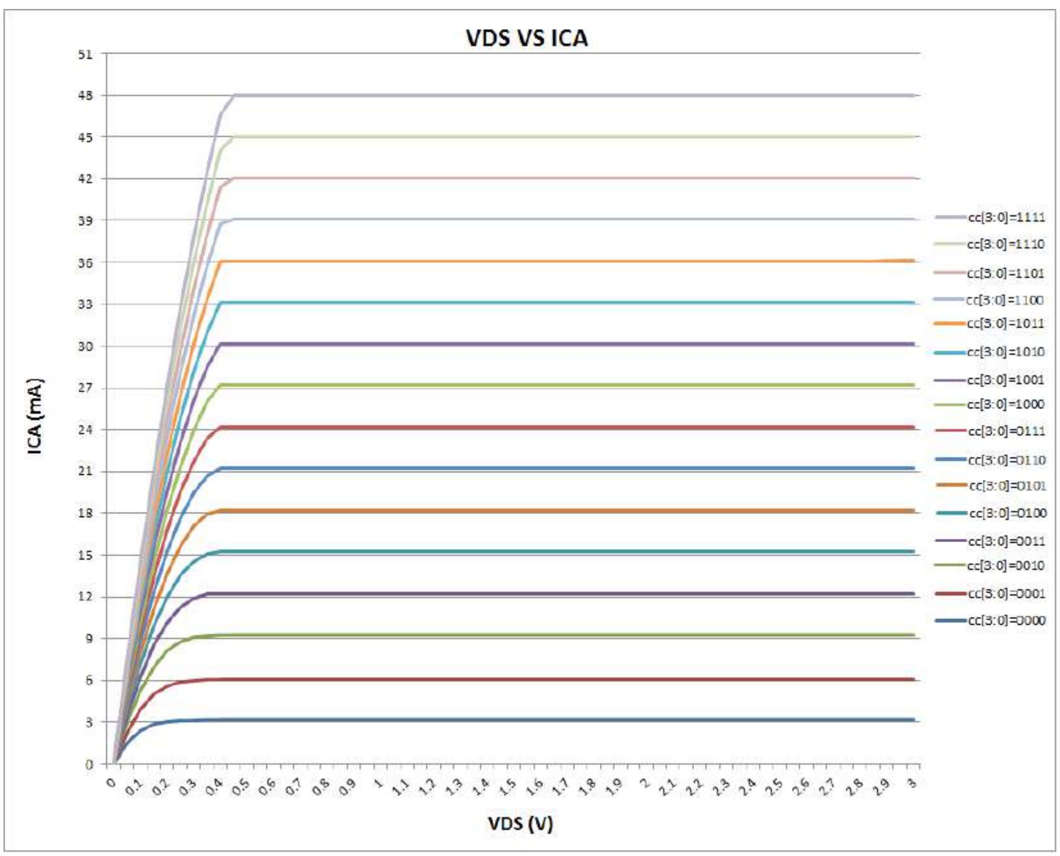
The temperature protection function detection temperature has a value of about 150°C. But as the detect temperature function includes hysteresis, its release temperature is about 125°C (Design reference value).

Constant Current Output

The Constant current output of each CA pin output channel can be setup internally. The current scale range can be adjusted by using the Constant Current Ratio command. The maximum current variation between channels is less than ±3%. The characteristics curve of output stage in the saturation region is flat for which users can refer to the charts below. The output current remains constant regardless of the LED forward voltage (V_F) variations.

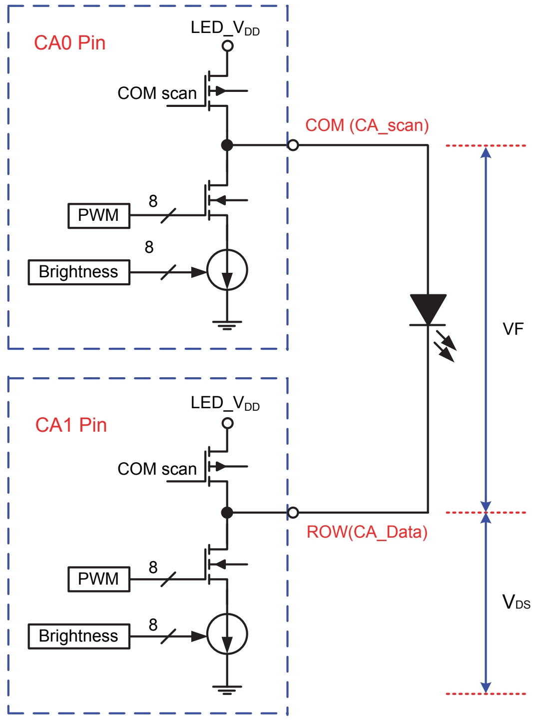
The output current (I_{CA}) scale range can be adjusted by using the Constant Current Ratio command. The maximum LED current is up to 48mA.

The default relationship between I_{CA} and Constant Current Ratio command set value is shown in the following figure.



Load Supply Voltage – LED_V_{DD}

The devices can be operated satisfactorily when V_{DS} lies in a range of 0.7V to 2.0V. It is recommended to use a low supply voltage for LED_V_{DD} to reduce the V_{DS} value which will reduce the device power consumption and subsequent device temperature.



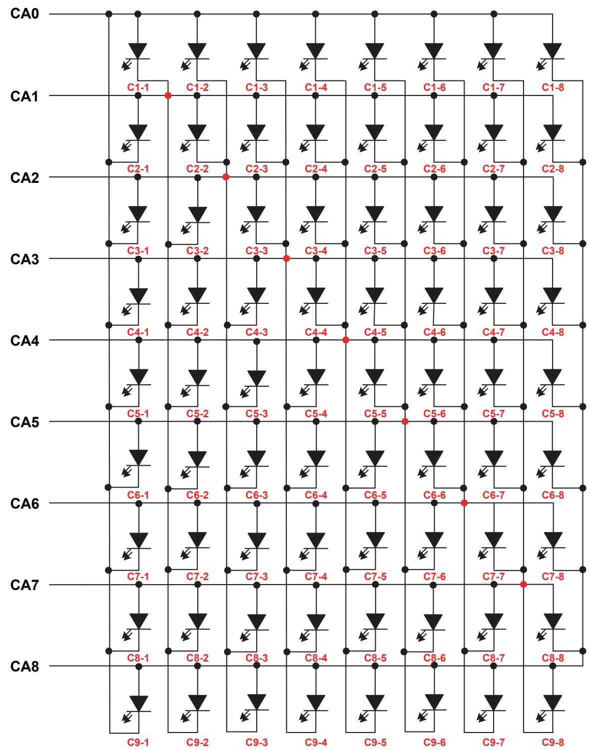
Display Data RAM – DDRAM

In the Binary Mode, the display RAM is a static 9×8-bit RAM in which the LED data is stored. A logic "1" in the RAM bit-map indicates an "on" state of the corresponding LED ROW. Similarly a logic "0" indicates an "off" state. There is a one-to-one correspondence between the display memory addresses and the CA pin outputs, and between the individual bits of a RAM word and the column outputs. The following shows the mapping from the RAM to the LED pattern.

Data Bit								ADDR
D7	D6	D5	D4	D3	D2	D1	D0	
C1-8	C1-7	C1-6	C1-5	C1-4	C1-3	C1-2	C1-1	00h
C2-8	C2-7	C2-6	C2-5	C2-4	C2-3	C2-2	C2-1	01h
C3-8	C3-7	C3-6	C3-5	C3-4	C3-3	C3-2	C3-1	02h
C4-8	C4-7	C4-6	C4-5	C4-4	C4-3	C4-2	C4-1	03h
C5-8	C5-7	C5-6	C5-5	C5-4	C5-3	C5-2	C5-1	04h
C6-8	C6-7	C6-6	C6-5	C6-4	C6-3	C6-2	C6-1	05h
C7-8	C7-7	C7-6	C7-5	C7-4	C7-3	C7-2	C7-1	06h
C8-8	C8-7	C8-6	C8-5	C8-4	C8-3	C8-2	C8-1	07h
C9-8	C9-7	C9-6	C9-5	C9-4	C9-3	C9-2	C9-1	08h

Note: The addresses will continuously increment automatically. The address will be wrapped around to address 00h when it exceeds the maximum address value of 08h.

The default relationship between RAM mapping and LED address is shown in the following figure.



In the Gray mode, the display RAM is a static 9×8×8-bit RAM in which the LED data is stored. A logic "1" in the RAM bit-map indicates an "on" state of the corresponding LED ROW. Similarly a logic 0 indicates an "off" state. There is a one-to-one correspondence between the display memory addresses and the CA pin outputs and between the individual bits of a RAM word and the column outputs.

The following shows the mapping from the RAM to the LED pattern.

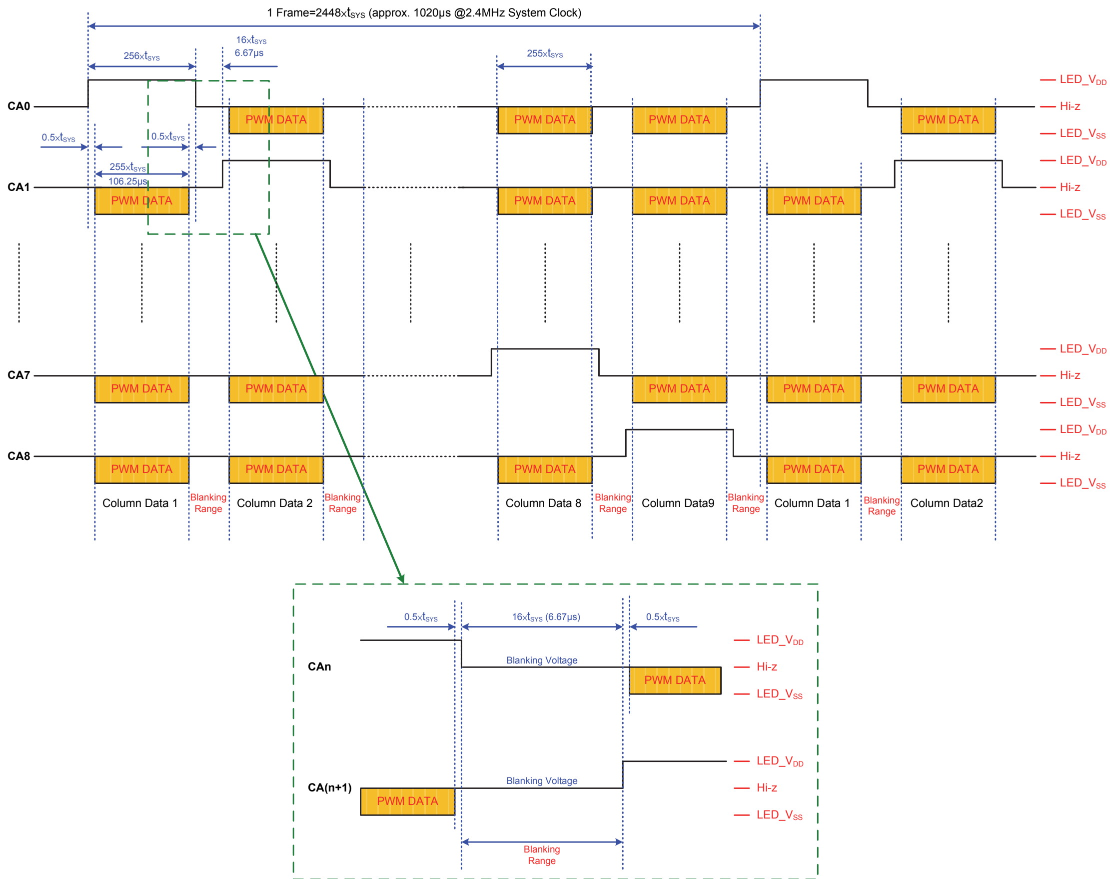
Data Byte								ADDR
D7~D0	D7~D0	D7~D0	D7~D0	D7~D0	D7~D0	D7~D0	D7~D0	
07h (C1-8)	06h (C1-7)	05h (C1-6)	04h (C1-5)	03h (C1-4)	02h (C1-3)	01h (C1-2)	00h (C1-1)	00h~07h
17h (C2-8)	16h (C2-7)	15h (C2-6)	14h (C2-5)	13h (C2-4)	12h (C2-3)	11h (C2-2)	10h (C2-1)	10h~17h
27h (C3-8)	26h (C3-7)	25h (C3-6)	24h (C3-5)	23h (C3-4)	22h (C3-3)	21h (C3-2)	20h (C3-1)	20h~27h
37h (C4-8)	36h (C4-7)	35h (C4-6)	34h (C4-5)	33h (C4-4)	32h (C4-3)	31h (C4-2)	30h (C4-1)	30h~37h
47h (C5-8)	46h (C5-7)	45h (C5-6)	44h (C5-5)	43h (C5-4)	42h (C5-3)	41h (C5-2)	40h (C5-1)	40h~47h
57h (C6-8)	56h (C6-7)	55h (C6-6)	54h (C6-5)	53h (C6-4)	52h (C6-3)	51h (C6-2)	50h (C6-1)	50h~57h
67h (C7-8)	66h (C7-7)	65h (C7-6)	64h (C7-5)	63h (C7-4)	62h (C7-3)	61h (C7-2)	60h (C7-1)	60h~67h
77h (C8-8)	76h (C8-7)	75h (C8-6)	74h (C8-5)	73h (C8-4)	72h (C8-3)	71h (C8-2)	70h (C8-1)	70h~77h
87h (C9-8)	86h (C9-7)	85h (C9-6)	84h (C9-5)	83h (C9-4)	82h (C9-3)	81h (C9-2)	80h (C9-1)	80h~87h

Note: The addresses will continuously increment automatically. The address will be wrapped around to address 00h when it exceeds the maximum address value of 87h.

LED Driver Output Waveform

The devices include a 72 (8×9) pattern LED driver. This can be setup in a 8×9 format for the COM outputs. This feature allows the device to be used in multiple LED applications. The LED driver mode waveforms and scanning format is as follows.

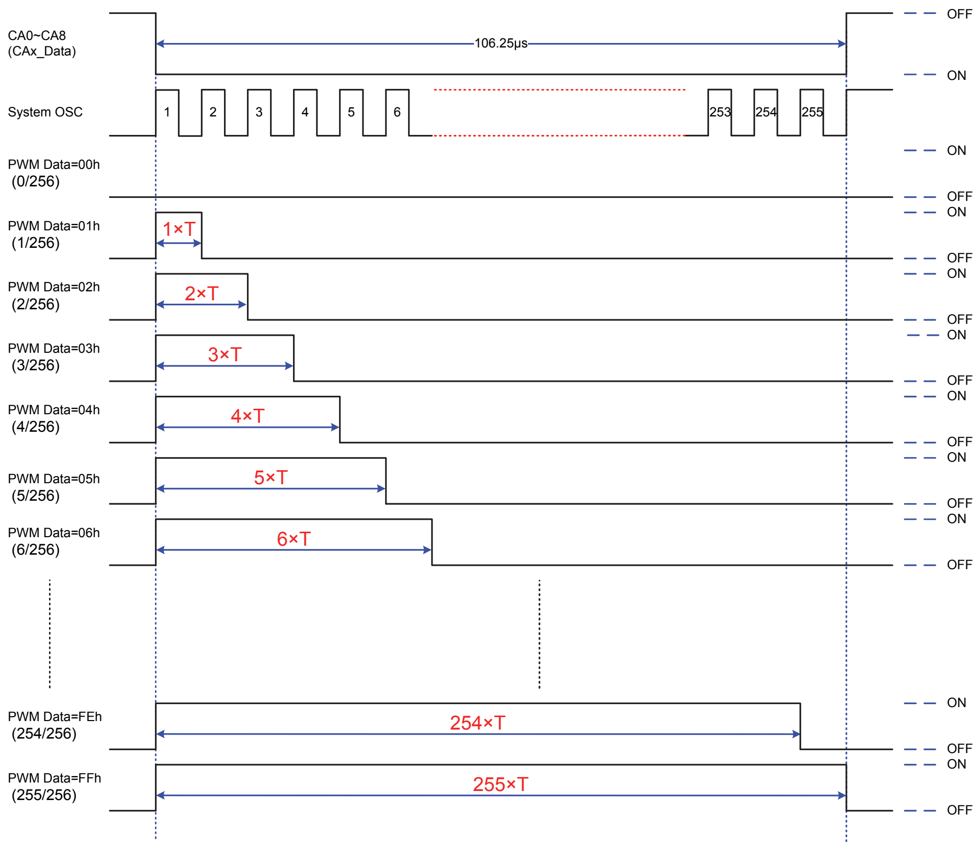
8×9 Driver Mode and Disable Discharge Function.



Note: $t_{SYS} = 1/f_{SYS}$ (1/2.4MHz).

PWM Data Width Timing

The PWM Data width timings are shown in the accompanying diagram.



Note: $t_{SYS} = 1/f_{SYS}$ (1/2.4MHz).

Fade Data RAM

The fade RAM is a static 36×8-bit RAM in which the mode function, delay time function and slope cycle time function for each dot is stored. There is a one-to-one correspondence between the fade function memory addresses and the CA pin outputs and between the individual bits of a RAM word and the column outputs.

Write Dot Fade Data	W	1	0	0	0	0	0	1	0	82h	Write Fade RAM Data
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	RAM Address
	W	FS2	FT2_1	FT1_1	FT0_1	FS1	FT2_0	FT1_0	FT0_0	—	Set Parameters for Fade Mode FS: Blink or Fade Mode select FT: Blink or Fade cycle time set

FS1/FS2	Select	Remarks
0	Fade Mode	Default
1	Blink Mode	—

The cycle time set is setup as follows.

FT2_0 /(FT 2_1)	FT 1_0 /(FT 1_1)	FT 0_0 /(FT 0_1)	Fade T1 Time	Remarks
0	0	0	Off	Default
0	0	1	256 frames	1×256
0	1	0	512 frames	2×256
0	1	1	1024 frames	4×256
1	0	0	1536 frames	6×256
1	0	1	2048 frames	8×256
1	1	0	2560 frames	10×256
1	1	1	3072 frames	12×256

Note: 1. In the Binary Mode the Fade data setting for each dot RAM is invalid.
2. The setup time is based on OSC frequency.

Pixel	1 Frame Time
8×9	((256+16)×9)/2.4MHz≈1.02ms

The following shows a mapping from the Fade RAM to the LED pattern.

Data Byte								ADDR
D7~ D4	D3~D0	D7~ D4	D3~D0	D7~ D4	D3~D0	D7~ D4	D3~D0	
03h (C1-8)	03h (C1-7)	02h (C1-6)	02h (C1-5)	01h (C1-4)	01h (C1-3)	00h (C1-2)	00h (C1-1)	00h~03h
13h (C2-8)	13h (C2-7)	12h (C2-6)	12h (C2-5)	11h (C2-4)	11h (C2-3)	10h (C2-2)	10h (C2-1)	10h~13h
23h (C3-8)	23h (C3-7)	22h (C3-6)	22h (C3-5)	21h (C3-4)	21h (C3-3)	20h (C3-2)	20h (C3-1)	20h~23h
33h (C4-8)	33h (C4-7)	32h (C4-6)	32h (C4-5)	31h (C4-4)	31h (C4-3)	30h (C4-2)	30h (C4-1)	30h~33h
43h (C5-8)	43h (C5-7)	42h (C5-6)	42h (C5-5)	41h (C5-4)	41h (C5-3)	40h (C5-2)	40h (C5-1)	40h~43h
53h (C6-8)	53h (C6-7)	52h (C6-6)	52h (C6-5)	51h (C6-4)	51h (C6-3)	50h (C6-2)	50h (C6-1)	50h~53h
63h (C7-8)	63h (C7-7)	62h (C7-6)	62h (C7-5)	61h (C7-4)	61h (C7-3)	60h (C7-2)	60h (C7-1)	60h~63h
73h (C8-8)	73h (C8-7)	72h (C8-6)	72h (C8-5)	71h (C8-4)	71h (C8-3)	70h (C8-2)	70h (C8-1)	70h~73h
83h (C9-8)	83h (C9-7)	82h (C9-6)	82h (C9-5)	81h (C9-4)	81h (C9-3)	80h (C9-2)	80h (C9-1)	80h~83h

Note: The addresses will continuously increment automatically. The address will be wrapped around to address 00h when it exceeds the maximum address value of 83h.

LED On/Off Control RAM Data

The LED on/off RAM is a static 9×8-bit RAM in which the LED mask data is stored. A logic "1" in the RAM bit-map indicates a "LED Control on" state of the corresponding LED ROW; similarly a logic "0" indicates a "LED Control off" state.

There is a one-to-one correspondence between the LED on/off Control memory addresses and the CA pin outputs and between the individual bits of a RAM word and the column outputs.

The following shows the mapping from the LED on/off Control RAM to the LED pattern.

Data Bit								ADDR
D7	D6	D5	D4	D3	D2	D1	D0	
C1-8	C1-7	C1-6	C1-5	C1-4	C1-3	C1-2	C1-1	00h
C2-8	C2-7	C2-6	C2-5	C2-4	C2-3	C2-2	C2-1	01h
C3-8	C3-7	C3-6	C3-5	C3-4	C3-3	C3-2	C3-1	02h
C4-8	C4-7	C4-6	C4-5	C4-4	C4-3	C4-2	C4-1	03h
C5-8	C5-7	C5-6	C5-5	C5-4	C5-3	C5-2	C5-1	04h
C6-8	C6-7	C6-6	C6-5	C6-4	C6-3	C6-2	C6-1	05h
C7-8	C7-7	C7-6	C7-5	C7-4	C7-3	C7-2	C7-1	06h
C8-8	C8-7	C8-6	C8-5	C8-4	C8-3	C8-2	C8-1	07h
C9-8	C9-7	C9-6	C9-5	C9-4	C9-3	C9-2	C9-1	08h

Note: 1. Write 9 bytes data into the LED on/off RAM from the start address 00h. The addresses will continuously increment automatically. The address will be wrapped around to address 00h when it exceeds the maximum address value of 08h.
2. In the Binary Mode the LED on/off Control RAM function is invalid.

Command Description

Command Table

Command	R/W	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Description
RAM Page Address Command											
RAM Page Address Set	W	1	1	1	1	1	1	0	1	FDh	Set RAM response page select
	W	X	X	X	X	A3	A2	A1	A0	00h	Page RAM address
RAM R/W Command											
Write Display Data	W	1	0	0	0	0	0	0	0	80h	Write display RAM data
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	RAM address
	W	D7	D6	D5	D4	D3	D2	D1	D0	—	Display data Range: 00h~FFh
Read Display Data	W	1	0	0	0	0	0	0	1	81h	Read display RAM
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	RAM address
	R	0	0	0	0	0	0	0	0	00h	Dummy byte
	R	D7	D6	D5	D4	D3	D2	D1	D0	—	Display data Range: 00h~FFh
Write Dot Fade Data	W	1	0	0	0	0	0	1	0	82h	Write fade RAM data
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	RAM address
	W	FS2	FT2_1	FT1_1	FT0_1	FS1	FT2_0	FT1_0	FT0_0	—	Set parameters for fade mode FS: Blink or fade mode select FT: Blink or fade cycle time set
Read Dot Fade Data	W	1	0	0	0	0	0	1	1	83h	Read parameters of fade RAM data
	W	A7	A6	A5	A4	A3	A2	A1	A0	00h	RAM address
	R	0	0	0	0	0	0	0	0	00h	Dummy byte
	R	FS1	FT2_1	FT1_1	FT0_1	FS0	FT2_0	FT1_0	FT0_0	—	Parameters of fade data

Command	R/W	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Description
Write LED Control Data	W	1	0	0	0	0	1	0	0	84h	Write LED on/off control Data for each dot.
	W	0	0	0	A4	A3	A2	A1	A0	00h	RAM Address
	W	D7	D6	D5	D4	D3	D2	D1	D0	—	LED on/off control data
Read LED Control Data	W	1	0	0	0	0	1	0	1	85h	Read LED on/off control Data for each dot.
	W	0	0	0	A4	A3	A2	A1	A0	00h	RAM Address
	R	0	0	0	0	0	0	0	0	00h	Dummy Byte
	R	D7	D6	D5	D4	D3	D2	D1	D0	—	LED on/off control Data
Function Command											
Picture Start Page Address	W	0	0	0	1	0	0	0	0	10h	Set start address for Picture Mode
	W	X	X	X	X	PFS3	PFS2	PFS1	PFS0	00h	
Movie Start Page Address	W	0	0	0	1	0	0	0	1	11h	Set start address for Movie Mode
	W	MEN	X	X	X	MFS3	MFS2	MFS1	MFS0	00h	
Movie Playing Length	W	0	0	0	1	0	0	1	0	12h	Number of pages played in a movie.
	W	X	X	X	X	MFL 3	MFL 2	MFL 1	MFL 0	01h	
Movie Cycles Time	W	0	0	0	1	0	0	1	1	13h	Number of loops played in a movie
	W	X	X	X	X	MCT3	MCT2	MCT1	MCT0	00h	
Movie Page Delay Time	W	0	0	0	1	0	1	0	0	14h	Delay time between two pages in a movie.
	W	X	X	MPD5	MPD4	MPD3	MPD2	MPD1	MPD0	04h	
Last Page	W	0	0	0	1	0	1	0	1	15h	The last page displayed in a movie (depending on the cycle time of loops played in a movie)
	W	X	X	X	X	MLP3	MLP2	MLP1	MLP0	00h	
Picture Scrolling Control	W	0	0	1	0	0	0	0	0	20h	Set scrolling function for Picture Mode SCEN: Scrolling SW on/off RL: Right or Left scrolling direction HSP0~4: Horizontal Speed
	W	SCEN	X	RL	HSP4	HSP3	HSP2	HSP1	HSP0	00h	
Display Mode	W	0	0	1	1	0	0	0	0	30h	Picture Display Mode or Movie Display Mode select
	W	X	X	X	X	X	X	X	MP	00h	
Configuration Mode	W	0	0	1	1	0	0	0	1	31h	Binary Mode or Gray Mode select
	W	BGS	X	X	X	X	X	X	X	00h	
Fade Function Control	W	0	0	1	1	0	0	1	0	32h	FFEN: Fade function enable/disable GMEN: Linear Intensity Mode or Gamma Intensity Mode GFEN: Global or each dot display mode FOT: Fade Out Time FET: Extinguish time FLT: Light time
	W	FFEN	GMEN	GFEN	FOT	FET1	FET0	FLT1	FLT0	4Ah	
Global Fade Time	W	0	0	1	1	0	0	1	1	33h	Global Blinking/Fade Period Time set
	W	GFS	X	X	X	X	GFT2	GFT1	GFT0	00h	
Cascade Mode	W	0	0	1	1	0	1	0	0	34h	Master Mode or Slave Mode select
	W	X	X	X	X	X	X	MS1	MS0	00h	
System Control	W	0	0	1	1	0	1	0	1	35h	System Oscillator on/off and Display on/off control
	W	X	X	X	X	X	X	FON	DON	00h	
Constant Current Ratio	W	0	0	1	1	0	1	1	0	36h	Constant Current Ratio – 16 steps
	W	X	X	X	X	CC3	CC2	CC1	CC0	0Ah	
Global Brightness	W	0	0	1	1	0	1	1	1	37h	Luminance Control – 256 steps
	W	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	FFh	

Command	R/W	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Description
Mode Control	W	0	0	1	1	1	0	0	0	38h	TSDEN: Thermal protect circuit on/off TSDS: Select auto control or user control display on/off function when the over temperature protection is enabled ODEN: Open Detection on/off SDEN: Short Detection on/off
	W	TSD EN	TSDS	X	X	X	X	OD EN	SD EN	00h	
Blanking Voltage Set	W	0	0	1	1	1	0	0	1	39h	Blanking Voltage Control –16 steps
	W	VBEN	X	X	X	VB3	VB2	VB1	VB0	0Fh	
Soft Reset	W	1	1	0	0	1	1	0	0	CCh	Soft Reset Function
Read Register Status	W	0	1	1	1	0	0	0	0	70h	Read internal command information
	R	D7	D6	D5	D4	D3	D2	D1	D0	—	Internal command information
Read Movie Frame Status	W	0	1	1	1	0	0	0	1	71h	Read Movie frame and status information
	R	MOF1	MOF0	X	X	MDF3	MDF2	MDF1	MDF0	—	MDF: Actual displayed frame. MOF: Movie is finished
Read Movie Loop Status	W	0	1	1	1	0	0	1	0	72h	Read Movie loop operation and status information
	R	MOL1	MOL0	X	X	MLP3	MLP2	MLP1	MLP0	—	MLP: Actual displayed loop times. MOL: Play loop is finished
Read Function Flag	W	0	1	1	1	0	0	1	1	73h	Read Function parameters flag data
	R	CAF	X	X	X	X	X	X	TSDF	00h	TSDF: Over temperature limit is reached. CAF: Indicate the 1st CA Scan waveform
Read Open Detection Data	W	0	1	1	1	0	1	0	0	74h	Read LED Matrix Open status address
	R	0	0	0	0	0	0	0	0	00h	Dummy byte
	R	D7	D6	D5	D4	D3	D2	D1	D0	—	Detection data information
Read Short Detection Data	W	0	1	1	1	0	1	0	1	75h	Read LED Matrix Short status address
	R	0	0	0	0	0	0	0	0	00h	Dummy byte
	R	D7	D6	D5	D4	D3	D2	D1	D0	—	Detection data information

Note: 1. X: Don't care
2. Def.: Power on reset default
3. It is not recommended to change between Master and Slave mode after a system enable
4. If programmed command data is not defined the function will not be affected

Software Reset

This command is set to initialise all functions

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Soft Reset	W	1	1	0	0	1	1	0	0	CCh

The internal circuit status after initialisation is as follows.

- All registers are set to their default value but the contents of the DDRAM are not affected
- System Oscillator is off
- All CA outputs are high impedance
- The LED display is in an off state

RAM Page Address Set

This command is to set the memory page address.

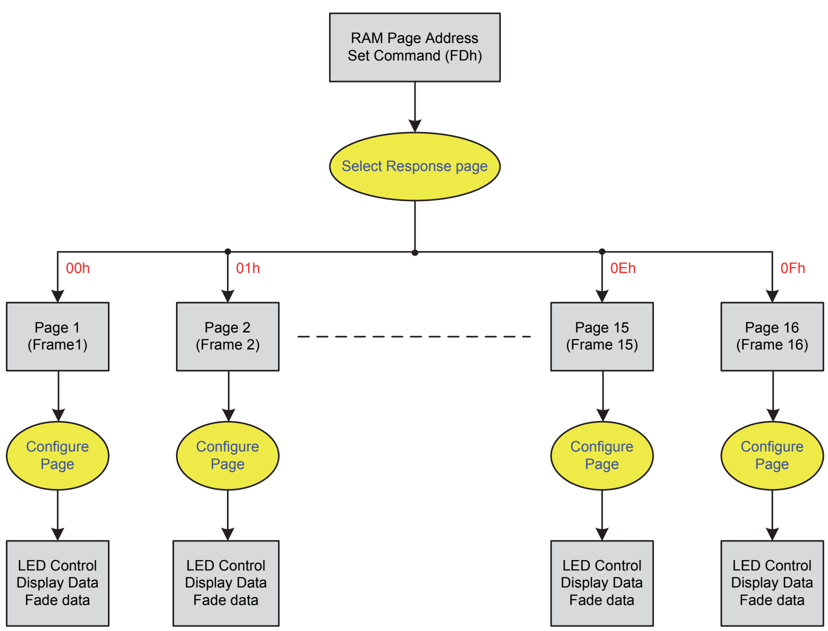
Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
RAM Page Address Set	W	1	1	1	1	1	1	0	1	FDh
	W	X	X	X	X	A3	A2	A1	A0	00h

A3	A2	A1	A0	RAM Page Address		Remarks
				Gray Mode	Binary Mode	
0	0	0	0	Page1	Page1	(Default)
0	0	0	1	Page2	Page2	—
0	0	1	0	—	Page3	—
0	0	1	1	—	Page4	—
0	1	0	0	—	Page5	—
0	1	0	1	—	Page6	—
0	1	1	0	—	Page7	—
0	1	1	1	—	Page8	—
1	0	0	0	—	Page9	—
1	0	0	1	—	Page10	—
1	0	1	0	—	Page11	—
1	0	1	1	—	Page12	—
1	1	0	0	—	Page13	—
1	1	0	1	—	Page14	—
1	1	1	0	—	Page15	—
1	1	1	1	—	Page16	—

Note: If programmed command data is not defined the function will not be affected.

RAM Page Configure

User has to first configure the RAM Page Address Set Command (FDh) , then follows is the data 00h~0Fh to select the Page No., and then users can configure the display data value and function in that Page No.



Picture Start Page Address

This command is to set the start display page in Picture Mode.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Picture Start Page Address	W	0	0	0	1	0	0	0	0	10h
	W	X	X	X	X	PFS3	PFS2	PFS1	PFS0	00h

PFS3	PFS2	PFS1	PFS0	RAM Page Address		Remarks
				Gray Mode	Binary Mode	
0	0	0	0	Page1	Page1	(Default)
0	0	0	1	Page2	Page2	—
0	0	1	0	—	Page3	—
0	0	1	1	—	Page4	—
0	1	0	0	—	Page5	—
0	1	0	1	—	Page6	—
0	1	1	0	—	Page7	—
0	1	1	1	—	Page8	—
1	0	0	0	—	Page9	—
1	0	0	1	—	Page10	—
1	0	1	0	—	Page11	—
1	0	1	1	—	Page12	—
1	1	0	0	—	Page13	—
1	1	0	1	—	Page14	—
1	1	1	0	—	Page15	—
1	1	1	1	—	Page16	—

Note: If programmed command data is not defined the function will not be affected.

Movie Start Page Address

This command is to set the start display page in Movie Mode.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Movie Start Page Address	W	0	0	0	1	0	0	0	1	11h
	W	MEN	X	X	X	MFS3	MFS2	MFS1	MFS0	00h

MEN	SW	Remarks
0	Movie disable	Default
1	Movie enable	—

MFS3	MFS2	MFS1	MFS0	RAM Page Address		Remark
				Gray Mode	Binary Mode	
0	0	0	0	Page1	Page1	(Default)
0	0	0	1	Page2	Page2	—
0	0	1	0	—	Page3	—
0	0	1	1	—	Page4	—
0	1	0	0	—	Page5	—
0	1	0	1	—	Page6	—
0	1	1	0	—	Page7	—
0	1	1	1	—	Page8	—
1	0	0	0	—	Page9	—
1	0	0	1	—	Page10	—

MFS3	MFS2	MFS1	MFS0	RAM Page Address		Remark
				Gray Mode	Binary Mode	
1	0	1	0	—	Page11	—
1	0	1	1	—	Page12	—
1	1	0	0	—	Page13	—
1	1	0	1	—	Page14	—
1	1	1	0	—	Page15	—
1	1	1	1	—	Page16	—

Note: If programmed command data is not defined the function will not be affected.

Movie Playing Length Set

This command is to set the playing page length in movie mode.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Movie Playing Length	W	0	0	0	1	0	0	1	0	12h
	W	X	X	X	X	MFL3	MFL2	MFL1	MFL0	01h

MFL3	MFL2	MFL1	MFL0	Page Number		Remarks
				Gray Mode	Binary Mode	
0	0	0	0	1 Page	1 Page	—
0	0	0	1	2 Pages	2 Pages	(Default)
0	0	1	0	—	3 Pages	—
0	0	1	1	—	4 Pages	—
0	1	0	0	—	5 Pages	—
0	1	0	1	—	6 Pages	—
0	1	1	0	—	7 Pages	—
0	1	1	1	—	8 Pages	—
1	0	0	0	—	9 Pages	—
1	0	0	1	—	10 Pages	—
1	0	1	0	—	11 Pages	—
1	0	1	1	—	12 Pages	—
1	1	0	0	—	13 Pages	—
1	1	0	1	—	14 Pages	—
1	1	1	0	—	15 Pages	—
1	1	1	1	—	16 Pages	—

Note: If programmed command data is not defined, the function will not be affected.

Movie Cycle Time Set

This command is to set the number of loops played in one movie.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Movie Cycle Time	W	0	0	0	1	0	0	1	1	13h
	W	X	X	X	X	MCT3	MCT2	MCT1	MCT0	00h

MCT3	MCT2	MCT1	MCT0	Loops Number	Remarks
0	0	0	0	1 loop	Default
0	0	0	1	2 loops	—
0	0	1	0	3 loops	—
0	0	1	1	4 loops	—
0	1	0	0	5 loops	—

MCT3	MCT2	MCT1	MCT0	Loops Number	Remarks
0	1	0	1	6 loops	—
0	1	1	0	7 loops	—
0	1	1	1	8 loops	—
1	X	X	X	Endless	Must be set to 0~7 to stop the movie

Note: 1. If programmed command data is not defined, the function will not be affected.
2. When a "Endless" mode is selected, the movie cycle time command must be set to a value in the range of from 0000b to 0111b to stop the movie play.

Movie Page Delay Time

This command is to set the delay time between two pages in a movie.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Movie Page Delay Time	W	0	0	0	1	0	1	0	0	14h
	W	X	X	MPD5	MPD4	MPD3	MPD2	MPD1	MPD0	04h

Note: If programmed command data is not defined, the function will not be affected.

The setup time is based on the OSC frequency.

Pixel	1 Frame Time
8×9	((256+16)×9)/2.4MHz≈1.02ms

Movie page delay time=(MPD[5:0]+1)×8×1frame time=(1~64)×8×1frame time=(8~512)×1 frame time.

For example, When MPD[5:0]=4, Movie page delay time=5×8×1.02(ms)=40.8ms.

Last Page Set

This command is to set the last page displayed in a movie and the setting is also depending on the cycle time of loops played in a movie.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Last Page Set	W	0	0	0	1	0	1	0	1	15h
	W	X	X	X	X	MLP3	MLP2	MLP1	MLP0	00h

MLP3	MLP2	MLP1	MLP0	RAM Page Address		Remarks
				Gray Mode	Binary Mode	
0	0	0	0	Page1	Page1	(Default)
0	0	0	1	Page2	Page2	—
0	0	1	0	—	Page3	—
0	0	1	1	—	Page4	—
0	1	0	0	—	Page5	—
0	1	0	1	—	Page6	—
0	1	1	0	—	Page7	—
0	1	1	1	—	Page8	—
1	0	0	0	—	Page9	—
1	0	0	1	—	Page10	—
1	0	1	0	—	Page11	—
1	0	1	1	—	Page12	—
1	1	0	0	—	Page13	—
1	1	0	1	—	Page14	—
1	1	1	0	—	Page15	—
1	1	1	1	—	Page16	—

Note: If programmed command data is not defined, the function will not be affected.

Picture Scrolling Control

This command is used to control the scrolling function on/off and picture scrolling direction.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Picture Scrolling Control	W	0	0	1	0	0	0	0	0	20h
	W	SCEN	X	RL	HSP4	HSP3	HSP2	HSP1	HSP0	00h

SCEN	Scrolling Function SW	Remarks
0	OFF	Default
1	ON	—

RL	Scrolling Direction	Remarks
0	Left	Default
1	Right	—

Horizontal Scrolling Speed=(HSP[4:0]+1)×32×1frame time=(1~32)×32×1frame time=(32~1024)×1 frame time.

The setup time is based on the OSC frequency.

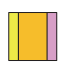
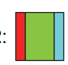
Pixel	1 Frame Time
8×9	((256+16)×9)/2.4MHz≈1.02ms

For example, When HSP [4:0]=3, Horizontal Scrolling Speed=4×32×1.02(ms)=130.56ms

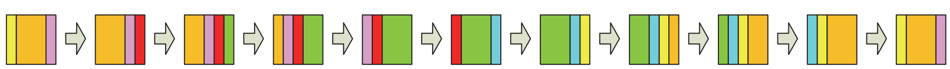
Note: 1. If programmed command data is not defined, the function will not be affected.
2. Single row horizontal scrolling.
3. When the scrolling mode is enabled, it is not recommended to execute the fade function or movie function.
4. The function is suitable for the Gray Mode only. In the Binary Mode, the scrolling function is invalid.

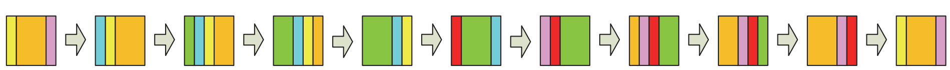
Example – Horizontal Scrolling Set

Set the display RAM data for each page as follows:

Page1:  Page2: 

After the scrolling function is enabled, the status of left or right scrolling is as follows:

Left Scrolling


Right Scrolling


Display Mode

This command is used to set the LED matrix display mode.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Display Mode	W	0	0	1	1	0	0	0	0	30h
	W	X	X	X	X	X	X	X	MP	00h

MP	Display Mode	Remarks
0	Picture	Default
1	Movie	—

Note: If programmed command data is not defined, the function will not be affected.

Configuration Mode

The command can be used to set the Binary Mode or Gray Mode.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Binary/Gray Select	W	0	0	1	1	0	0	0	1	31h
	W	BGS	X	X	X	X	X	X	X	00h

BGS	Select	Remarks
0	Gray	Default
1	Binary	—

Note: If programmed command data is not defined, the function will not be affected.

Fade Function Control

This command is used to control the fade function on/off, the display option. This command parameter is validated during the Timing 1 period of each frame when the command is set.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Fade Function Control	W	0	0	1	1	0	0	1	0	32h
	W	FFEN	GMEN	GFEN	FOT	FET1	FET0	FLT1	FLT0	4Ah

FFEN	Fade Function Control SW	Remarks
0	Disable	Default
1	Enable	—

GMEN	CA Output Option Selection	Remarks
0	Linear Intensity Mode	—
1	Gamma Intensity Mode	Default

GFEN	Display Option Selection	Remarks
0	Each Dot	Default
1	Global	—

FOT	Fade Out Time Control (T3)	Remarks
0	T1	Default
1	T1×2	—

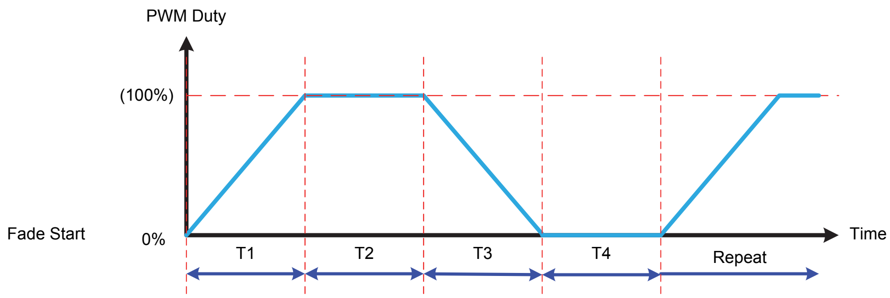
FET1	FET0	Extinguish Time Control (T4)	Remarks
0	0	T1×0.25	—
0	1	T1×0.5	—
1	0	T1	Default
1	1	T1×2	—

FLT1	FLT0	Light Time Control (T2)	Remarks
0	0	T1×0.25	—
0	1	T1×0.5	—
1	0	T1	Default
1	1	T1×2	—

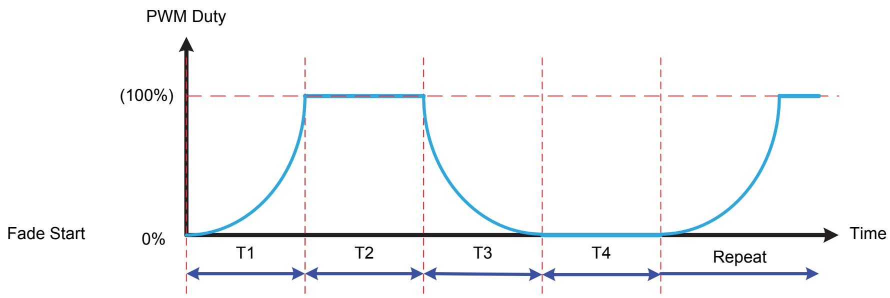
Note: 1. If programmed command data is not defined, the function will not be affected.
2. The T1 time is controlled by the Write Dot Fade Data Command of RAM R/W commands.
3. In the Binary Mode the Fade for each dot function is invalid.

Fade Function

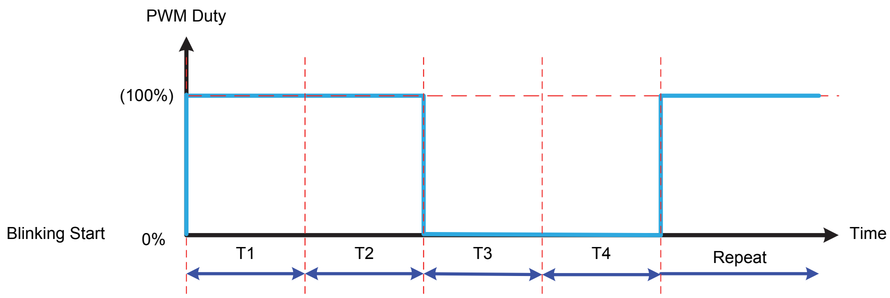
(1) Linear intensity mode



(2) Gamma intensity mode



Blinking Function



Global Fade Time

The device contains a versatile blinking function. The whole display can be made to blink or fade times selected by the global blinking/fade time command, this command parameter is validated by each timing 1 of frame when the command is set.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Global Fade Time	W	0	0	1	1	0	0	1	1	33h
	W	GFS	X	X	X	X	GFT2	GFT1	GFT0	00h

Note: The blinking times are integer multiples of the system frequency. The ratios between the system oscillator and the blinking times depend upon the mode, in which the device is operating.

GFS	Select	Remarks
0	Fade Mode	Default
1	Global Blink Mode	—

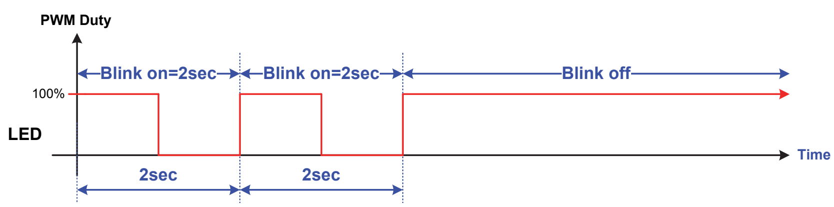
GFT2	GFT1	GFT0	Global Fade Time (T1)	Remarks
0	0	0	OFF	Default
0	0	1	256 frames	1×256
0	1	0	512 frames	2×256
0	1	1	1024 frames	4×256
1	0	0	1536 frames	6×256
1	0	1	2048 frames	8×256
1	1	0	2560 frames	10×256
1	1	1	3072 frames	12×256

Note: 1. If programmed command data is not defined, the function will not be affected.
2. The setup time is based on OSC frequency.

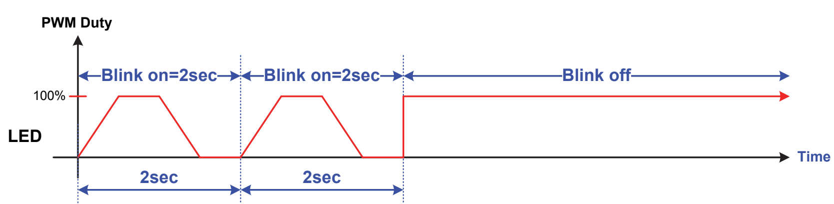
Pixel	1 frame time
8×9	((256+16)×9)/2.4MHz≈1.02ms

Examples

- Blink Output Type – Blinking Time = 2sec



- Fade Output Type – Blinking Time = 2sec



Cascade Mode

This command will select master/slave mode.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Cascade Mode	W	0	0	1	1	0	1	0	0	34h
	W	X	X	X	X	X	X	MS1	MS0	00h

MS1	MS0	SYNC pin Status	Remarks
0	0	High impedance	1. Default 2. Only single chip application
0	1	Oscillator output mode	Master Mode
1	0	Oscillator input mode	Slave Mode
1	1	High impedance	—

Note: It is not recommended to change between MASTER and SLAVE mode after a system oscillator enable.

System Control

This command controls the system oscillator on/off and display on/off.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
System Control	W	0	0	1	1	0	1	0	1	35h
	W	X	X	X	X	X	X	FON	DON	00h

FON	DON	System Oscillator	LED Display	Remarks
0	X	Off	Off	1. Default 2. Standby mode 3. Temperature protection disable
1	0	On	Off	CA active
1	1	On	On	Normal display mode

Note: If programmed command data is not defined, the function will not be affected.

Constant Current Ratio

This command is used to select the constant current ratio according to the LED panel characteristics.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Constant Current Ratio	W	0	0	1	1	0	1	1	0	36h
	W	X	X	X	X	CC3	CC2	CC1	CC0	0Ah

CC3	CC2	CC1	CC0	Constant Current Ratio	Remarks
0	0	0	0	3mA	—
0	0	0	1	6mA	—
0	0	1	0	9mA	—
0	0	1	1	12mA	—
0	1	0	0	15mA	—
0	1	0	1	18mA	—
0	1	1	0	21mA	—
0	1	1	1	24mA	—
1	0	0	0	27mA	—
1	0	0	1	30mA	—
1	0	1	0	33mA	Default
1	0	1	1	36mA	—
1	1	0	0	39mA	—
1	1	0	1	42mA	—
1	1	1	0	45mA	—
1	1	1	1	48mA	—

Note: If programmed command data is not defined, the function will not be affected.

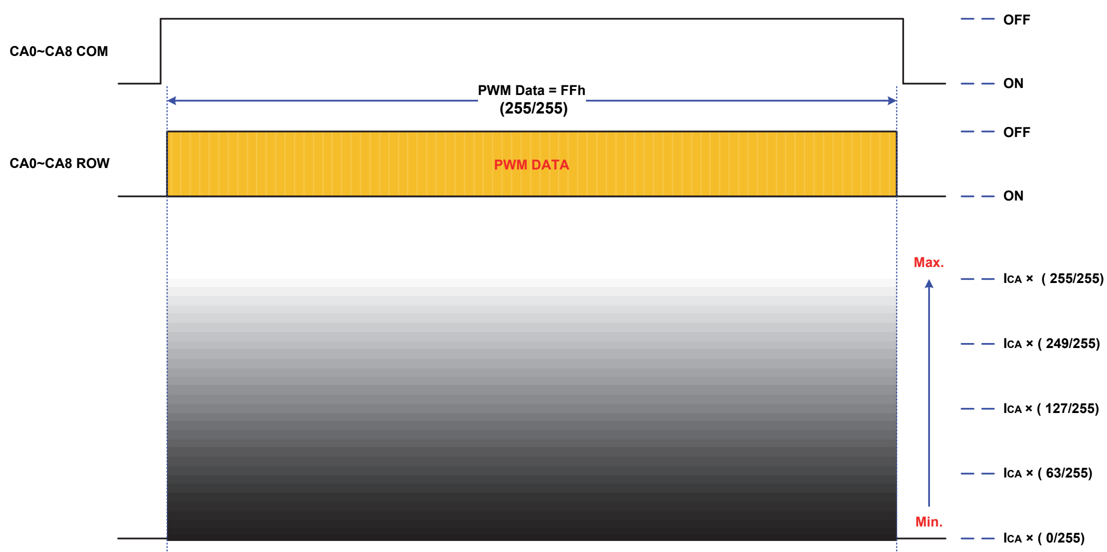
Brightness Control

This command controls the 256-step PWM luminance control. It has a common setting for all dots by digital dimming duty adjustment.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Brightness control	W	0	0	1	1	0	1	1	1	37h
	W	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	FFh

BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	Digital Dimming Duty	Remarks
0	0	0	0	0	0	0	0	0/255	—
0	0	0	0	0	0	0	1	1/255	—
0	0	0	0	0	0	1	0	2/255	—
⁞								⁞	⁞
0	0	0	1	0	0	0	0	16/255	—
0	0	0	1	0	0	0	1	17/255	—
0	0	0	1	0	0	1	0	18/255	—
⁞								⁞	⁞
1	0	0	0	0	0	0	0	128/255	—
1	0	0	0	0	0	0	1	129/255	—
1	0	0	0	0	0	1	0	130/255	—
⁞								⁞	⁞
1	1	1	1	1	1	0	0	252/255	—
1	1	1	1	1	1	0	1	253/255	—
1	1	1	1	1	1	1	0	254/255	—
1	1	1	1	1	1	1	1	255/255	Default

Note: The luminance = Maximum constant current ratio set values (I_{CA}) × Brightness Digital Dimming Duty (set by BC[7:0]), as shown in the accompanying diagram.



Mode Control

This command is used to control the thermal shutdown circuit and open/short detection functions.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Mode Control	W	0	0	1	1	1	0	0	0	38h
	W	TSDEN	TSDS	X	X	X	X	ODEN	SDEN	00h

TSDEN	TSDS	Temperature Protection SW	Control Mode	Remarks
0	X	OFF	—	Default
1	0	ON	User Control	Users read TSDF flag to control the display on/off
1	1	ON	Auto Control	Auto control the display on/off

ODEN	Open Detection Start	Remarks
0	OFF	Default
1	ON (Auto detect)	—

SDEN	Short Detection Start	Remarks
0	OFF	Default
1	ON (Auto detect)	—

Note: 1. If the TSDS bit is “1”, the Temperature protection function will enter Auto control mode:
- When the chip junction temperatures exceeds 150°C, the entire IC display will be off.
- When the chip junction temperatures falls below 125°C.The device will resume operation with a normal display.

2. If the TSDS bit is “0”, the Temperature protection function will enter user control mode:
- The TSDF flag bit will be read to determine if the IC display is off.
- When the chip junction temperatures exceeds 150°C, the TSDF flag bit is set to “1”.
- When the chip junction temperatures falls below 125°C, the TSDF flag bit is cleared to “0”.

3. Open/Short detection can be enabled through ODEN/SDEN bit setting.
Firstly use the constant current ratio command to set the LED current. It is recommended to use 9mA for this test.
And then enable the open/short detection. Lastly read the open/short detection data.
- Once the ODEN/SDEN is set high to enable the detection function, all other operation modes are ignored and the system starts to re-run the LED matrix for the LED open short detection.

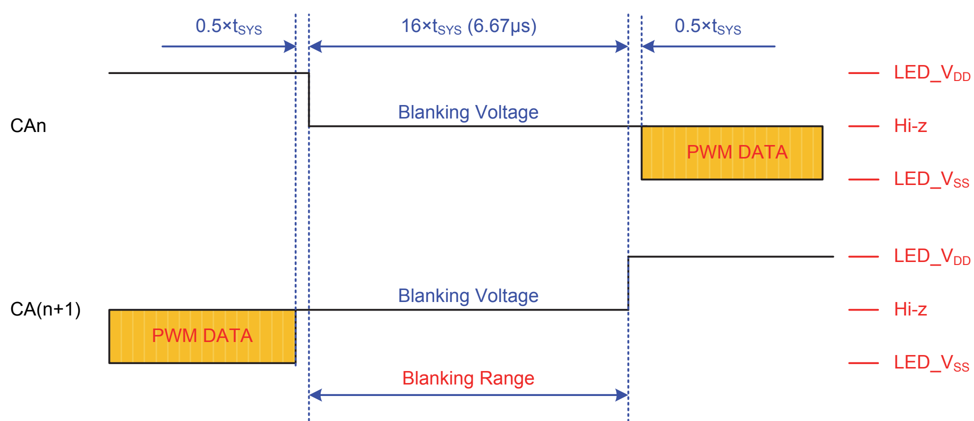
Blanking Control Voltage Setting

This command is used to control the blanking control voltage on/off function as well as setting the value of the blanking control voltage during the LED output blanking time.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Blanking Voltage Set	W	0	0	1	1	1	0	0	1	39h
	W	VBEN	X	X	X	VB3	VB2	VB1	VB0	0Fh

VBEN	Blanking Voltage Function SW	Remarks
0	OFF	Default
1	ON	—

VB3	VB2	VB1	VB0	Blanking Voltage (V)	Remarks
0	0	0	0	LED_VSS	—
0	0	0	1	$LED\_V_{DD} \times (1/15)$	—
0	0	1	0	$LED\_V_{DD} \times (2/15)$	—
0	0	1	1	$LED\_V_{DD} \times (3/15)$	—
0	1	0	0	$LED\_V_{DD} \times (4/15)$	—
0	1	0	1	$LED\_V_{DD} \times (5/15)$	—
0	1	1	0	$LED\_V_{DD} \times (6/15)$	—
0	1	1	1	$LED\_V_{DD} \times (7/15)$	—
1	0	0	0	$LED\_V_{DD} \times (8/15)$	—
1	0	0	1	$LED\_V_{DD} \times (9/15)$	—
1	0	1	0	$LED\_V_{DD} \times (10/15)$	—
1	0	1	1	$LED\_V_{DD} \times (11/15)$	—
1	1	0	0	$LED\_V_{DD} \times (12/15)$	—
1	1	0	1	$LED\_V_{DD} \times (13/15)$	—
1	1	1	0	$LED\_V_{DD} \times (14/15)$	—
1	1	1	1	LED_V_{DD}	Default



Read Open Detection Data

The read open detection data format is as below.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Read Open Detection Data	W	0	1	1	1	0	1	0	0	74h
	R	Dummy Data								00h
	R	Read Data								—

Note: Each dot Detect time is equal to the input CLK pulse time.

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
1st	0	1	1	1	0	1	0	0	74h
2nd	0	0	0	0	0	0	0	0	00h
3rd	C1-8	C1-7	C1-6	C1-5	C1-4	C1-3	C1-2	C1-1	00h
4th	C2-8	C2-7	C2-6	C2-5	C2-4	C2-3	C2-2	C2-1	00h
5th	C3-8	C3-7	C3-6	C3-5	C3-4	C3-3	C3-2	C3-1	00h
6th	C4-8	C4-7	C4-6	C4-5	C4-4	C4-3	C4-2	C4-1	00h
7th	C5-8	C5-7	C5-6	C5-5	C5-4	C5-3	C5-2	C5-1	00h
8th	C6-8	C6-7	C6-6	C6-5	C6-4	C6-3	C6-2	C6-1	00h
9th	C7-8	C7-7	C7-6	C7-5	C7-4	C7-3	C7-2	C7-1	00h
10th	C8-8	C8-7	C8-6	C8-5	C8-4	C8-3	C8-2	C8-1	00h
11th	C9-8	C9-7	C9-6	C9-5	C9-4	C9-3	C9-2	C9-1	00h

Read Short Detection Data

The read short detection data format is as below.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Read Short Detection Data	W	0	1	1	1	0	1	0	1	75h
	R	Dummy Data								00h
	R	Read Data								—

Note: Each dot Detect time is equal to the input CLK pulse time.

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
1st	0	1	1	1	0	1	0	0	74h
2nd	0	0	0	0	0	0	0	0	00h
3rd	C1-8	C1-7	C1-6	C1-5	C1-4	C1-3	C1-2	C1-1	00h
4th	C2-8	C2-7	C2-6	C2-5	C2-4	C2-3	C2-2	C2-1	00h
5th	C3-8	C3-7	C3-6	C3-5	C3-4	C3-3	C3-2	C3-1	00h
6th	C4-8	C4-7	C4-6	C4-5	C4-4	C4-3	C4-2	C4-1	00h
7th	C5-8	C5-7	C5-6	C5-5	C5-4	C5-3	C5-2	C5-1	00h
8th	C6-8	C6-7	C6-6	C6-5	C6-4	C6-3	C6-2	C6-1	00h
9th	C7-8	C7-7	C7-6	C7-5	C7-4	C7-3	C7-2	C7-1	00h
10th	C8-8	C8-7	C8-6	C8-5	C8-4	C8-3	C8-2	C8-1	00h
11th	C9-8	C9-7	C9-6	C9-5	C9-4	C9-3	C9-2	C9-1	00h

Read Register Status

The command can be used to obtain the device internal status. The read register status format is as below.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Read Status	W	0	1	1	1	0	0	0	0	70h
	R	Read Data								—

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description	Def.
—	0	1	1	1	0	0	0	0	Read Register Status Command	70h
1st	X	X	X	X	X	X	X	MP	Picture/Movie Display Mode	00h
2nd	BGS	X	X	X	X	X	X	X	Binary/Gray Mode	00h
3rd	FFEN	GMEN	GFEN	FOT	FET1	FET0	FLT1	FLT0	Fade Parameter Settings	4Ah
4th	GFS	X	X	X	X	GFT2	GFT1	GFT0	Global Fade Time	00h
5th	X	X	X	X	X	X	MS1	MS0	Master or Slave Mode	00h
6th	X	X	X	X	X	X	FON	DON	System Oscillator On/Off and Display On/Off Status	00h
7th	X	X	X	X	CC3	CC2	CC1	CC0	Constant Current Ratio	0Ah
8th	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	Luminance – 256 steps	FFh
9th	TSDEN	TSDS	X	X	X	X	ODEN	SDEN	Thermal Protection On/Off Open/Short Detection On/Off	00h
10th	VBEN	X	X	X	VB3	VB2	VB1	VB0	Blanking Voltage – 16 steps	00h
11th	SCEN	X	RL	HSP4	HSP3	HSP2	HSP1	HSP0	Scrolling Function Status	00h
12th	X	X	X	X	PFS3	PFS2	PFS1	PFS0	Picture Display First Address Setting	00h
13th	MEN	X	X	X	MFS3	MFS2	MFS1	MFS0	Movie Display First Address Setting	00h
14th	X	X	X	X	MFL3	MFL2	MFL1	MFL0	Movie Display Play Length Setting	01h
15th	X	X	X	X	MCT3	MCT2	MCT1	MCT0	Movie Display Play Cycle Time Setting	00h
16th	X	X	MPD5	MPD4	MPD3	MPD2	MPD1	MPD0	Delay Time between two pages in a movie	04h
17th	X	X	X	X	MLP3	MLP2	MLP1	MLP0	The Last Page in a movie	00h

Read Movie Frame Status

The read movie frame status format is as below.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Read Movie Frame Status	W	0	1	1	1	0	0	0	1	71h
	R	MOF1	MOF0	X	X	MDF3	MDF2	MDF1	MDF0	00h

MOF1	MOF0	Movie Operation Status	Remarks
0	X	No Movie	—
1	0	Movie is Playing	—
1	1	Movie is finished	—

MDF3	MDF2	MDF1	MDF0	RAM Page Address		Remarks
				Gray Mode	Binary Mode	
0	0	0	0	Page1	Page1	(Default)
0	0	0	1	Page2	Page2	—
0	0	1	0	—	Page3	—
0	0	1	1	—	Page4	—
0	1	0	0	—	Page5	—
0	1	0	1	—	Page6	—
0	1	1	0	—	Page7	—
0	1	1	1	—	Page8	—
1	0	0	0	—	Page9	—
1	0	0	1	—	Page10	—
1	0	1	0	—	Page11	—
1	0	1	1	—	Page12	—
1	1	0	0	—	Page13	—
1	1	0	1	—	Page14	—
1	1	1	0	—	Page15	—
1	1	1	1	—	Page16	—

Note: If programmed command data is not defined the function will not be affected.

Read Movie Loop Status

The read movie loop status format is as below.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Read Movie Loop Status	W	0	1	1	1	0	0	1	0	72h
	R	MOL1	MOL0	X	X	MLP3	MLP2	MLP1	MLP0	00h

MOL1	MOL0	Movie Operation Status	Remarks
0	X	No Movie	—
1	0	Loops are playing	—
1	1	Loop play is finished	—

MLP3	MLP2	MLP1	MLP0	Displayed Loop	Remarks
0	0	0	0	Loop1	—
0	0	0	1	Loop2	—
0	0	1	0	Loop3	—
0	0	1	1	Loop4	—
0	1	0	0	Loop5	—
0	1	0	1	Loop6	—
0	1	1	0	Loop7	—
0	1	1	1	Loop8	—
1	X	X	X	Endless	Display Loop1~loop8 repeatedly

Read Function Flag

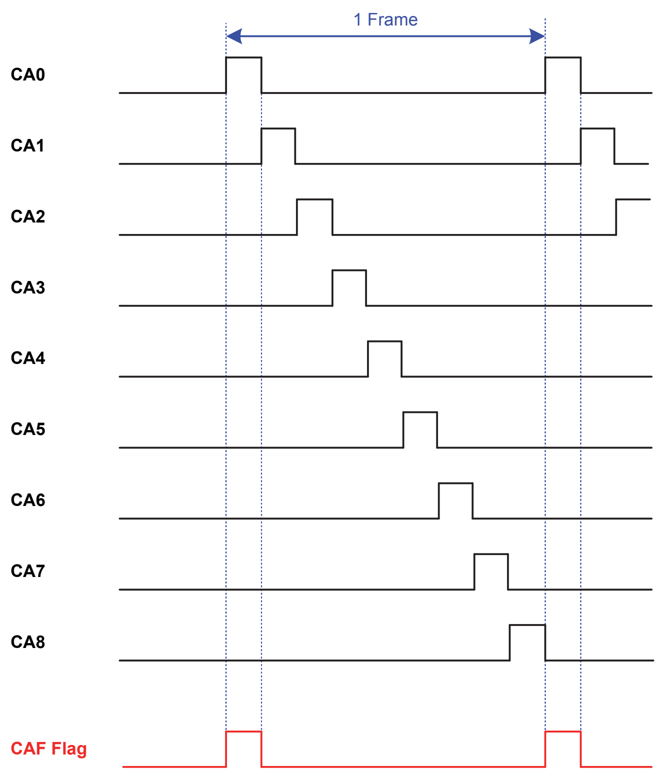
The read function flag format is as below.

Command	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Read Function Flag	W	0	1	1	1	0	0	1	1	73h
	R	CAF	X	X	X	X	X	X	TSDF	00h

CAF	Scanning Location	Remarks
0	Other CA	—
1	CA0	—

TSDF	Chip Junction Temperature	Remarks
0	< 125°C	Default When the chip junction temperature falls below 125°C, the TSDF flag bit is cleared to “0”.
1	> 150°C	When the chip junction temperature exceeds 150°C, the TSDF flag bit is set to “1”.

The relationship between the CA0 scanning location and CAF flag is shown as follows.



SPI 3-wire Serial Interface

The HT16D31A device includes an SPI 3-wire serial interface.

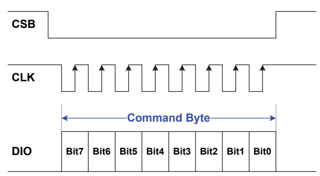
The CSB pin is used to identify the transmitted data. The transmission is controlled by the active low signal CSB, After the CSB falls to a low level, the data can start to be transferred. The data is transferred from the MSB of each byte (MSB First), and the data is shifted into a register at the rising edge of CLK. The input data is automatically loaded into a register for every 8 bits of input data. The sequence starts from the falling edge of the CSB signal.

For the read mode, when CSB is low the DIO pin will change into an output mode after sending a read command code and the start read address setup value. If the MCU sets the CSB signal to a high level after receiving the output data, the DIO pin will be changed into an input mode and the read mode cycle will terminate. For the read mode, the data is outputted from DIO pin at falling edge of CLK.

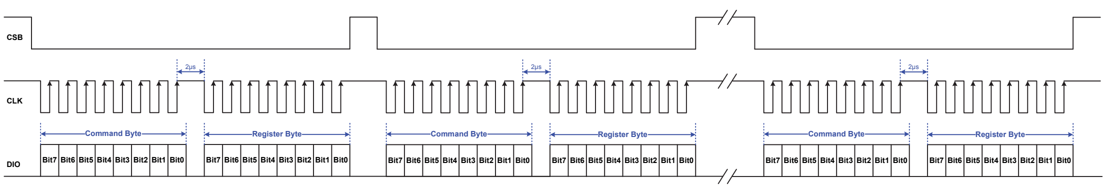
Write Operation

Command Byte Transfer

• Single Command Byte

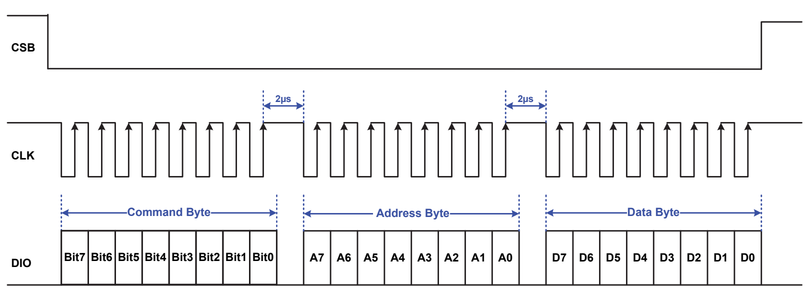


• Compound Command Byte



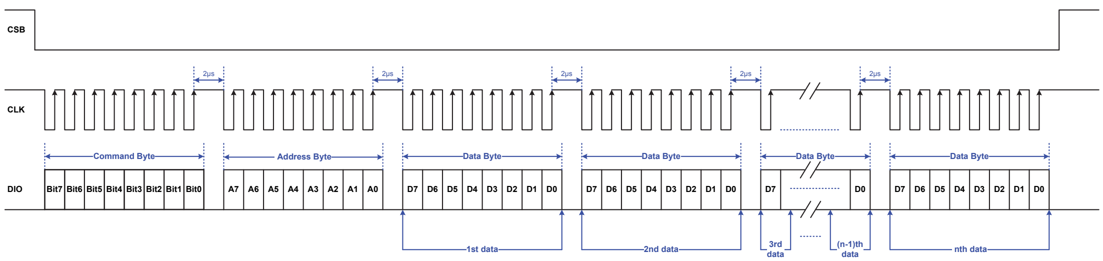
Data Byte Transfer

• Single Write RAM Data Operation



Note: If the input memory location value is greater than the limit value, the input memory location value will be invalid.

• **Pages Write RAM Data Operation**



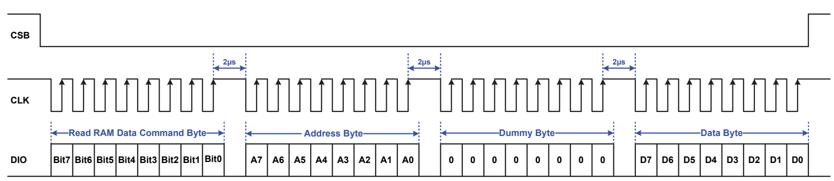
Note: If the memory location exceeds the limit value, the memory pointer will return to 00H. The Memory location limit values are shown as below.

Mode	Memory Location Limit Value		
	Display Data	Fade Data	LED On/Off Control
Binary	08h	No support function	
Gray	87h	83h	08h

Read Operation

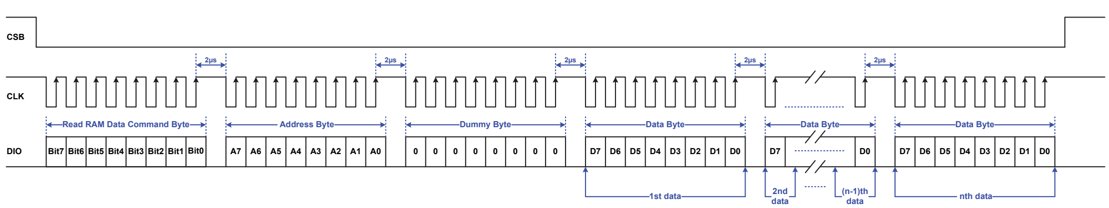
1. The data must be read in byte units.
2. It is recommended that the host controller should read in the data from the DIO line between the rising edge of the CLK line and the falling edge of the next CLK line.

• **Single Read RAM Data Operation**



Note: If the input memory location value is greater than the limit value, the input memory location value will be invalid.

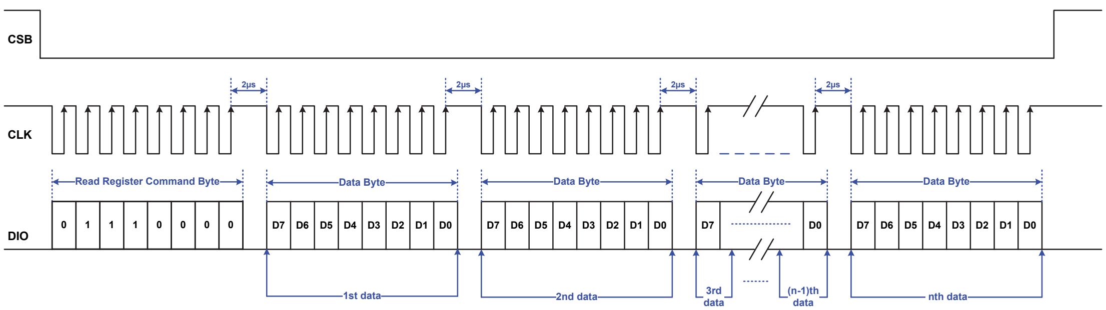
• **Page Read RAM Data Operation**



Note: If the memory location exceeds the limit value, the memory pointer will return to 00H. The Memory location limit values are shown as below.

Mode	Memory Location Limit Value		
	Display Data	Fade Data	LED On/Off Control
Binary	08h	No support function	
Gray	87h	83h	08h

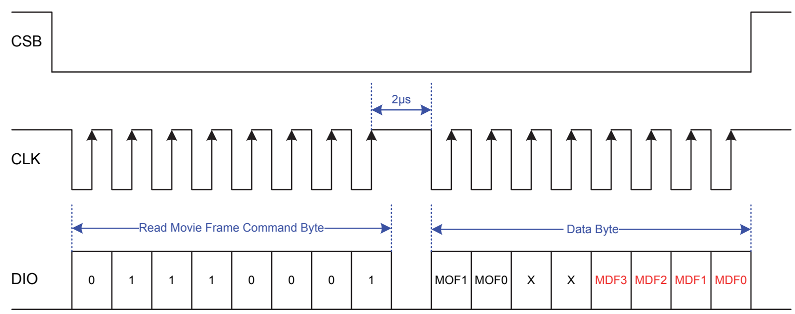
• **Read Register Status**



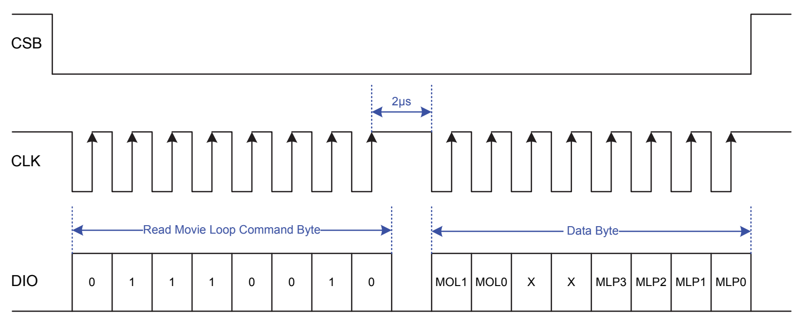
Note: 1. The display data must be read in byte units.

2. If the register location exceeds the limit value, the register pointer will return to the first address. The register location has a limit value of 20.

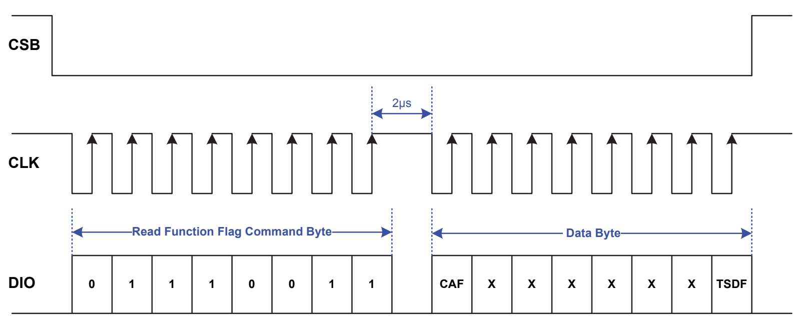
• **Read Movie Frame Status**



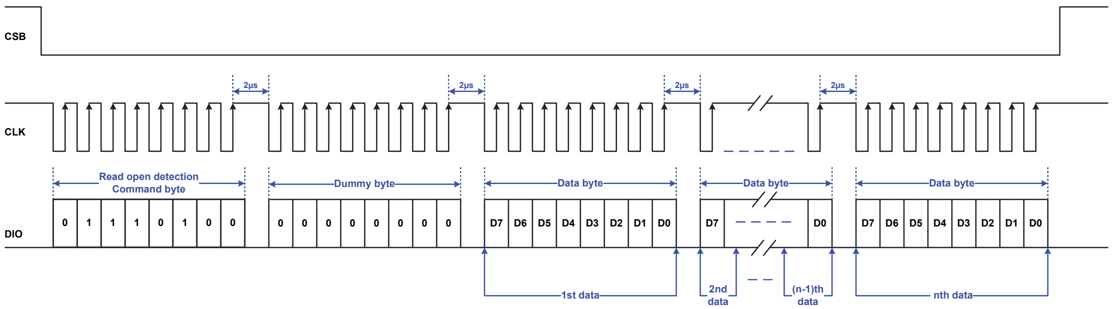
• **Read Movie Loop Status**



• **Read Function Flag**



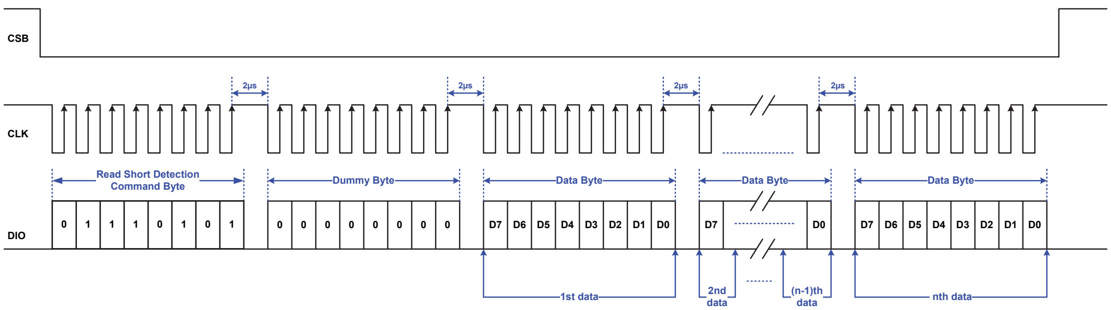
- **Read Open Detection Data**



Note: 1. The display data must be read in byte units.

2. If the register location exceeds the limit value, the register pointer will return to the first address. The register location has a limit value of 09th address.

- **Read Short Detection Data**



Note: 1. The display data must be read in byte units.

2. If the register location exceeds the limit value, the register pointer will return to the first address. The register location has a limit value of 09th address.

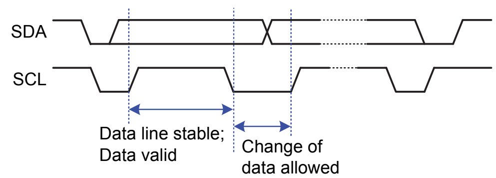
I²C Serial Interface

The HT16D31B device includes an I²C serial interface.

The I²C bus is a bidirectional two-line communication link between different ICs or modules. The two lines of the interface are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to the positive supply via a pull-up resistor, typically a value of 10kΩ for a frequency of 100kHz. When the bus is free both lines will be high. The output stages of devices connected to the bus must have open-drain or open-collector output types to implement the wired-AND function necessary for connection. Data transfer is initiated only when the bus is not busy.

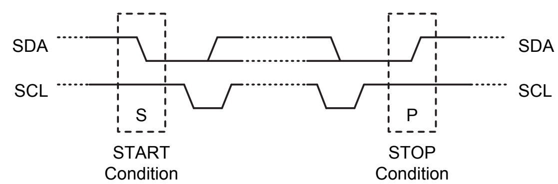
Data Validity

The data on the SDA line must be stable during the clock high period. The high or low state of the data line can only change when the clock signal on the SCL line is low as shown in the accompanying diagram.



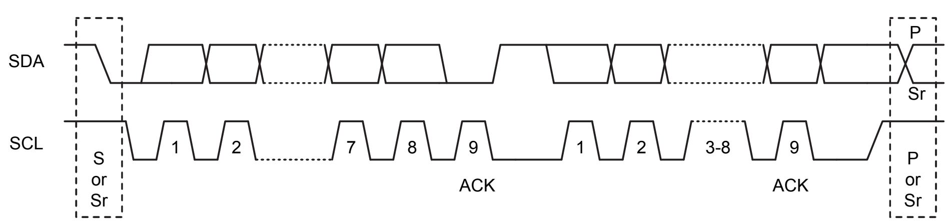
START and STOP Conditions

- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus remains busy if a repeated START (Sr) is generated instead of a STOP condition. The START(S) and repeated START (Sr) conditions are functionally identical.



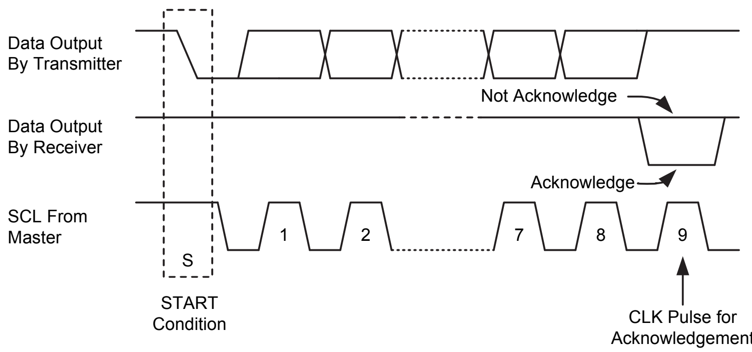
Byte Format

Every byte put on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.



Acknowledge

- Each byte of eight bit length is followed by one acknowledge bit. This acknowledges bit is a low level placed on the bus by the receiver. The master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an Acknowledge, ACK, after the reception of each byte.
- The device that provides an Acknowledge must pull down the SDA line during the acknowledge clock pulse so that it remains at a stable low level during the high period of this clock pulse.
- A master receiver must signal an end of data to the slave by generating a not-acknowledge, NACK, bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse so as to not acknowledge. The master will generate a STOP or a repeated START condition.



Slave Addressing

- The device requires an 8-bit slave address word following a start condition to enable the device for a write operation. The device address word consist of a mandatory one, zero sequence for the first four most significant bits. Refer to the diagram showing the slave Address. This is common to all LED devices.
- The slave address byte is the first byte received following the START condition from the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines whether a read or write operation is to be performed. When the R/W bit is "1", then a read operation is selected. A "0" selects a write operation.
- The address bits are "1, 1, 0, 1, 1, A1, A0". When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an Acknowledge on the SDA line.

Slave Address

MSB — LSB

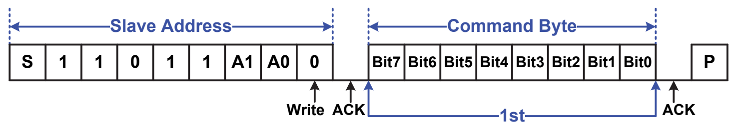
1	1	0	1	1	A1	A0	R/W

Note: 1. When the AD pin is connected to V_{SS} (GND), the [A1,A0] bits should be set to [0,0]
2. When the AD pin is connected to V_{DD}, the [A1,A0] bits should be set to [1,1]
3. When the AD pin is connected to the SCL, the [A1,A0] bits should be set to [0,1]
4. When the AD pin is connected to the SDA, the [A1,A0] bits should be set to [1,0]
5. Common address that all devices are responding on the slave address bits are "0,1,0,1,1,1,0"

Write Operation

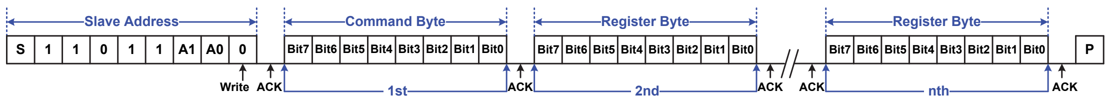
• Single Command Byte

A command byte write operation requires a START condition, a slave address with an R/W bit, a command (1st) and a STOP condition.



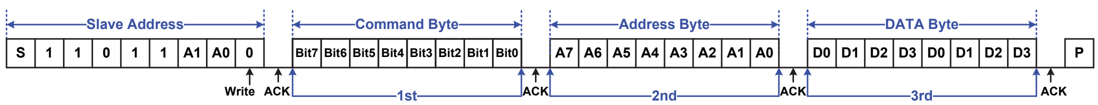
• Compound Command Byte

A byte write operation requires a START condition, a slave address with an R/W bit, a command (1st), one or more register byte commands (2nd~nth) and a STOP condition for compound command byte.



• Single Write RAM Data Byte Operation

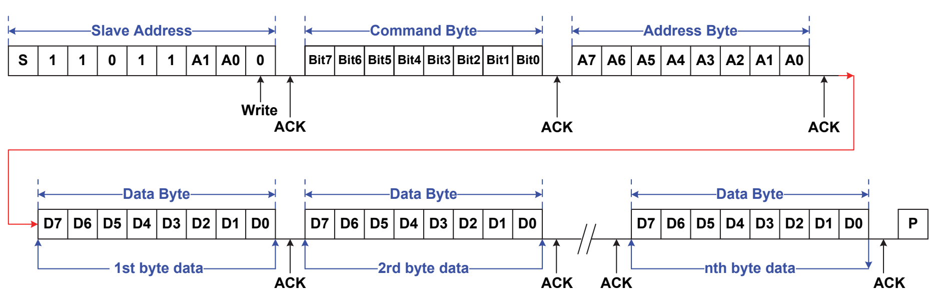
Following a START condition, the slave address with R/W bit is placed on the bus. Then follows the display data address setup command code (1st). The address point (An) is then written to the address pointer (2nd) and then valid data and a STOP condition for a compound write single data byte.



Note: If the input memory location value is greater than the limit value, the input memory location value will be invalid.

• Page Write RAM Data Operation

Following a START condition, the slave address with R/W bit is placed on the bus along with the display data address setup command code (1st) and the address point, An, (2nd). The data to be written to the memory is next, after which the internal address pointer is incremented to the next address location on the reception of an acknowledge clock.



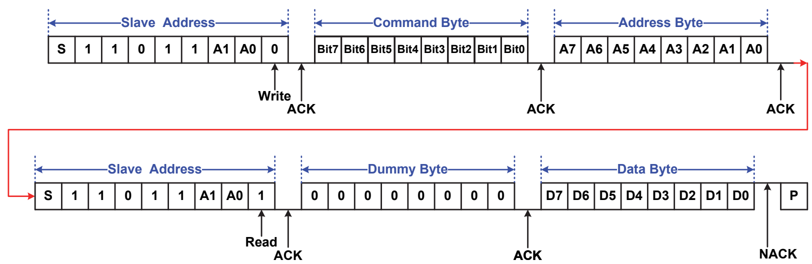
If memory location exceeds limit value, the memory pointer will return to 00H. The Memory location limit values are shown as below:

Mode	Memory Location Limit Value		
	Display Data	Fade Data	LED on/off Control
Binary	08h	No support function	
Gray	87h	83h	08h

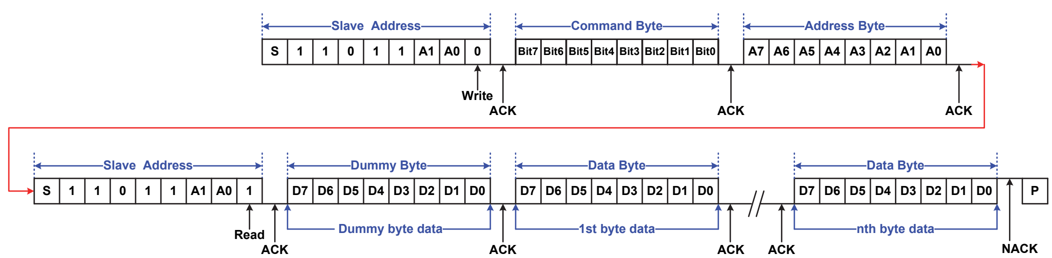
Read Operation

In this mode, the master reads the device data after setting the slave address. Following the R/W bit (="0"), and the acknowledge bit, then follows the address setting command code (1st). After this is the address pointer (An) which is written to the address pointer (2nd). Next come the START condition and slave address, followed by an R/W bit (="1"). The addressed data is then transmitted. The address pointer is only incremented on reception of an acknowledge clock. The device will place the data at address An+1 onto the bus. The master reads and acknowledges the new byte and the address pointer is incremented to "An+2". If only a read command is sent to the I²C interface, then dummy data is transmitted. This cycle for reading consecutive addresses will continue until the master sends a NACK and STOP condition.

• Single Read RAM Data Operation



• Page Read RAM Data Operation



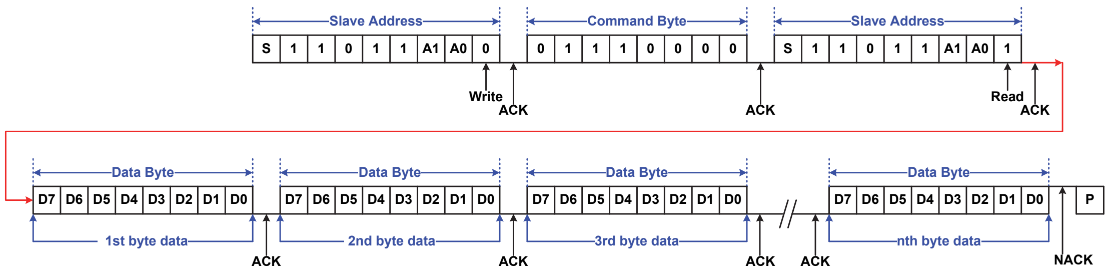
Note: 1. The cycle to read consecutive addresses will continue until the master sends a NACK and STOP condition.

2. If memory location exceeds limit value, the memory pointer will return to 00H. The Memory location limit values are shown as below:

Mode	Memory Location Limit Value		
	Display Data	Fade Data	LED On/Off Control
Binary	08h	No support function	
Gray	87h	83h	08h

Read Register Status

In this mode, the master reads the device data after setting the slave address. Following the R/W bit (= “0”), and the acknowledge bit, then follows the Read Register Status command code. Next is the START condition and slave address, followed by an R/W bit (= “1”). The addressed data is then transmitted.

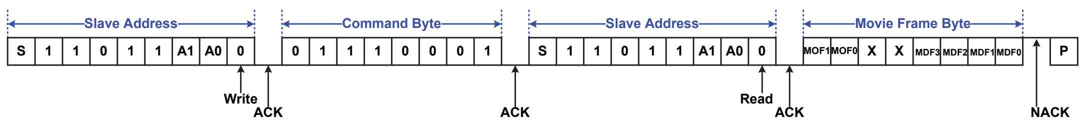


Note: 1. If the register location exceeds the limit value, the register pointer will return to the 1st. The register location limit value is 20th address.

2. The cycle to read consecutive addresses will continue until the master sends a NACK and STOP condition.

Read Movie Frame status

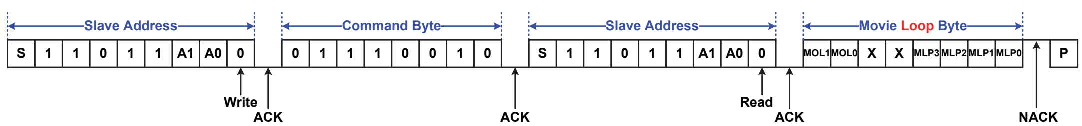
In this mode, the master reads the device data after setting the slave address. Following the R/W bit (= “0”), and the acknowledge bit, then follows the Read Movie Frame Status command code. Next is the START condition and slave address, followed by an R/W bit (= “1”). The addressed data is then transmitted.



Note: The cycle to read consecutive addresses will continue until the master sends a NACK and STOP condition.

Read Movie Loop Status

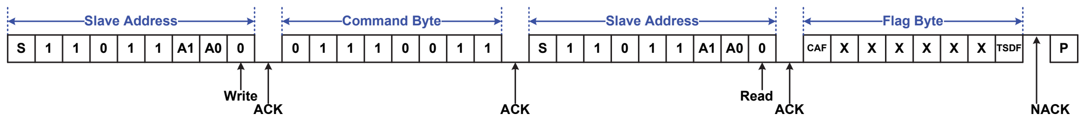
In this mode, the master reads the device data after setting the slave address. Following the R/W bit (= “0”), and the acknowledge bit, then follows the Read Movie Loop Status command code. Next is the START condition and slave address, followed by an R/W bit (= “1”). The addressed data is then transmitted.



Note: The cycle to read consecutive addresses will continue until the master sends a NACK and STOP condition.

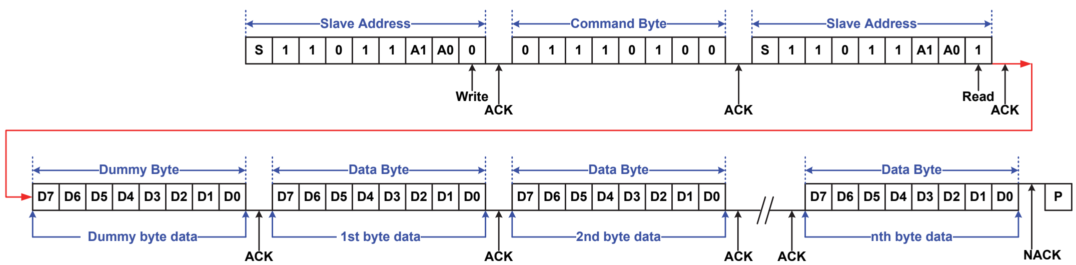
Read Function Flag

In this mode, the master reads the device data after setting the slave address. Following the R/W bit (="0"), and the acknowledge bit, then follows the Read Function Flag command code. Next is the START condition and slave address, followed by an R/W bit (="1"). The addressed data is then transmitted.



Note: The cycle to read consecutive addresses will continue until the master sends a NACK and STOP condition.

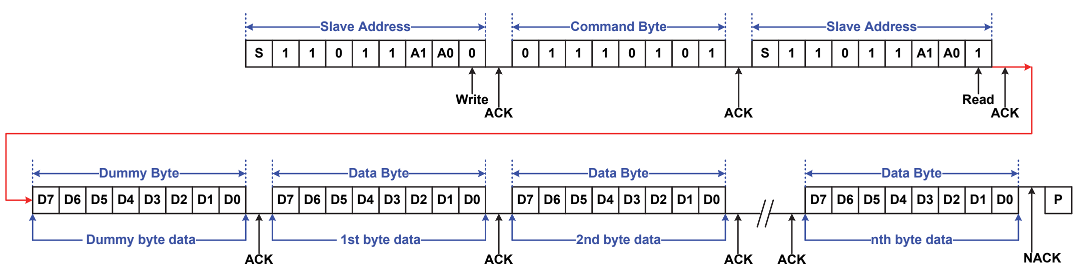
Read Open Detection Data



Note: 1. The display data must be read in byte units.

2. If the register location exceeds the limit value, the register pointer will return to the first address. The register location has a limit value of 09th address.

Read Short Detection Data



Note: 1. The display data must be read in byte units.

2. If the register location exceeds the limit value, the register pointer will return to the first address. The register location has a limit value of 09th address.

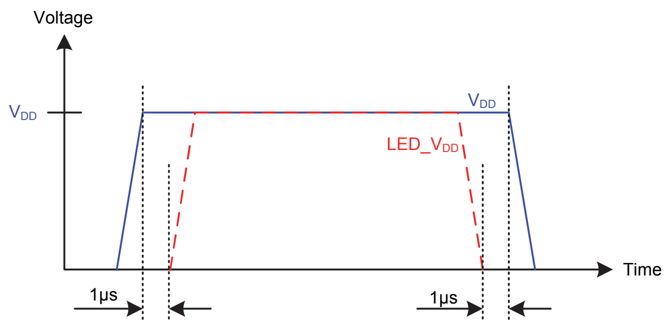
Power Supply Sequence

- If the power is individually supplied on the LED_VDD and VDD pins, it is strongly recommended to follow the Holtek power supply sequence requirement.
- If the power supply sequence requirement is not followed, it may result in malfunction.

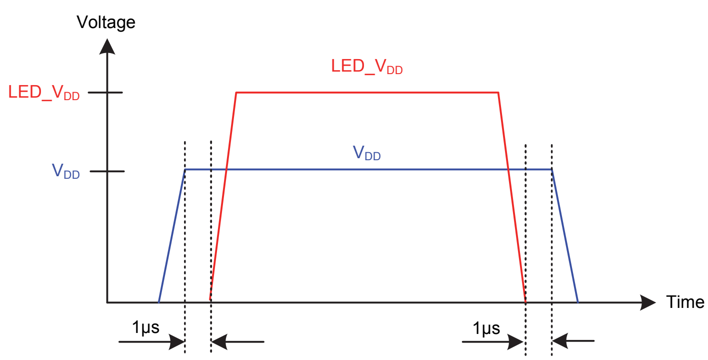
Holtek Power Supply Sequence Requirement.

1. Power-on sequence:
   Turn on the logic power supply V_{DD} first and then turn on the LED driver power supply LED_V_{DD}.
2. Power-off sequence:
   Turn off the LED driver power supply LED_V_{DD}. First and then turn off the logic power supply V_{DD}.
3. The Holtek Power Supply Sequence Requirement must be followed no matter whether the LED_V_{DD} voltage is higher than the V_{DD} voltage.

- When the LED_V_{DD} voltage is equal to V_{DD} voltage application:



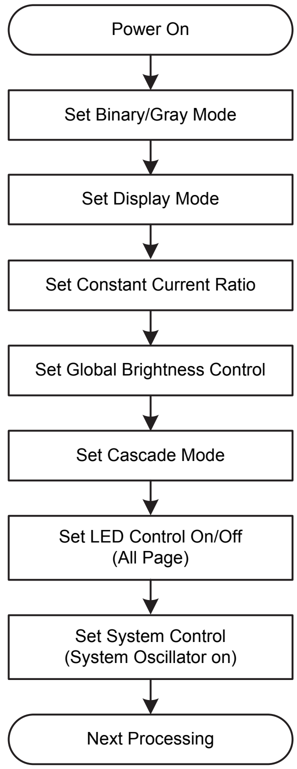
- When the LED_V_{DD} voltage is greater than the V_{DD} voltage application



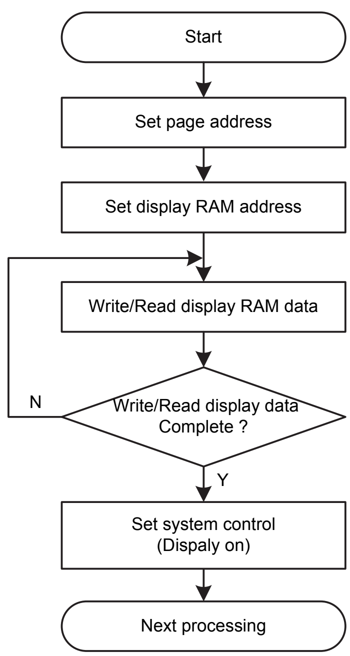
Operation Flow Charts

Access procedures are illustrated below by means of flowcharts.

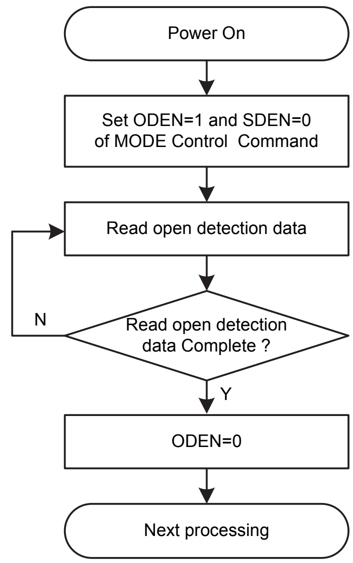
• Initialisation



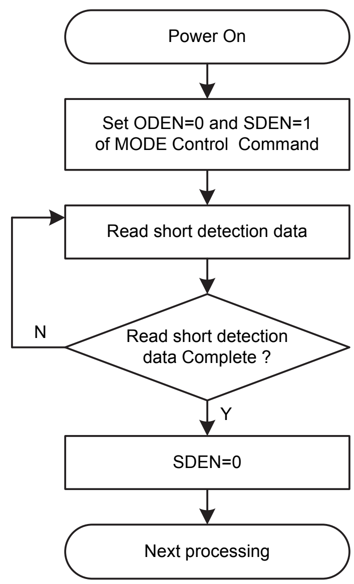
• Display Data Read/Write – Address Setting



• **Open Detection flow chart**

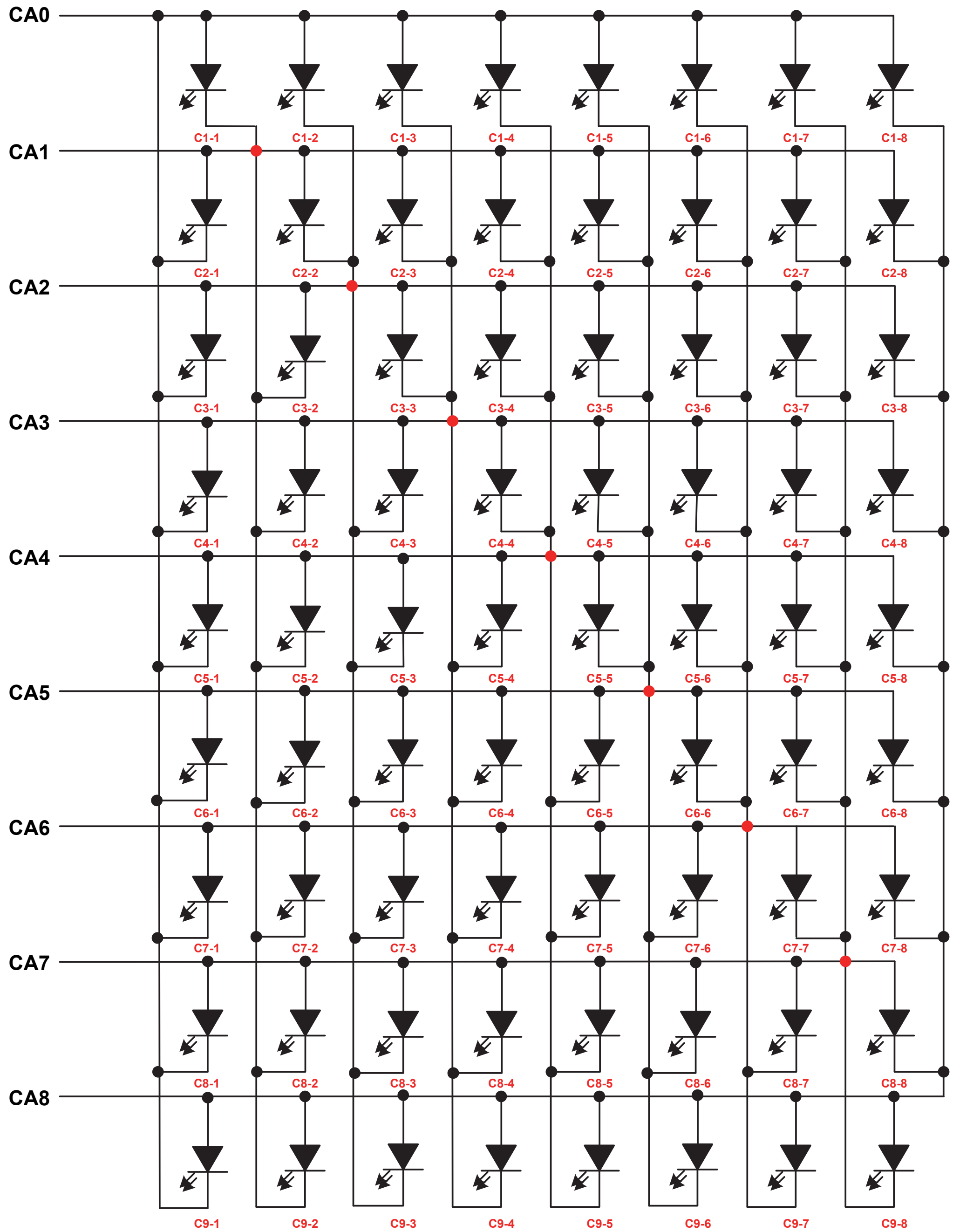


• **Short Detection flow chart**

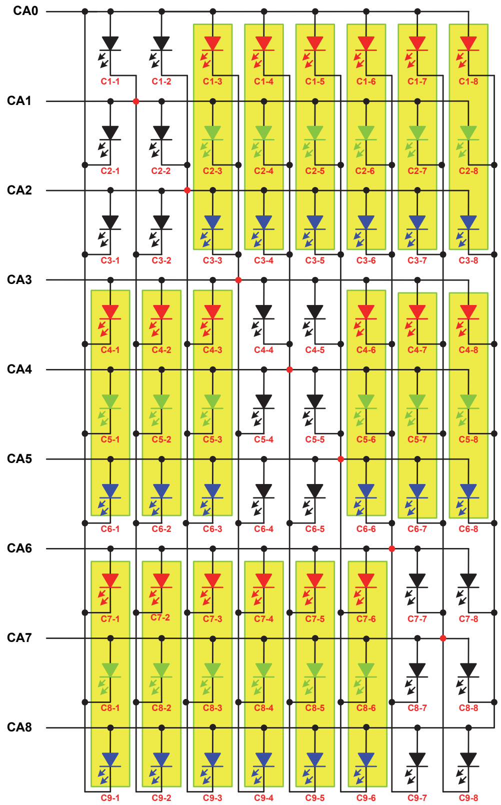


Application Circuits

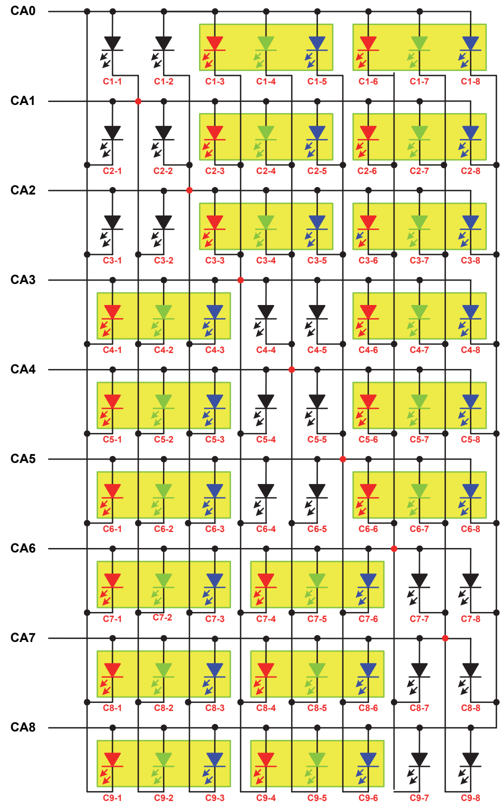
LED Matrix Circuit



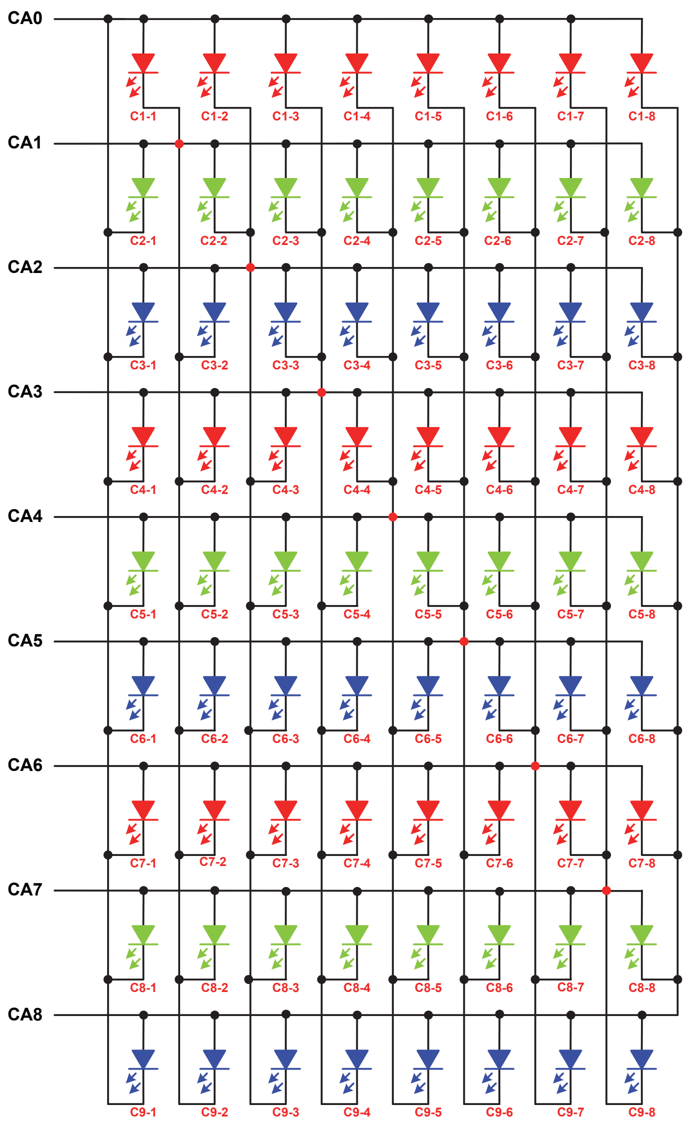
RGB LED Matrix Circuit



Common Cathode RGBs Connection

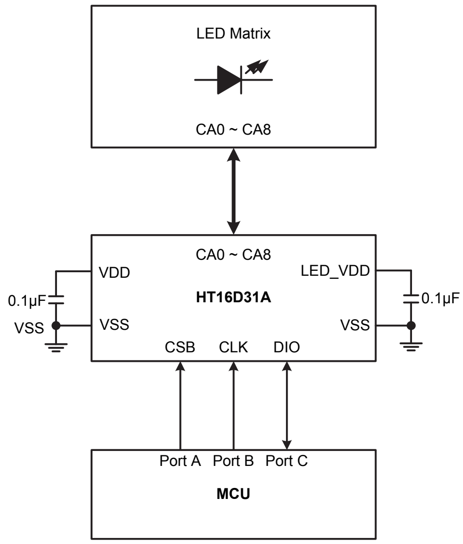


Common Anode RGBs Connection

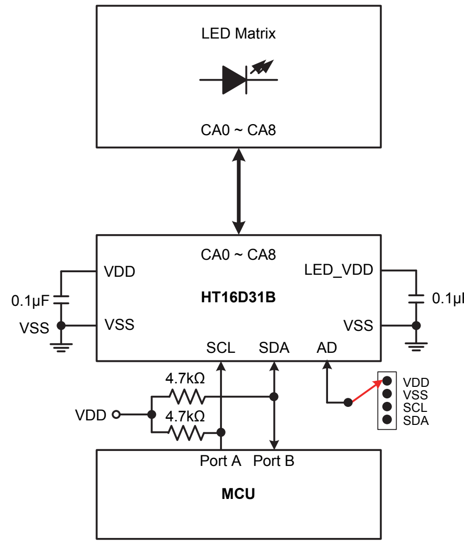


Respective RGBs Connection

Single LED IC Application



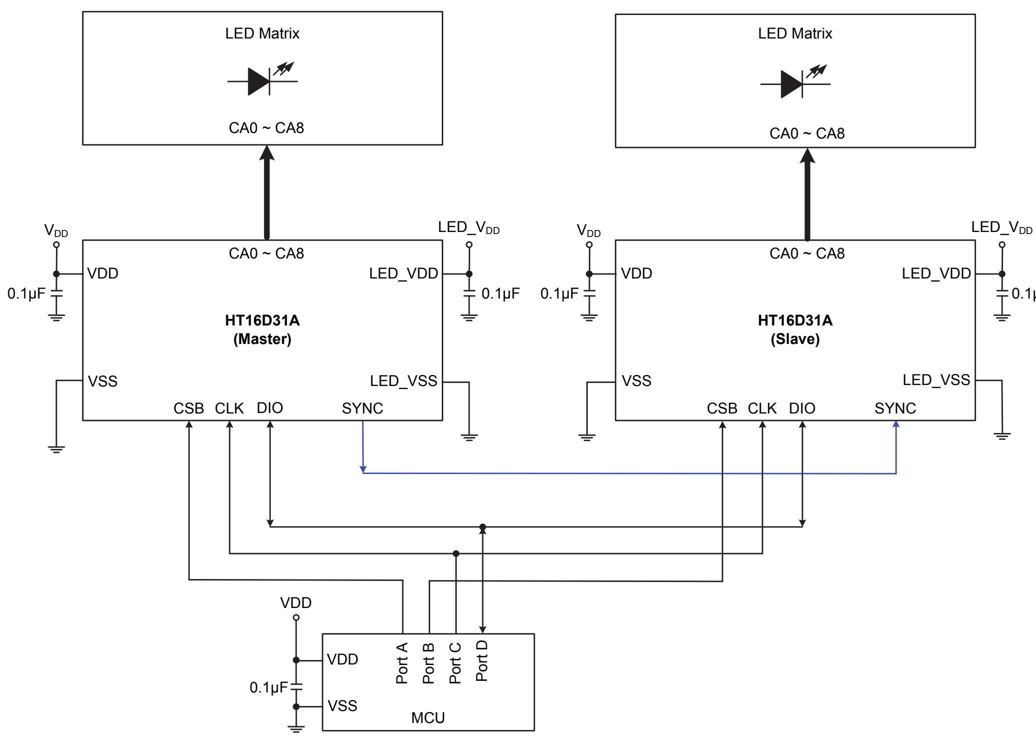
3-wire Serial Bus



I^2C Serial Bus

Cascade Function

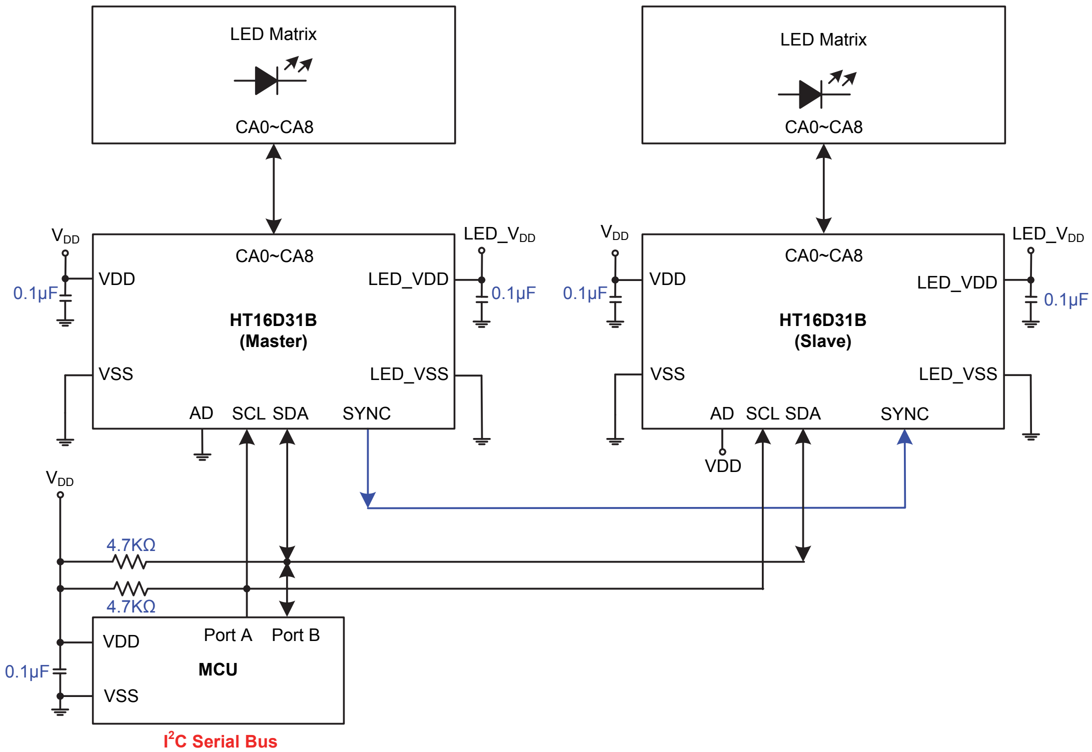
LED Application Example – SPI 3-wire Serial Bus



3-Wire Serial Bus

Note: Cascading can also be implemented using software. Users must set the Master in the master mode and the Slave in the slave mode using commands. The CSB pin must be connected to the MCU individually for independent read and write.

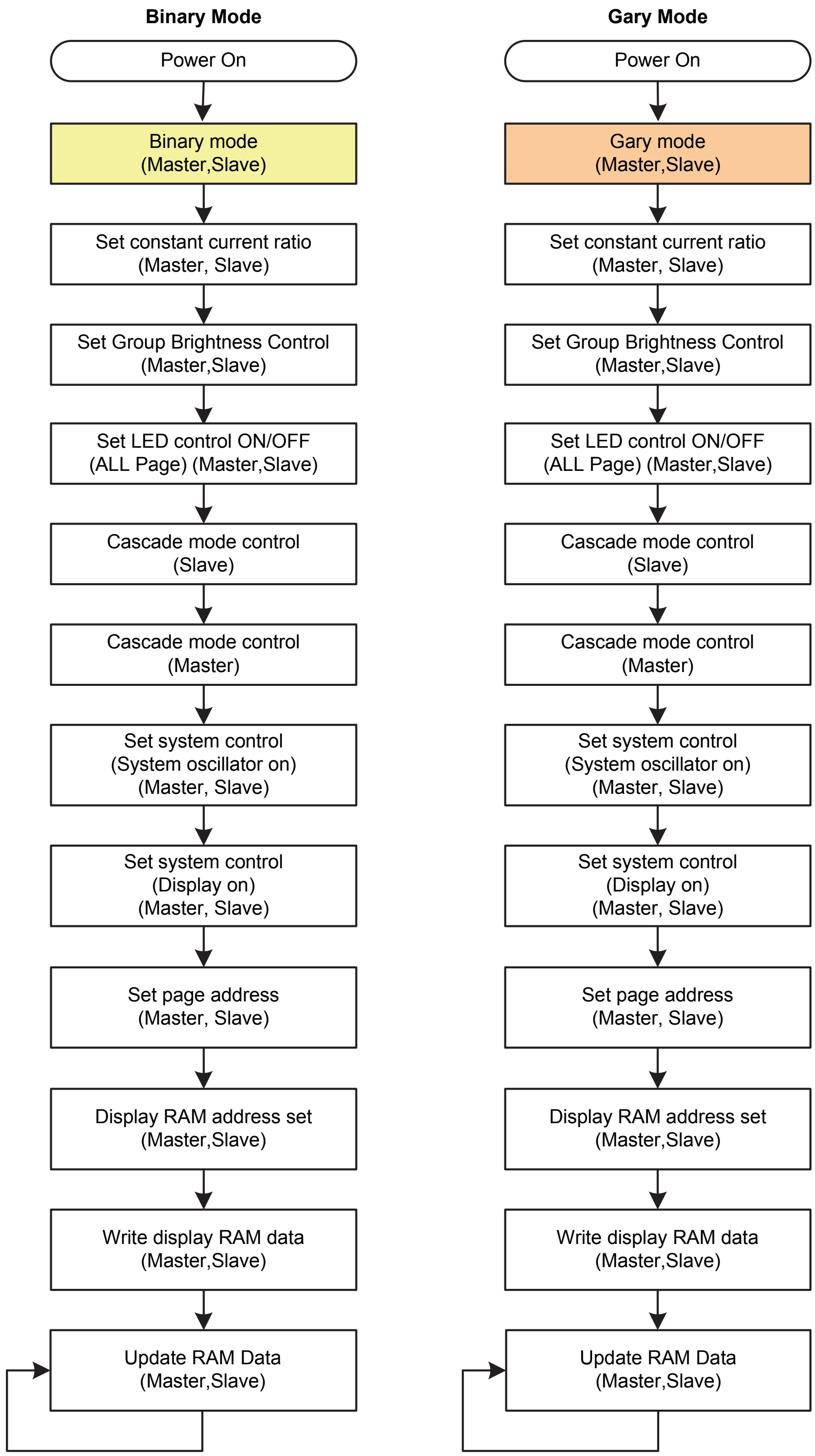
LED Application Example – I²C Serial Bus



Note: Cascading can also be implemented using software. Users must set the Master in the master mode and the Slave in the slave mode using commands. The CSB pin must be connected to the MCU individually for independent read and write.

Cascade Control Flow

Access procedures are illustrated below using flowcharts.



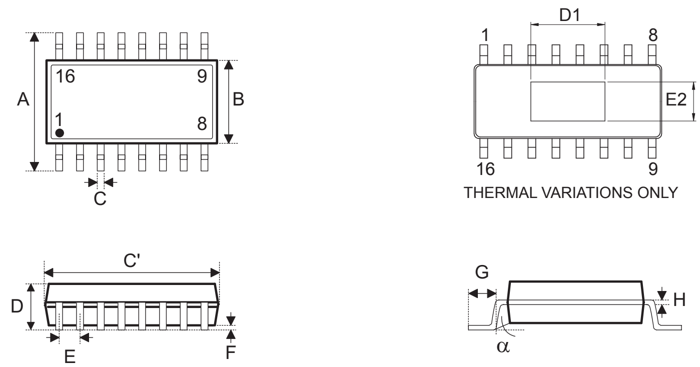
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

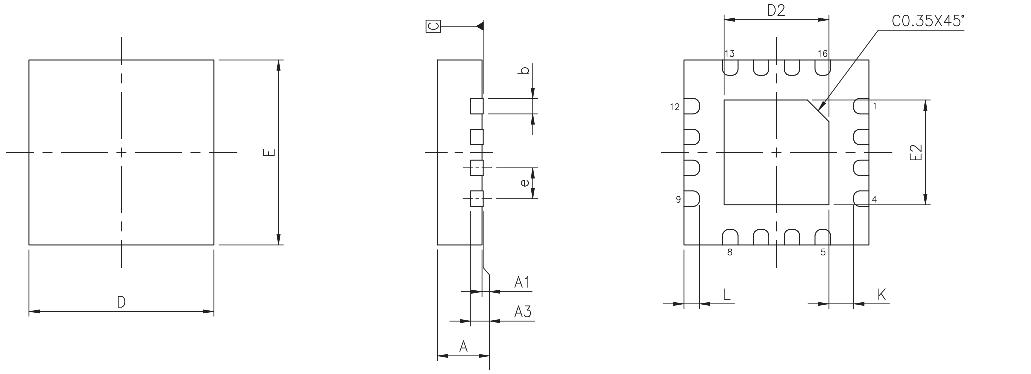
16-pin NSOP-EP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
D1	0.059	—	—
E2	0.039	—	—
C	0.012	—	0.020
C’	—	0.390 BSC	—
D	—	—	0.069
E	—	0.050 BSC	—
F	0.000	—	0.006
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.00 BSC	—
B	—	3.90 BSC	—
D1	1.50	—	—
E2	1.00	—	—
C	0.31	—	0.51
C’	—	9.90 BSC	—
D	—	—	1.75
E	—	1.27 BSC	—
F	0.00	—	0.15
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°

SAW Type 16-pin QFN (3mm×3mm for FP0.25mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.007	0.010	0.012
D	—	0.118 BSC	—
E	—	0.118 BSC	—
e	—	0.020 BSC	—
D2	0.063	0.067	0.069
E2	0.063	0.067	0.069
L	0.008	0.010	0.012
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A3	—	0.200 BSC	—
b	0.180	0.250	0.300
D	—	3.000 BSC	—
E	—	3.000 BSC	—
e	—	0.50 BSC	—
D2	1.60	1.70	1.75
E2	1.60	1.70	1.75
L	0.20	0.25	0.30
K	0.20	—	—