HT16512
1/4 to 1/11 Duty VFD Controller

Features

- Logic voltage: 3.0V~5.5V
- High-voltage output: V_{DD}–35V max.
- Multiple display (11-segment & 11-digit to 16-segment & 6-digit)
- 6×4 matrix key scanning
- 8 steps dimmer circuit
- 4 LED output ports
- 4-bit general purpose input port
- No external resistors necessary for driver output (provides PMOS open-drain and pull-low resistor output)
- Serial interface with MCU (CLK, $\overline{CS}$, DI, DO)
- 44-pin LQFP package

Applications

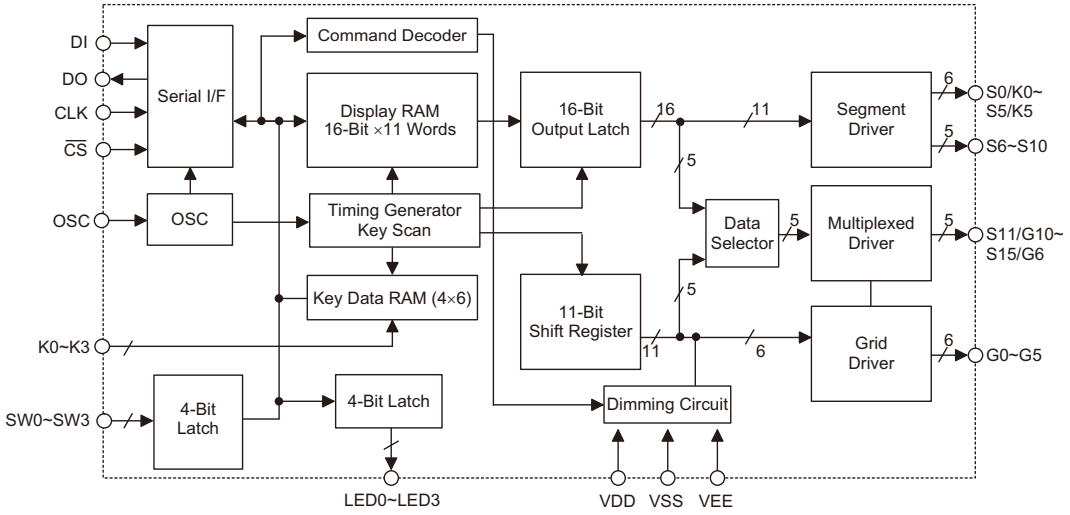
- Consumer products panel function control
- Industrial measuring instrument panel function control
- Other similar application panel function control

General Description

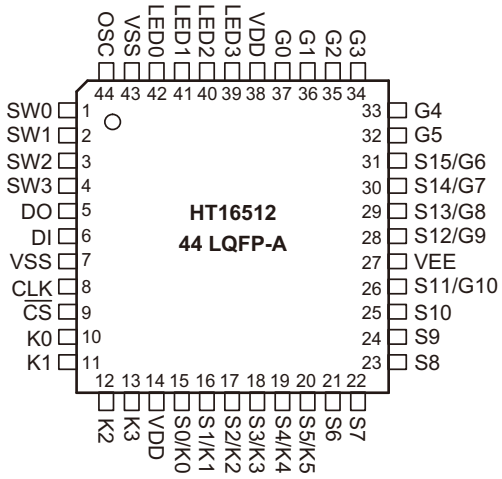
HT16512 is a VFD (Vacuum Fluorescent Display) controller/driver that is driven on a 1/4 to 1/11 duty factor. It consists of 11 segment output lines, 6 grid output lines, 5 segment/grid output drive lines, 4 LED output ports, a control circuit, a display memory, and a key scan circuit.

Serial data inputs to the HT16512 through a three-line serial interface. This VFD controller/driver is ideal as a peripheral device for an MCU.

Block Diagram



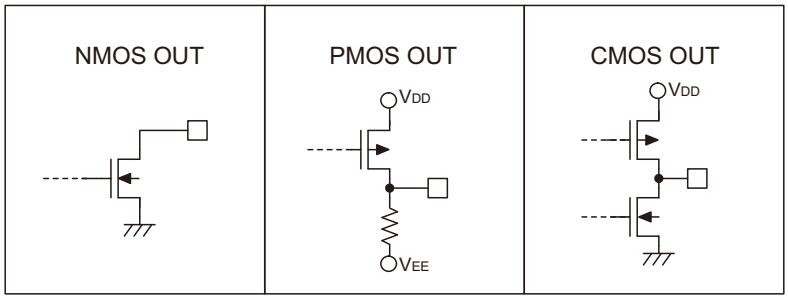
Pin Assignment



Pin Description

Pin No.	Pin Name	I/O	Description
1~4	SW0~SW3	I	4-bit general purpose input port Whether these pins are used or not, they should be connected to VDD or VSS.
5	DO	O	Output serial data at the falling edge of the shift clock, starting from low order bit. This is an NMOS open-drain output pin.
6	DI	I	Input serial data at the rising edge of the shift clock, starting from the low order bit.
7, 43	VSS	—	Negative power supply, ground Both of the VSS (pin 7 and pin 43) should be connected to ground.
8	CLK	I	Reads serial data at the rising edge, and outputs data at the falling edge.
9	$\overline{CS}$	I	Initializes serial interface at the rising or falling edge of the HT16512. Then it waits to receive a command. Data input after $\overline{CS}$ has fallen is processed as a command. While command data is processed, current processing is stopped, and the serial interface is initialized. While $\overline{CS}$ is high, CLK is ignored.
10~13	K0~K3	I	Keying data input to these pins is latched at the end of the display cycle.
14, 38	VDD	—	Posistive power supply
15~20	S0/K0~S5/K5	O	Segment or key source output pins (dual function). This is PMOS open-drain and pull-low resistor output.
21~25	S6~S10	O	Segment driver output pins (segment only). This is PMOS open-drain and pull-low resistor output.
26, 28~31	S11/G10~S15/G6	O	Segment or Grid driver output pins. These pins are selectable for segment or grid driving. This is PMOS open-drain and pull-low resistor output.
27	VEE	—	VFD power supply
37~32	G0~G5	O	Grid driver output pins (Grid only). This is PMOS open-drain and pull-low resistor output.
42~39	LED0~LED3	O	LED driver output ports. This is a CMOS output pin.
44	OSC	I	Connected to an external resistor or an RC oscillator circuit.

Approximate Internal Connections



Absolute Maximum Ratings

Supply Voltage ..... V_{SS}–0.3V to V_{SS}+5.5V

Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3V

Operating Temperature ..... –25°C to 75°C

Storage Temperature ..... –50°C to 125°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Logic Supply Voltage	3.3V	—	3.0	3.3	3.6	V
		5.0V		4.5	5.0	5.5	V
V_{EE}	VFD Supply Voltage	—	—	0	—	V_{DD}–35	V
f_{OSC}	Oscillation Frequency	3.3V	R_{OSC}=51kΩ	480	565	650	kHz
		5.0V		465	545	630	kHz
R_{PL}	Output Pull-low Resistor	3.3V	Driver output	50	100	150	kΩ
		5.0V					
I_{DD}	Operating Current	3.3V	No load, VFD display off	—	—	3	mA
		5.0V		—	—	5	mA
I_{OL}	Driver Leakage Current	3.3V	V_O=V_{DD}–35V, VFD driver off	—	—	–5	μA
		5.0V		—	—	–10	μA
I_{OL1}	LED Sink Current	3.3V	V_{OL}=1V, LED0~LED3	10	—	—	mA
		5.0V		20	—	—	mA
I_{OH1}	LED Source Current	3.3V	V_{OH}=0.9V_{DD} LED0~LED3	–0.5	—	—	mA
		5.0V		–1.0	—	—	mA
I_{OH21}	Segment/Key Source Current	3.3V	V_{OH}=V_{DD}–2V S0/K0~S5/K5, S6~S10	–1.5	—	—	mA
		5.0V		–3.0	—	—	mA
I_{OH22}	Segment/Grid Source Current	3.3V	V_{OH}=V_{DD}–2V G0~G5, S11/G10~S15/G6	–7.5	—	—	mA
		5.0V		–15.0	—	—	mA
I_{OL3}	DO Sink Current	3.3V	V_{OL}=0.4V	2	—	—	mA
		5.0V		4	—	—	mA

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{IH}	"H" Input Voltage	—	—	$0.7V_{DD}$	—	V_{DD}	V
V_{IL}	"L" Input Voltage	—	—	0	—	$0.3V_{DD}$	V
V_{OH1}	High-level Output Voltage	3.3V	LED0~LED3, I_{OH1}=–0.5mA	$0.9V_{DD}$	—	V_{DD}	V
		5.0V	LED0~LED3, I_{OH1}=–1mA				
V_{OL1}	Low-level Output Voltage	3.3V	LED0~LED3, I_{OL1}=10mA	0	—	1	V
		5.0V	LED0~LED3, I_{OL1}=20mA				
V_{OL2}	Low-level Output Voltage	3.3V	DO, I_{OL2}=2mA	0	—	0.4	V
		5.0V	DO, I_{OL2}=4mA				

A.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_{PHL}	Propagation Delay Time	3.3V	CLK→DO C_L=15pF, R_L=10kΩ	—	—	200	ns
		5.0V		—	—	100	ns
t_{PLH}		3.3V		—	—	600	ns
		5.0V		—	—	300	ns
t_{r1}	Rise Time	3.3V	C_L=300pF, S0~S10	—	—	4.0	μs
		5.0V		—	—	2.0	μs
t_{r2}		3.3V	C_L=300pF, G0~G5, S11/G10~S15/G6	—	—	1.0	μs
		5.0V		—	—	0.5	μs
t_f	Fall Time	3.3V	C_L=300pF, Sn, Gn	—	—	240	μs
		5.0V		—	—	120	μs
f_{max}	Maximum Clock Frequency	3.3V	Duty=50%	—	—	0.5	MHz
		5.0V		—	—	1.0	MHz
C_i	Input Capacitance	3.3V	—	—	—	15	pF
		5.0V		—	—	15	pF
t_{CW}	Clock Pulse Width	3.3V	—	800	—	—	ns
		5.0V		400	—	—	ns
t_{SW}	Strobe Pulse Width	3.3V	—	2	—	—	μs
		5.0V		1	—	—	μs
t_{SU}	Data Setup Time	3.3V	—	200	—	—	ns
		5.0V		100	—	—	ns
t_h	Data Hold Time	3.3V	—	200	—	—	ns
		5.0V		100	—	—	ns
t_{CS}	Clock-Strobe Time	3.3V	CLK rising edge to CS rising edge	2	—	—	μs
		5.0V		1	—	—	μs
t_W	Wait Time	3.3V	CLK rising edge to CLK falling edge	2	—	—	μs
		5.0V		1	—	—	μs

Functional Description

Display RAM and Display Mode

The static display RAM is organized into 22×8 bits and stores the data transmitted from an external device to the HT16512 through a serial interface. The contents of the RAM are directly mapped to the contents of the VFD driver. Data in the RAM can be accessed through the data setting, address setting and display control commands. It is assigned addresses in 8-bit unit as follows:

S0 ~ S3	S4 ~ S7	S8 ~ S11	S12 ~ S15	
Address: 00H		01H		Digit0
02H		03H		Digit1
04H		05H		Digit2
06H		07H		Digit3
08H		09H		Digit4
0AH		0BH		Digit5
0CH		0DH		Digit6
0EH		0FH		Digit7
10H		11H		Digit8
12H		13H		Digit9
14H		15H		Digit10
b0 b1 b2 b3 b4 b5 b6 b7		b0 b1 b2 b3 b4 b5 b6 b7		

Dimming Control

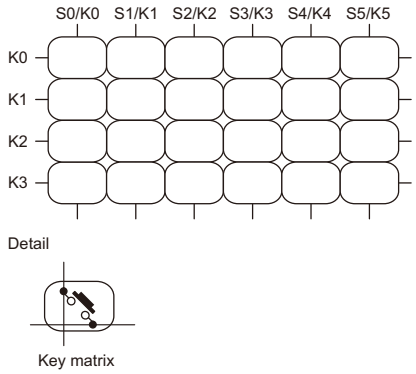
HT16512 provides 8-step dimmer function on display by controlling the 3-bit binary command code. The full pulse width of grid signal is divides into 16 uniform sections by PWM (pulse width modulation) technology.

The 16 uniform sections available form 8 steps dimmer via 3-bit binary code. The 8-step dimmer includes 1/16, 2/16, 4/16, 10/16, 11/16, 12/16, 13/16 and 14/16. The 1/16 pulse width indicates minimum lightness. The 14/16 pulse width represents maximum lightness. (Refer to the display control command).

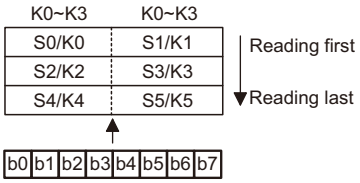
Key Matrix and Key-Input Data Storage RAM

The key matrix scans the series key states at each level of the key strobe signal (S0/K0~S5/K5) output of the HT16512. The key strobe signal outputs are time-multiplexed signals from S0/K0~S5/K5. The states of inputs K0~K3 are sampled by strobe signal S0/K0~S5/K5 and latched into the register.

The key matrix is made up of a 6×4 matrix, as shown below.



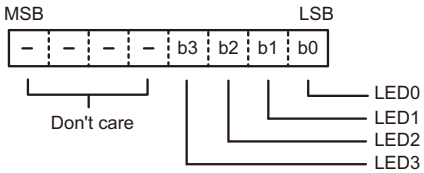
The data of each key is stored as illustrated below, and is read with the read command, starting from the least significant bit.



LED Port

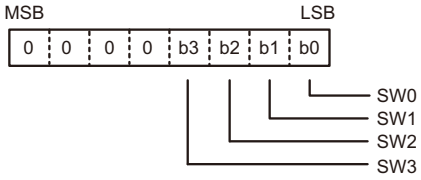
The LED port belongs to the CMOS output configuration.

Data is written to the LED port with the write command, starting from the least port's least significant bit. In our application (see application circuits), the user adopts an internal NMOS device to a driver LED component by connecting VDD. When a bit of this port is 0, the corresponding LED lights; when the bit is 1, the LED turns off. The data of bits 5 through 8 are ignored.



SW Data

HT16512 provides an extra 4-bit general input port. The SW data is provided with available binary code. The SW data is read with the read command, starting from the least significant bit. Bits 5 through 8 of the SW data are 0.



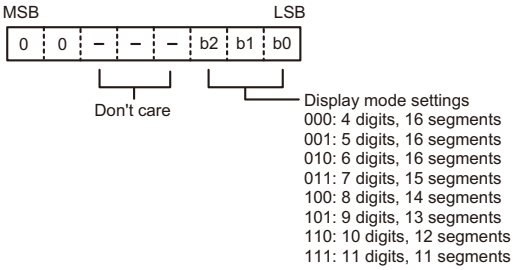
Commands

Commands set the display mode and status of the VFD driver.

The first 1 byte input to the HT16512 through the DI pin after the $\overline{CS}$ pin has fallen, is regarded as a command. If $\overline{CS}$ is set high while commands/data are transmitted, serial communication is initialized, and the commands/data being transmitted are not valid (however, the commands/data previously transmitted remains valid).

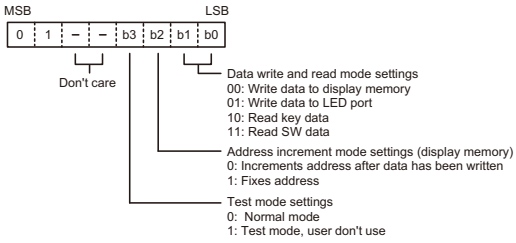
- Display mode setting commands

  These commands initialize the HT16512 and select the number of segments and the number of grids (1/4~1/11 duty, 11 segments to 16 segments).
  When these commands are executed, the display is forcibly turned off, and key scanning is also stopped. To resume display, the display command "ON" must be executed. If the same mode is selected, nothing happens.



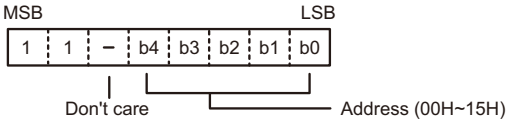
- Data setting commands

  These commands set the data write and data read modes.



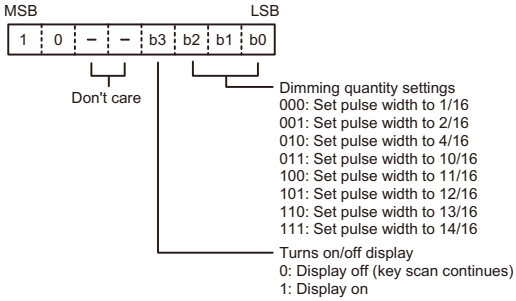
- Address setting commands

  These commands set the address of the display memory.

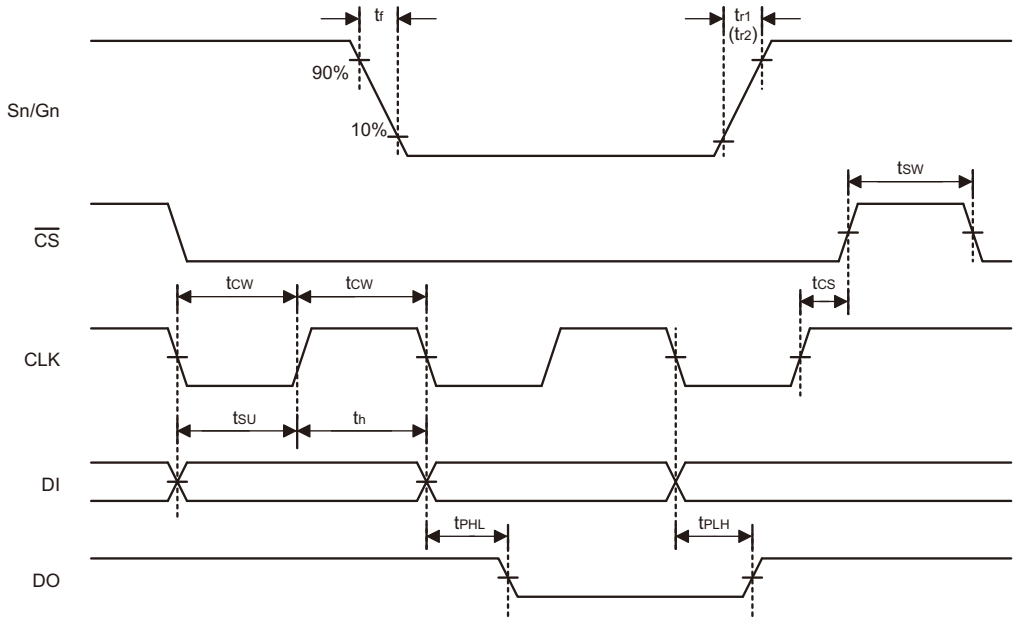


  If address 16H or higher is set, data is ignored until a valid address is set.

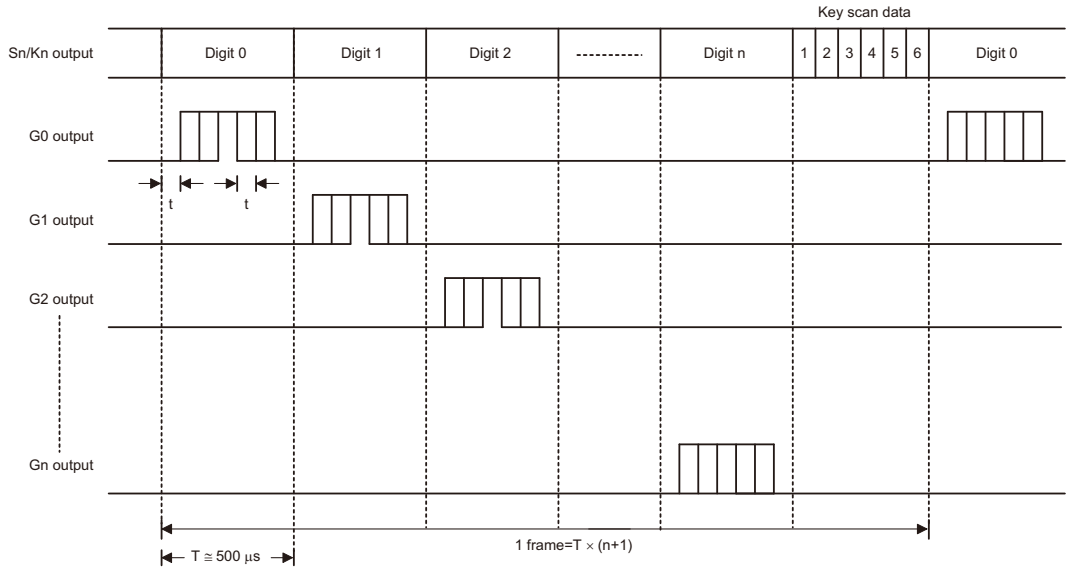
- Display control commands



Timing Diagrams



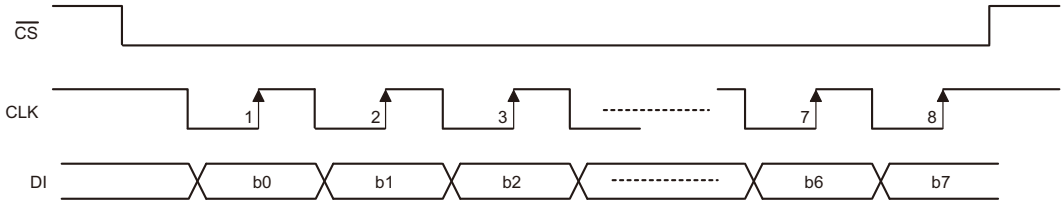
Key Scanning and Display Timing



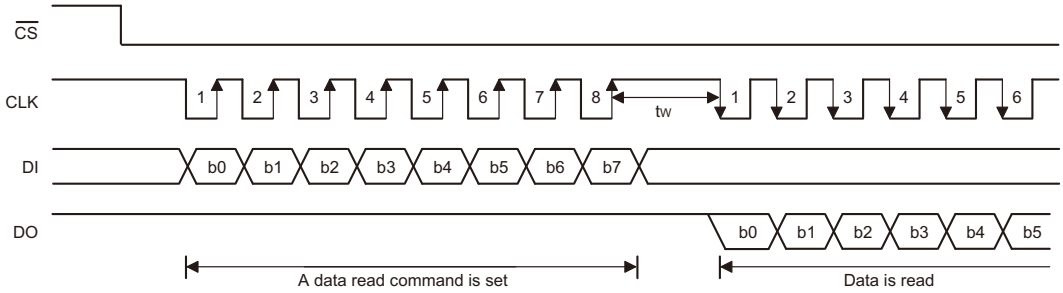
Note: n=0~5
t=1/16T
T: pulse width of segment signal is decided by oscillator frequency
One cycle of key scanning consists of one frame.

Serial Communication Format

- Reception (command/data write)

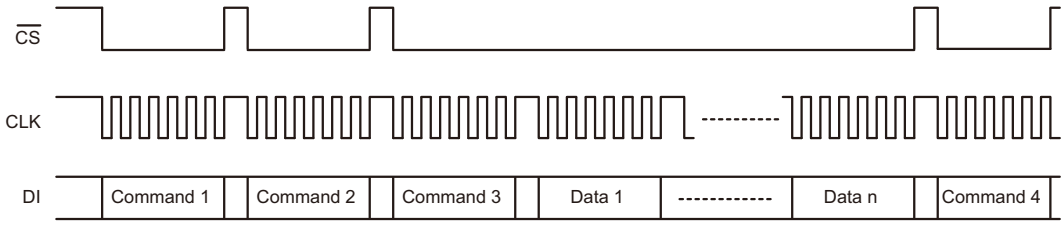


- Transmission (data read)



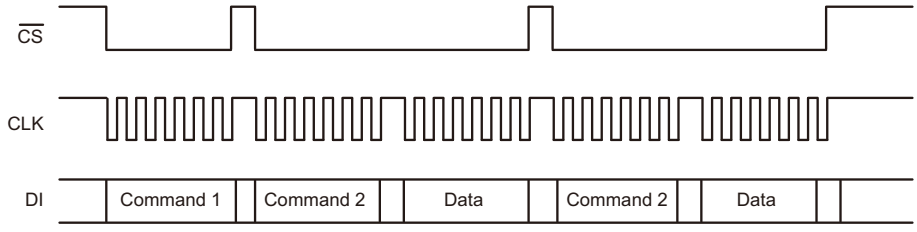
DO must be sure to connect an external pull-high resistor to this pin (1kΩ to 10kΩ).
Note: When data is read, a wait time "t_W" of 1μs is necessary.

- Updating display memory by incrementing address



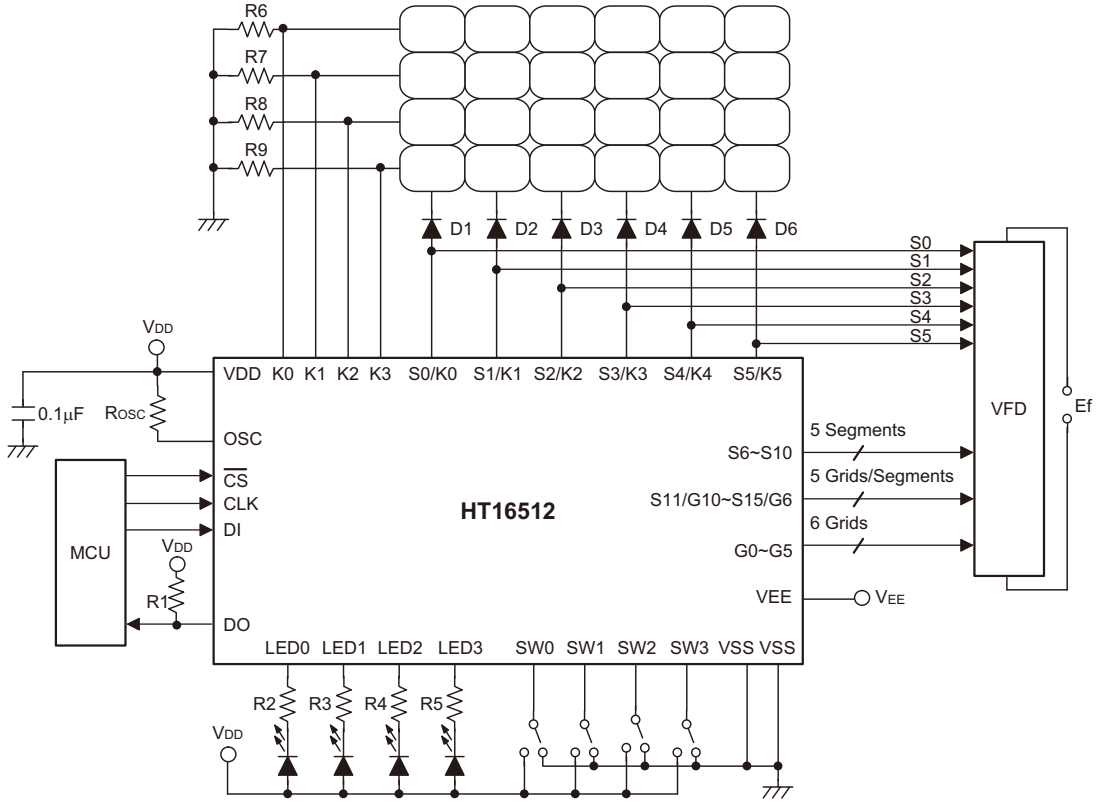
Command 1: sets display mode
Command 2: sets data
Command 3: sets address
Data 1 to n: transfers display data (22 bytes max.)
Command 4: controls diplay

- Updating specific addresses



Command 1: sets data
Command 2: sets address
Data: display data

Application Circuits

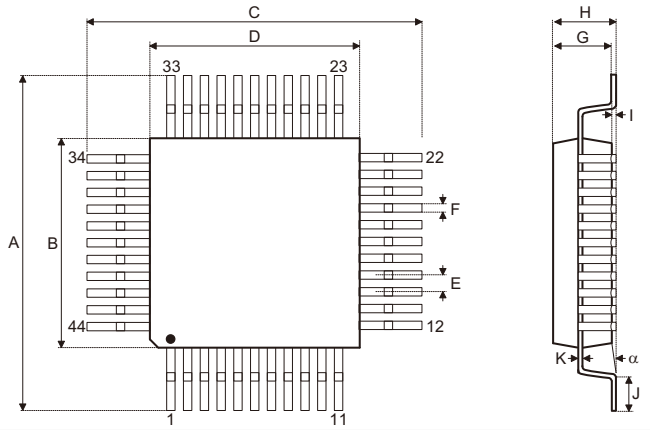


Note: R_{OSC}=51kΩ for oscillator resistor
R1=1~10kΩ for external pull-high resistor
R2~R5=750Ω~1.2kΩ
R6~R9=10kΩ for external pull-low resistor
D1~D6=1N4001
Ef=Filament voltage for VFD
Both of the VSS (pin 7 and pin 43) should be connected to ground.

Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website or the latest version of the package information.

44-pin LQFP (10mm×10mm) (FP2.0mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.469	—	0.476
B	0.390	—	0.398
C	0.469	—	0.476
D	0.390	—	0.398
E	—	0.031	—
F	—	0.012	—
G	0.053	—	0.057
H	—	—	0.063
I	—	0.004	—
J	0.018	—	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	11.90	—	12.10
B	9.90	—	10.10
C	11.90	—	12.10
D	9.90	—	10.10
E	—	0.80	—
F	—	0.30	—
G	1.35	—	1.45
H	—	—	1.60
I	—	0.10	—
J	0.45	—	0.75
K	0.10	—	0.20
α	0°	—	7°

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