HT32FP2350/HT32FP2450
Datasheet

32-Bit Arm® Cortex®-M0 USB Type-C PD MCU

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1 General Description

The Holtek HT32FP2350/HT32FP2450 are 32-bit high performance, low power consumption devices based around an Arm® Cortex®-M0 processor core and designed for USB Power Delivery product applications.

The devices operate at a frequency of up to 21.6 MHz and provide 16 KB of multi-time programming (MTP) memory, 16 KB of ROM and 2 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as 10-bit ADC, two I^2C interfaces (master and slave), Buck / Boost PWM Controller, Timer, Watchdog Timer, etc., are also implemented in the devices.

The devices integrate USB Power Delivery (PD) PHY layer communication protocols and compliant with USB PD 3.0 specification. They provide excellent flexibility for various Power Delivery products such as car chargers, power banks and so on. The devices also provide the PD product application related protection circuits, such as over voltage/under voltage protection (OUVP), over current protection (OCP), over temperature protection (OTP), and VCONN current-limit protection. The devices provide an integration of power management circuit and PD communication physical layer for the USB Quick charger product applications with few external components and simple PCB layout.

2 Features

Core & Memory

- 32-bit Arm® Cortex®-M0 processor
- Up to 21.6 MHz operating frequency
- Embedded Controller
- Application Processor
- 16 KB MTP memory
- 16 KB ROM
- 2 KB SRAM

The Cortex®-M0 processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized processor. The EC (embedded controller) or AP (application processor) can receive the operating status of the voltage, current and temperature and also can be used for the firmware updates. The device offers users the multi-time programming MTP memory, ROM and SRAM.

Under Voltage Lockout – UVLO

- V_{DD} voltage UVLO threshold: $V_{TH\_VDDUVLO}$ = 4V
- V_{PVDD} voltage UVLO threshold: $V_{TH\_PVDDUVLO}$ = 4V
- V_{REGV2} voltage UVLO threshold: V_{TH_V2UVLO} = 1.4V

The UVLO function can continuously monitor the voltages on the VDD, PVDD and V2 pins for ensuring the MCU and PWM controller operate normally. If the voltage on the VDD and V2 pins rise above the respective UVLO thresholds, the internal MCU_UVLO signal will go low and the MCU is activated. If the voltage on the PVDD pin is above the V_{PVDD} voltage UVLO threshold, the PWM_UVLO signal goes low. Only when both the UVLO signals which are the MCU_UVLO and PWM_UVLO, are low, can the PWM controller be activated. Otherwise the MCU or PWM controller will stop and in under voltage lockout status to prevent any undesirable operation.

Pulse Skipping Mode (PSM) with Diode Emulation

- PSM voltage threshold: V_{TH_PSM} = 1.969V
- ZCD voltage threshold: V_{TH_ZCDB} = 4 mV; V_{TH_ZCDD} = 4 mV
- Fixed frequency PWM mode or PSM mode controlled by comparing the voltage

When the system operates in a light load condition, most power loss is caused by switching losses. To improve the efficiency in light load condition, the switching frequency should be reduced. The Pulse Skipping Mode is provided for improving the operating efficiency in light load condition. When the system operates in discontinuous conduction mode which will cause the power losses, the Diode Emulation Mode (DEM) can be used to improve the efficiency.

An internal compensation voltage which follows the voltage at the COMPV or COMPI pin is to be compared with the programmable PSM threshold. When the compensation voltage is above the PSM threshold, the PWM controller operates at normal fixed-frequency mode. While when the voltage drops below the PSM threshold, the PWM controller will enter the PSM mode with lower converter switching frequency to minimize the power losses.

Diode Emulation Mode (DEM) is also a necessary function to avoid energy loss. The DEM function is equipped with two zero current detection (ZCD) circuits which are controlled by the LGATE1 MOSFET and UGATE2 MOSFET respectively. One ZCD circuit is to monitor the source to drain voltage (V_{SDB}) between the PGND and PHASE1 pins and compare the V_{SDB} voltage with the zero current threshold of V_{TH_ZCDB}. When the V_{SDB} drops below the V_{TH_ZCDB}, the LGATE1 MOSFET is turned off thereby avoiding reverse inductor current. The other ZCD circuit is to monitor the source to drain voltage (V_{SDD}) between the PHASE2 and ZCD pins and compare the V_{SDD} voltage with the zero current threshold of V_{TH_ZCDD}. When the V_{SDD} drops below the V_{TH_ZCDD}, the UGATE2 MOSFET is turned off.

Cable Voltage Drop Compensation – CDC

The device is capable of providing constant voltage regulation. The cable voltage drop compensation function can be used to slightly adjust the output voltage to compensate the voltage drop on the USB cable, so as to improve the output power accuracy during PD communications.

Over Voltage & Under Voltage Protection – OUVP

- Programmable VBUS OVP threshold: 3V ~ 24V (8-bit, 97.66mV / Step)
- Programmable VO UVP threshold: 3V ~ 20V (8-bit, 93.75mV / Step)
- Programmable debounce time

The VBUS OVP function is a hardware-based protection which monitors the VBUS pin voltage and compares the voltage with the programmable OVP threshold. When the VBUS voltage exceeds the specified OVP threshold, the OVP comparator output state changes from 0 to 1.

The VO UVP function is a hardware-based protection which monitors the VO pin voltage and compares the voltage with the programmable UVP threshold. When the VO voltage falls below the specified UVP threshold, the UVP comparator output state changes from 0 to 1.

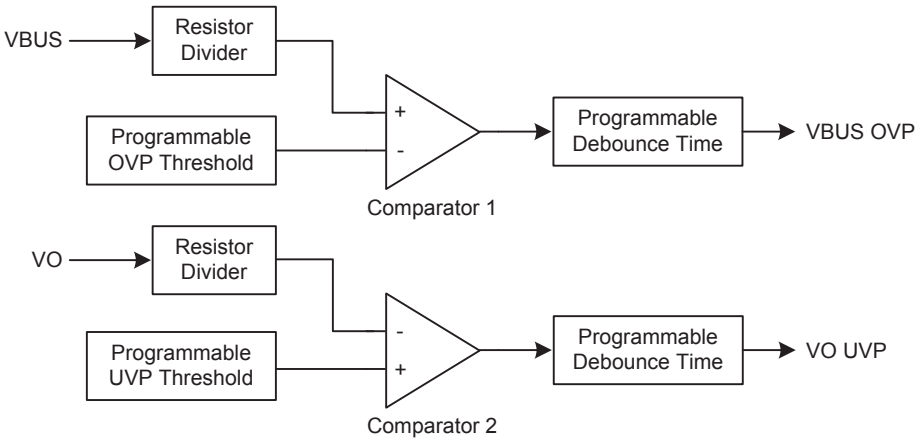


Figure 1. VBUS OVP and VO UVP Block Diagram

Constant Current (CC) Regulation

- Current-Sense Voltage (V_{CS}): 10mV~ 60mV (9-bit, 0.1174mV / Step)

The device integrates a current-sensing amplifier to sense the output current for constant current regulation. The amplifier is equipped with offset cancellation function to accurately sense the current-sense voltage between the CSOP and CSON pins.

Current-sense voltage V_{CS} = Output current × Current-sense resistor

Power-Path Charge-Pump Gate Driver

The device integrates a charge-pump gate driver for driving the N-channel power MOSFETs between the PWM converter output and the USB-C VBUS terminal, thus controlling the output power path on or off. When the GP output which is controlled by the internal "ON" signal is pulled high, the MOSFETs of Q1A and Q1B are turned on. When the GP pin output goes low level, the charge-pump is blocked and the MOSFETs are turned off to disconnect the power path.

The Charge-Pump has two power inputs which are from the VO and VDD. The VO pin should be connected to the PWM converter output to ensure the power NMOS can be turned on successfully. The capacitor (C_{GP}) is used to control the V_{GP} rising rate to reduce the surge current in the power path when the power MOSFETs being switched on. When the power MOSFETs being switched off, the resistor (R_{GP}) is used to reduce the falling rate of the power-path current and prevent voltage spikes. A 1µF MLCC capacitor (C_{MID}) which is connected to ground as shown in the figure below is necessary in order to prevent oscillation when the two MOSFETs are connected together.

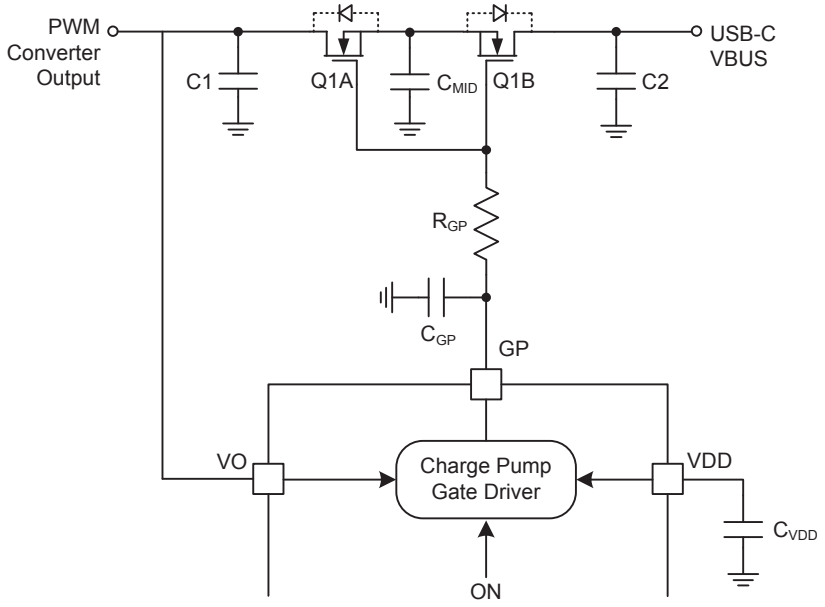


Figure 2. Power-Path Charge-Pump Gate Driver

Power Output for USB Plug Power (V_{CONN})

Two internal switches from the VCONN to VCONN1 and from the VCONN to VCONN2 are provided to control the VCONN power path to VCONN1 or to VCONN2. Either one of the V_{CONN1} and V_{CONN2} can be selected as the power of the USB Type-C cable plug E-Marker ICs. Connect the VCONN1 / VCONN2 pins to USB-C CC1 / 2 terminals via Schottky diodes to prevent reverse current.

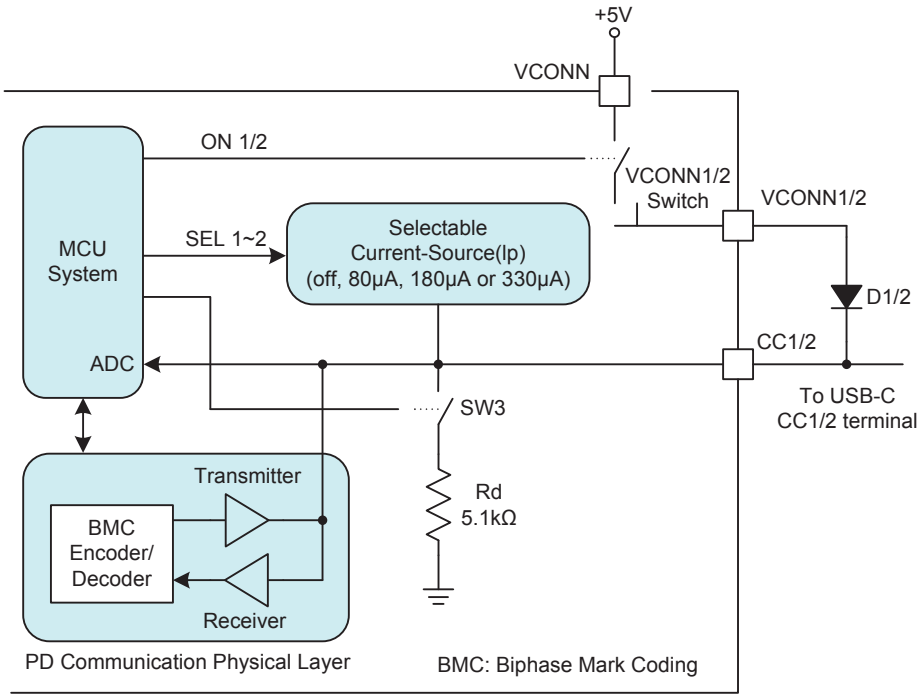


Figure 3. Power Output for USB Plug Power

Output Bleeder for Quick Discharge

The device integrates two Output Bleeders on the VBUS and BLD pins for quick discharge. When the MOSFETs of Q1A and Q1B are turned off, the discharge time (t_{DIS_CVBUS}) of the capacitor connected to the VBUS pin is determined by the following equation:

$$t_{DIS\_CVBUS} = R_{BLD\_INT} \times C_{VBUS} \times \ln\left(\frac{V_{BUS\_INI}}{V_{BUS\_FINAL}}\right)$$

Where:

- R_{BLD_INT} is the total internal resistance of the MOSFET Q_{BLD2}.
- C_{VBUS} is the capacitance coupled to the VBUS pin.
- V_{BUS_INI} is the initial BUS voltage before the discharging.
- V_{BUS_FINAL} is the final BUS voltage after the discharging is complete.

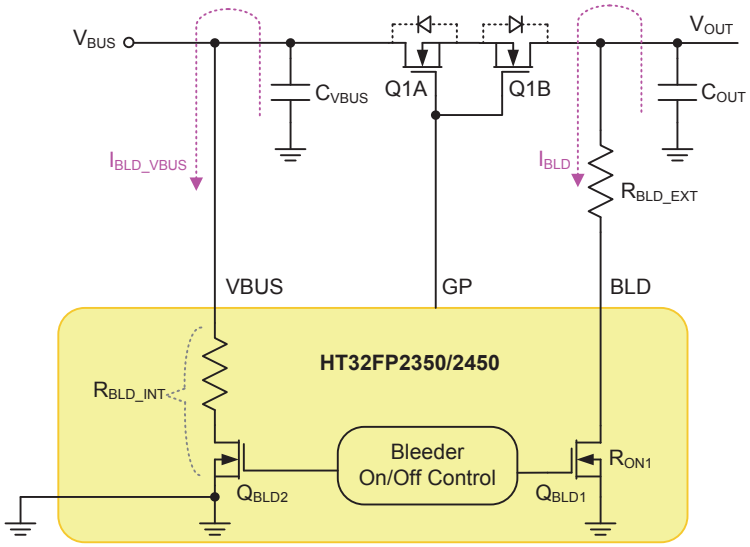


Figure 4. Output Bleeder for Quick Discharge

When the MOSFETs of Q1A and Q1B are on, the discharge time (t_{DIS_COUT}) of the capacitor connected to the BLD pin is determined by the following equation.

$$t_{DIS\_COUT} = (R_{BLD\_EXT} + R_{ON1}) \times C_{OUT} \times \ln\left(\frac{V_{OUT\_INI}}{V_{OUT\_FINAL}}\right)$$

Where:

- R_{BLD_EXT} is the resistance of the external resistor connected to the MOSFET Q_{BLD1}.
- R_{ON1} is the on-resistance of the internal MOSFET Q_{BLD1}.
- C_{OUT} is the capacitance connected to the V_{OUT}.
- V_{OUT_INI} is the initial PWM converter output voltage before the discharging.
- V_{OUT_FINAL} is the final PWM converter output voltage after the discharging is complete.

Package and Operation Temperature

- 40-pin QFN (5mm × 5mm)
- Operation temperature range: -40 °C to +85 °C

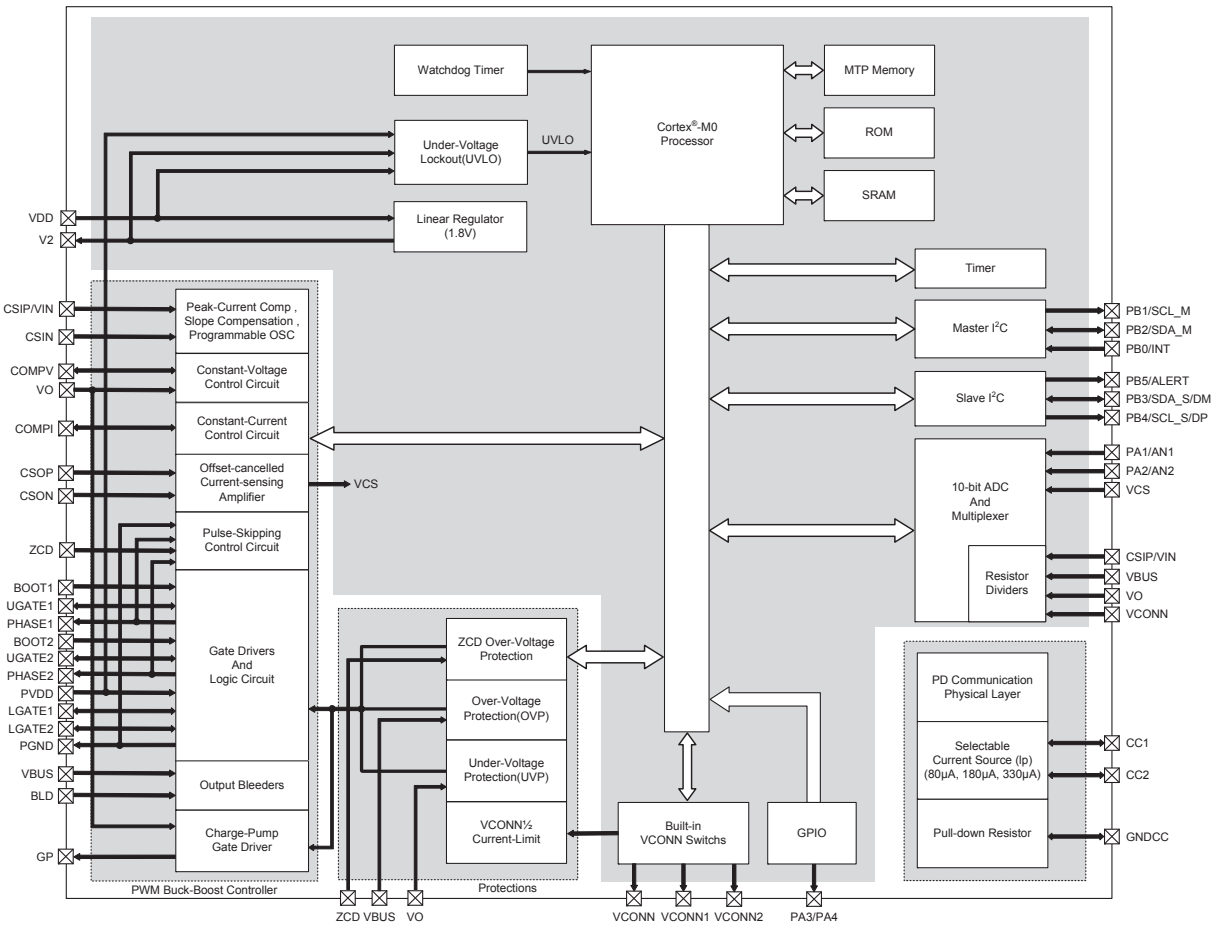
3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32FP2350	HT32FP2450
MTP Flash (KB)		16	16
ROM Flash (KB)		16	16
SRAM (KB)		2	2
Timer	Timer	1	1
	WDT	1	1
Communication	I²C	2	2
GPIO		4	4
EXTI		2	2
10-bit ADC		1	1
Number of channels		2 Channels	2 Channels
Comparator		2	2
Amplifier		1	1
CPU frequency		Up to 21.6 MHz	Up to 21.6 MHz
Operating voltage		4.25 V ~ 5.5 V	4.25 V ~ 5.5 V
Operating temperature		-40 °C ~ +85 °C	-40 °C ~ +85 °C
Package		40-pin QFN (5mm × 5mm)	40-pin QFN (5mm × 5mm)

Block Diagram



Note: the LGATE2, BOOT2, UGATE2 and PHASE2 pins are for the HT32FP2450 device only.

Figure 5. Block Diagram

4 Pin Assignment

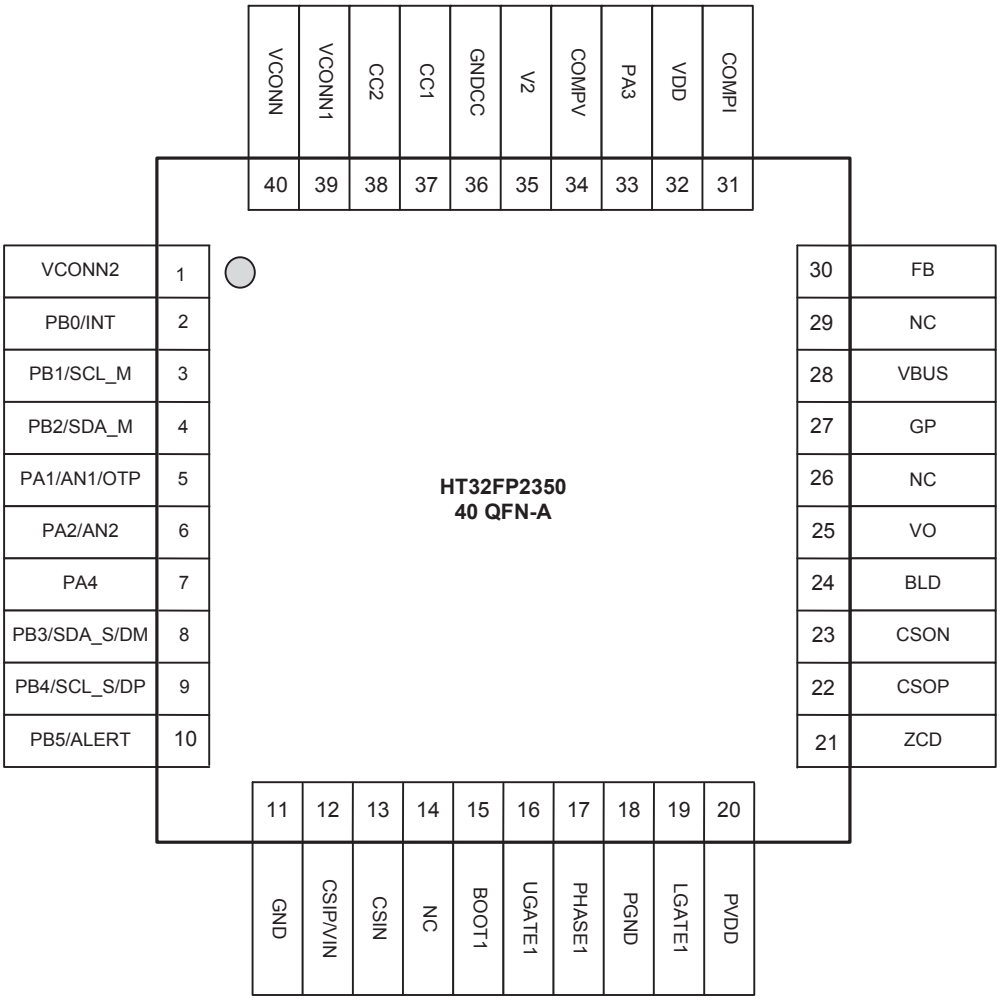


Figure 6. HT32FP2350 40-pin QFN Pin Assignment

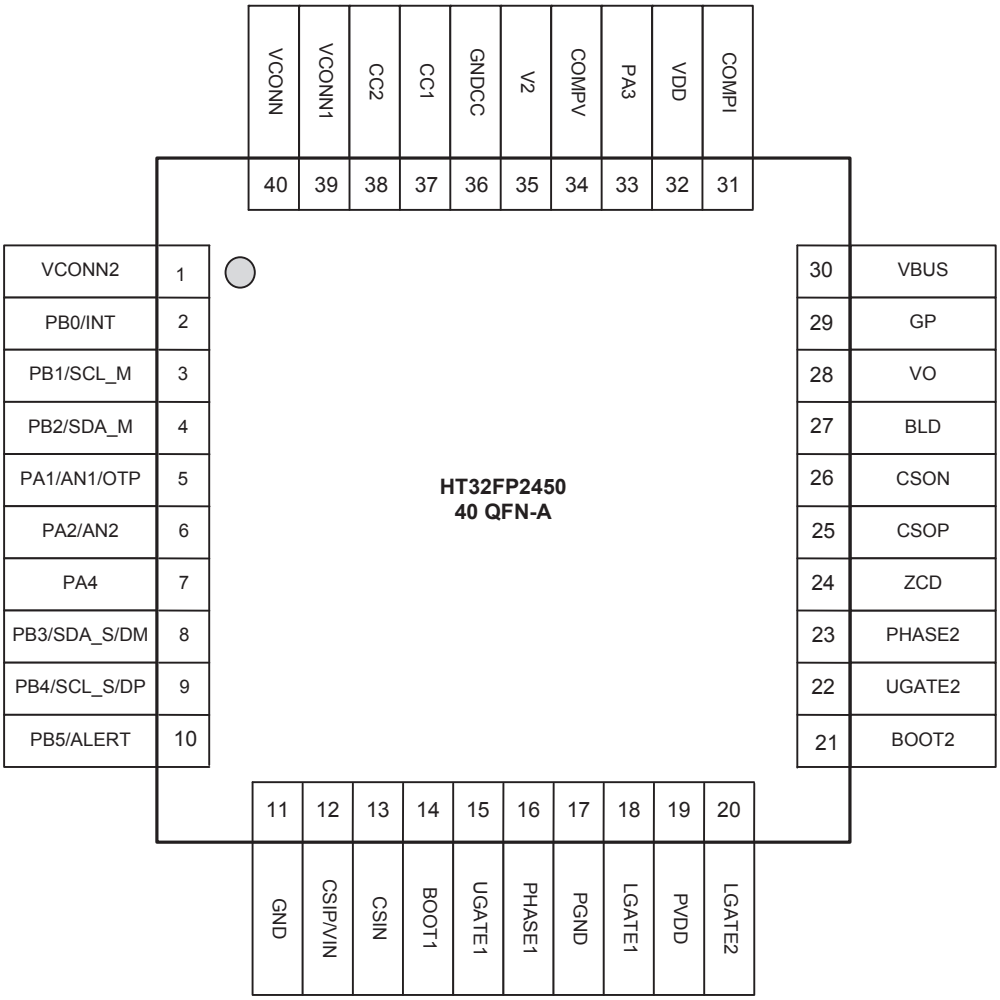


Figure 7. HT32FP2450 40-pin QFN Pin Assignment

5 Pin Description

Table 2. HT32FP2350 Pin Description

No	Name	Description
1	VCONN2	Power output to supply USB Plug power (VCONN) through USB-C CC2 Pin. An integrated MOSFET is controlled to turn on/off the power path from the VCONN to the VCONN2. Generally a Schottky diode is connected to the USB-C CC2 pin.
2	PB0/INT	Interrupt input pin. When a low-level signal is received, the pin can be used for emergency control. The pin can be configured as an open-drain/ push-pull GPIO pin.
3	PB1/SCL_M	Master I²C open-drain clock signal output pin. The pin can be configured as an open-drain/push-pull GPIO pin.
4	PB2/SDA_M	Master I²C open-drain data input/output pin. The pin can be configured as an open-drain/push-pull GPIO pin.
5	PA1/AN1/OTP	Open-drain/push-pull GPIO or analog input or external over temperature protection signal input pin. A NTC can be connected between this pin and GND for the over temperature protection (OTP).
6	PA2/AN2	Open-drain/push-pull GPIO or analog input pin.
7	PA4	Open-drain/push-pull GPIO pin.
8	PB3/SDA_S/DM	Slave I²C open-drain data input/output or USB D- Data Line input/output pin. The pin can be configured as an open-drain GPIO or connects to USB D- for special communication protocol.
9	PB4/SCL_S/DP	Slave I²C open-drain clock input or USB D+ Data Line input/output pin. The pin can be configured as an open-drain GPIO or connects to USB D+ for special communication protocol.
10	PB5/ALERT	Open-drain interrupt signal output pin. When a low level signal is output from this pin to an external MCU, the MCU will check the slave I²C registers to do an emergency control. The pin can be configured as an open-drain/push-pull GPIO pin.
11	GND	Analog Ground.
12	CSIP/VIN	Positive input for input current sensing, or input for converter input voltage sensing.
13	CSIN	Negative input for input current sensing.
14	NC	No Connection
15	BOOT1	Positive power-rail pin of high-side gate driver. Connect a 0.1μF capacitor between this pin and the PHASE1 pin.
16	UGATE1	Output of high-side gate driver.
17	PHASE1	Negative power-rail pin of high-side gate driver.
18	PGND	Low-side gate driver ground, or one input pin of the LGATE1 controlled MOSFET zero current detection.
19	LGATE1	Output of low-side gate driver.
20	PVDD	Low-side gate driver power supply (5V). A 1μF MLCC is recommended to be connected between this pin and the PGND pin.
21	ZCD	Input of the LGATE1 MOSFET controlled zero current detection, or input of the output over voltage protection.
22	CSOP	Positive input of offset-cancelled current-sensing amplifier for output constant current regulation and output current detection. An external current sense resistor and RC filter should be connected to this pin.

No	Name	Description
23	CSON	Negative input of offset-cancelled current-sensing amplifier for output constant current regulation and output current detection. An external current sense resistor and RC filter should be connected to this pin.
24	BLD	For output bleeder, integrating a pull-low NMOS, provides a path to discharge the capacitor at the output of the PWM converter. An external resistor is connected to this pin.
25	VO	Input of the output feedback. The voltage on this pin is monitored by the under voltage protection.
26	NC	No Connection
27	GP	Charge-pump Gate Driver output. Drive the NMOS to turn on/turn off the output power path.
28	VBUS	USB-C VBUS voltage input. The voltage on this pin is monitored by the over voltage protection.
29	NC	No Connection
30	FB	Used for internal feedback, the pin should be kept floating.
31	COMPI	Constant Current (CC) error amplifier output. Connect an external RC network between this pin and the ground for constant current loop feedback compensation.
32	VDD	5V MCU power supply input. It is recommended to connect an external RC filter of 1μF and 2Ω.
33	PA3	Open-drain/push-pull GPIO.
34	COMPV	Constant Voltage (CV) error amplifier output. Connect an external RC network between this pin and the ground for constant voltage loop feedback compensation.
35	V2	1.8V linear regulator output for internal circuit power supply. Should connect an external MLCC (1μF typ. or larger).
36	GNDCC	Ground.
37	CC1	Connect with USB-C CC1 terminal.
38	CC2	Connect with USB-C CC2 terminal.
39	VCONN1	Power output to supply USB Plug power (VCONN) through USB-C CC1 Pin. An integrated MOSFET is controlled to turn on/off the power path from the VCONN to the VCONN1. Generally a Schottky diode is connected to the USB-C CC1 pin.
40	VCONN	Power supply input. The power on VCONN can be input to VCONN1 and VCONN2. Generally the pin is connected to a 5V voltage source.

Table 3. HT32FP2450 Pin Description

No	Name	Description
1	VCONN2	Power output to supply USB Plug power (VCONN) through USB-C CC2 Pin. An integrated MOSFET is controlled to turn on/off the power path from the VCONN to the VCONN2. Generally a Schottky diode is connected to the USB-C CC2 pin.
2	PB0/INT	Interrupt input pin. When a low-level signal is received, the pin can be used for emergency control. The pin can be configured as an open-drain/ push-pull GPIO pin.
3	PB1/SCL_M	Master I²C open-drain clock signal output pin. The pin can be configured as an open-drain/push-pull GPIO pin.
4	PB2/SDA_M	Master I²C open-drain data input/output pin. The pin can be configured as an open-drain/push-pull GPIO pin.
5	PA1/AN1/OTP	Open-drain/push-pull GPIO or analog input or external over temperature protection signal input pin. A NTC can be connected between this pin and GND for the over temperature protection (OTP).
6	PA2/AN2	Open-drain/push-pull GPIO or analog input pin.
7	PA4	Open-drain/push-pull GPIO pin.
8	PB3/SDA_S/DM	Slave I²C open-drain data input/output or USB D- Data Line input/output pin. The pin can be configured as an open-drain GPIO or connects to USB D- for special communication protocol.
9	PB4/SCL_S/DP	Slave I²C open-drain clock input or USB D+ Data Line input/output pin. The pin can be configured as an open-drain GPIO or connects to USB D+ for special communication protocol.
10	PB5/ALERT	Open-drain interrupt signal output pin. When a low level signal is output from this pin to an external MCU, the MCU will check the slave I²C registers to do an emergency control. The pin can be configured as an open-drain/push-pull GPIO pin.
11	GND	Analog Ground.
12	CSIP/VIN	Positive input for input current sensing, or input for converter input voltage sensing.
13	CSIN	Negative input for input current sensing.
14	BOOT1	Positive power-rail pin of high-side gate driver. Connect a 0.1μF capacitor between this pin and the PHASE1 pin.
15	UGATE1	Output of high-side gate driver.
16	PHASE1	Negative power-rail pin of high-side gate driver.
17	PGND	Low-side gate driver ground, or one input pin of the LGATE1 controlled MOSFET zero current detection.
18	LGATE1	Output of low-side gate driver.
19	PVDD	Low-side gate driver power supply (5V). A 1μF MLCC is recommended to be connected between this pin and the PGND pin.
20	LGATE2	Output of low-side gate driver.
21	BOOT2	Positive power-rail pin of high-side gate driver. Connect a 0.1μF capacitor between this pin and the PHASE2 pin.
22	UGATE2	Output of high-side gate driver.
23	PHASE2	Negative power-rail pin of high-side gate driver.
24	ZCD	Input of the LGATE1 MOSFET controlled zero current detection, or input of the output over voltage protection.
25	CSOP	Positive input of offset-cancelled current-sensing amplifier for output constant current regulation and output current detection. An external current sense resistor and RC filter should be connected to this pin.

No	Name	Description
26	CSON	Negative input of offset-cancelled current-sensing amplifier for output constant current regulation and output current detection. An external current sense resistor and RC filter should be connected to this pin.
27	BLD	For output bleeder, integrating a pull-low NMOS, provides a path to discharge the capacitor at the output of the PWM converter. An external resistor is connected to this pin.
28	VO	Input of the output feedback. The voltage on this pin is monitored by the under voltage protection.
29	GP	Charge-pump Gate Driver output. Drive the NMOS to turn on/turn off the output power path.
30	VBUS	USB-C VBUS voltage input. The voltage on this pin is monitored by the over voltage protection.
31	COMPI	Constant Current (CC) error amplifier output. Connect an external RC network between this pin and the ground for constant current loop feedback compensation.
32	VDD	5V MCU power supply input. It is recommended to connect an external RC filter of 1μF and 2Ω.
33	PA3	Open-drain/push-pull GPIO.
34	COMPV	Constant Voltage (CV) error amplifier output. Connect an external RC network between this pin and the ground for constant voltage loop feedback compensation.
35	V2	1.8V linear regulator output for internal circuit power supply. Should connect an external MLCC (1μF typ. or larger).
36	GNDCC	Ground.
37	CC1	Connect with USB-C CC1 terminal.
38	CC2	Connect with USB-C CC2 terminal.
39	VCONN1	Power output to supply USB Plug power (VCONN) through USB-C CC1 Pin. An integrated MOSFET is controlled to turn on/off the power path from the VCONN to the VCONN1. Generally a Schottky diode is connected to the USB-C CC1 pin.
40	VCONN	Power supply input. The power on VCONN can be input to VCONN1 and VCONN2. Generally the pin is connected to a 5V voltage source.

6 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute Maximum Ratings

Parameter		Min.	Max.	Unit
V2 to GND		-0.3	+2.5	V
VDD to GND		-0.3	+6.5	V
PVDD to GND		-0.3	+6.5	V
VCONN to GND		-0.3	+6.5	V
FB to GND		-0.3	+6.5	V
COMPV to GND		-0.3	+6.5	V
COMPI to GND		-0.3	+6.5	V
VCONN1 to GND		-0.3	Vvconn+0.3	V
VCONN2 to GND		-0.3	Vvconn+0.3	V
VBUS to GND		-0.3	+25	V
CSOP to GND		-0.3	+25	V
CSON to GND		-0.3	+25	V
VO to GND		-0.3	+25	V
BLD to GND		-0.3	+25	V
ZCD to GND		-0.3	+25	V
$V_{CSOP-CSON}$ (1)		-5	+5	V
GP to GND		-0.3	+33	V
CSIP/VIN to GND		-0.3	+40	V
CSIN to GND		-0.3	+40	V
CSIP/VIN to CSIN		-5	+5	V
PA, PB to GND		-0.3	+6.5	V
CC1/CC2 to GND		-0.3	+25	V
$V_{BOOT-PHASE}$ (2)		-0.3	+6.5	V
$V_{UGATE-PHASE}$ (3)		-0.3	$V_{BOOT-PHASE}$+0.3	V
PHASE1 to GND		-0.3	+40	V
PHASE2 to GND		-0.3	+25	V
LGATE1/2 to PGND		-0.3	V_{PVDD}+0.3	V
PGND/GNDCC to GND		-0.3	0.3	V
Power Dissipation, PD @ T_A = 25°C		—	3.63	W
Package Thermal Resistance @ T_A = 25°C	Junction to Ambient, θ_{JA}	—	27.5	°C/W
	Junction to Case, θ_{JC}	—	6	°C/W

Parameter	Min.	Max.	Unit
Maximum Junction Temperature	—	150	°C
Lead Temperature Range	—	260	°C
Storage Temperature Range	-65	+150	°C
Electrostatic Discharge Voltage – Human Body Model	-2000	+2000	V

Note: 1.$V_{CSOP-CSON}$ = CSOP to CSON voltage.
2. $V_{BOOT-PHASE}$ = BOOT1 to PHASE1 voltage or BOOT2 to PHASE2 voltage.
3. $V_{UGATE-PHASE}$ = UGATE1 to PHASE1 voltage or UGATE2 to PHASE2 voltage.

Recommended DC Operating Conditions

Table 5. Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	CSIP/VIN Input Voltage	4	—	36	V
V_{BUS}	VBUS Input Voltage	3	—	22	V
V_{DD}	VDD Input Voltage	4.25	5	5.5	V
V_{PVDD}	PVDD Input Voltage	4.5	5	5.5	V
V_{TOH}	TX High Level Output Voltage	1.05	—	1.2	V
V_{TOL}	TX Low Level Output Voltage	0	—	75	mV
V_{RIH}	RX High Level Input Voltage	0.67	—	1.45	V
V_{RIL}	RX Low Level Input Voltage	-0.25	—	0.43	V

Power Consumption

Table 6. Power Consumption Characteristics

V_{DD} = V_{PVDD} = V_{VCONN} = 5V, T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current (Run Mode)	PWM on, MCU on, Digital output pins open	—	10	15	mA
	Supply Current (Sleep Mode)	PWM on, MCU off, No load current, GP on, Digital output pins open	—	5	8	mA
	Supply Current (Deep-Sleep Mode)	PWM off, MCU off, Digital output pins open	—	75	150	μA
I_{PVDD}	PVDD Input Current	PWM off	—	—	3	μA
I_{VCONN}	VCONN Input Current	Resistor divider & Switches off	—	—	3	μA
I_{BOOT}	BOOT Input Current	$V_{BOOT1/2}$ = 4.5V, PWM off	—	—	3	μA

V2 Linear Regulator Characteristics

Table 7. V2 Linear Regulator Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{REGV2}	V2 Output Voltage	I_{V2} = 0A	1.58	1.76	1.94	V
I_{SHTV2}	V2 Short Circuit Current	—	30	50	80	mA

UVLO Characteristics

Table 8. UVLO Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{TH\_VDDUVLO}$	V_{DD} UVLO Threshold	—	3.8	4.0	4.2	V
$V_{HY\_VDDUVLO}$	V_{DD} UVLO Hysteresis	—	—	0.25	—	V
V_{TH_V2UVLO}	V_{REGV2} UVLO Threshold	—	—	1.4	—	V
V_{HY_V2UVLO}	V_{REGV2} UVLO Hysteresis	—	—	0.15	—	V
$V_{TH\_PVDDUVLO}$	V_{PVDD} UVLO Threshold	—	3.8	4.0	4.2	V
$V_{HY\_PVDDUVLO}$	V_{PVDD} UVLO Hysteresis	—	—	0.2	—	V

OUVP Characteristics

Table 9. OUVP Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{TH\_CSIP/VINUVP}$	CSIP/VIN UVP Threshold	—	2.7	2.9	3.1	V
$V_{HY\_CSIP/VINUVP}$	CSIP/VIN UVP Hysteresis	—	—	0.25	—	V
$V_{TH\_VBUSOVP}$	VBUS OVP Threshold	Programmable (8-bit, 97.66mV / step)	3.03	—	24.90	V
$A_{TH\_VBUSOVP}$	VBUS OVP Threshold Accuracy	$V_{TH\_VBUSOVP}$ = 5.96V / 24.0V	-5	—	+5	%
$t_{DB\_VBUSOVP}$	VBUS OVP Debounce Time	Programmable	—	4.5	6.6	μs
			—	7.0	9.6	
			—	12	15.6	
			—	22	27.6	
V_{TH_VOUVP}	VO UVP Hysteresis	Programmable (8-bit, 93.75mV / step)	3.00	—	19.97	V
A_{TH_VOUVP}	VO UVP Threshold Accuracy	V_{TH_VOUVP} = 3V / 15V	-5	—	+5	%
t_{DEB}	VO UVP Debounce Time	Programmable	—	8	13.6	μs
			—	10.5	16.6	
			—	15.5	22.6	
			—	25.5	34.6	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{BT}	VO UVP Blanking Time during Start-up	Programmable	4	5	6	ms
			8	10	12	
			16	20	24	
			32	40	48	

CC1/CC2 Voltage Detection

Table 10. CC1/CC2 Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{CC1/2}$	CC1/2 Voltage Detection Range	Using the 10-bit ADC	0	—	2.7	V
$A_{CC1/2}$	CC1/2 Voltage Detection Accuracy	Using the 10-bit ADC, $V_{CC1/2}$ = 0.1 ~ 2.7V	-40	—	+40	mV
I_P	CC1/2 Pull-up Current Source	For default USB power	64	80	96	μA
		1.5A @ 5V	165.6	180	194.4	μA
		3A @ 5V	303.6	330	356.4	μA
R_D	CC1/ CC2 pin Pull-down Resistor	—	4.6	5.1	5.6	kΩ
$V_{OUT\_CC1/2}$	CC1/2 Maximum Output Voltage	CC1/CC2 open	—	V_{DD}-0.7V	—	V

MCU AC Characteristics

Table 11. MCU AC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{MCU}	MCU Frequency (Normal Operation)	—	19.4	21.6	23.8	MHz
f_{MCU_HALT}	MCU Frequency (Sleep modes)	—	—	80	—	kHz

VCONN Characteristics

Table 12. VCONN Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
—	On-resistance of the VCONN to VCONN1/2 MOSFET	—	—	0.4	0.8	Ω
—	VCONN1/2 Output Voltage Accuracy	Output current = 0 ~ 200mA	4.7	—	—	V
—	VCONN1/2 Current-limit Threshold	VCONN1/2 = GND	350	500	650	mA

PWM Controller Characteristics

Table 13. PWM Controller Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{OSC}	Oscillator Frequency	Programmable	200	—	600	kHz
A_{OSC}	Oscillator Frequency Accuracy	T_A = 25°C	-6	—	+6	%
		T_A = -40 ~ 85°C	-10	—	+10	
t_{ON_MAX}	Oscillator Maximum On Time	Programmable	0.32	—	5.88	μs
V_{REG_VO}	Constant Voltage Regulated Voltage (VO pin)	Programmable (10-bit), 15.625 mV/step	3.00	—	15.98	V
		Programmable (10-bit), 23.438mV/step	3.00	—	23.977	
—	Output Voltage Accuracy (VO pin)	T_A= 25°C, V_{OUT} = 5V/9V/12V/15V/20V 23.438mV/step	-2	—	+2	%
		T_A = -40 ~ 85°C, V_{OUT} = 5V/9V/12V/15V/20V 23.438mV/step	-3	—	+3	%
G_{MV}	COMPV Amplifier Trans-Conductance	I_{COMPV} = ±20μA	412	550	688	μA / V
—	COMPV Maximum Output Voltage	COMPV open	3.2	3.5	—	V
V_{OFS1}	COMPV Offset Voltage	—	—	0.35	—	V
—	CSON/CSOP Operating Voltage	—	3	—	22	V
V_{REF_CC}	CC Regulated Voltage Range between CSON and CSOP	Programmable (8-bit), 0.234 mV/step, V_{CSON} > 3V, V_{CSOP} > 3V	10	—	60	mV
—	CC Reference Voltage Accuracy	V_{REF_CC} =20 mV / 60mV	-3	—	+3	mV
G_{MI}	COMPI Amplifier Trans-Conductance	I_{COMPI} = ±20μA	412	550	688	μA / V
—	COMPI Maximum Output Voltage	COMPI open	3.2	3.5	—	V
V_{OFS2}	COMPI Offset Voltage	—	—	0.35	—	V
V_{TH_CSMAX}	Maximum Input Current-sensing Voltage	Programmable	—	—	140	mV
—	V_{TH_CSMAX} Voltage Threshold Accuracy	—	-15	—	+15	mV
t_{LEB}	Leading Edge Blanking Time of Input Peak/Over Current Comparator	From V_{UGATE1} rising edge, programmable	—	100	—	ns
				150		
				200		
				250		
		From V_{LGATE2} rising edge, programmable	—	100	—	ns
				150		
				200		
				250		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
—	Voltage Rate of Slope Compensation	Programmable	0	—	92	mV/μs
V_{TH_PSM}	PSM Voltage Threshold (COMPV& COMPI pin)	Programmable	—	—	1.969	$+V_{OFS1/2}$
V_{TH_ZCDD}	MOS-D ZCD Voltage Threshold between PHASE2 and ZCD pins	—	—	4	—	mV
V_{TH_ZCDB}	MOS-B ZCD Voltage Threshold between PGND and PHASE1 pins	—	—	4	—	mV
t_{LEBD}	Leading Edge Blanking Time of MOS-D ZCD	From V_{UGATE2} Rising, Programmable	—	150 225 300 375	—	ns
t_{LEBB}	Leading Edge Blanking Time of MOS-B ZCD	From V_{LGATE1} Rising, Programmable	—	100 150 200 250	—	ns
—	UGATE1/2 Pull-up Resistance	$V_{BOOT-PHASE}$ = 5V, $V_{BOOT-UGATE}$ = 0.1V	—	1.7	—	Ω
—	UGATE1/2 Pull-low Resistance	$V_{UGATE-PHASE}$ = 0.1V	—	0.8	—	Ω
—	LGATE1/2 Pull-up Resistance	V_{PVDD} - $V_{LGATE1/2}$ = 0.1V	—	1.7	—	Ω
—	LGATE1/2 Pull-low Resistance	$V_{LGATE1/2}$ = 0.1V	—	0.8	—	Ω
—	Dead Time before UGATE1/2 Rising Edge	—	—	20	—	ns
—	Dead Time after UGATE1/2 Falling Edge	—	—	20	—	ns
—	BLD Pull-low MOS On-resistance	Pull-low NMOS on, I_{BLD} = 10mA	—	8	16	Ω
—	BLD Leakage Current	V_{BLD} = 20V, Pull-low NMOS off	—	—	1	μA
—	VBUS Pull-low Resistance	Pull-low NMOS on	—	1.1	1.5	kΩ

PA & PB & RX/TX & GP Electrical Characteristics

Table 14. PA & PB & RX/TX & GP Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_R	TX Output Voltage Rise Time	From 10% to 90%, C_L= 200pF ~ 600pF	300	—	—	ns
t_F	TX Output Voltage Fall Time	From 90% to 10%, C_L= 200pF ~ 600pF	300	—	—	ns
—	GP Pull-low MOS On-resistance	—	—	100	—	Ω
V_{GP}	Maximum GP Voltage	V_{VO} = 20V, R_{GP-GND} = 50MΩ	V_{VO}+V_{DD}	V_{VO} +2×V_{DD} -3V	V_{VO} +2×V_{DD} -1V	V
V_{IH}	PA/PB High Level Input Voltage	Configure the pins in input type	1.5	—	—	V
V_{IL}	PA/PB Low Level Input Voltage	Configure the pins in input type	—	—	0.4	V
V_{OH}	PA/PB High Level Output Voltage	Source current = 2mA, output high	—	V_{DD}-0.8V	—	V
V_{OL}	PA/PB Low Level Output Voltage	Sink current = 2mA	—	—	0.3	V
I_{LEAK}	PA/PB Leakage Current	Input voltage = 5V	—	—	1	μA
R_{DP-DM}	Internal Resistance of DP to DM	—	—	12	30	Ω
—	RT Current Source	V_{RT} < 2.7V	95	100	105	μA

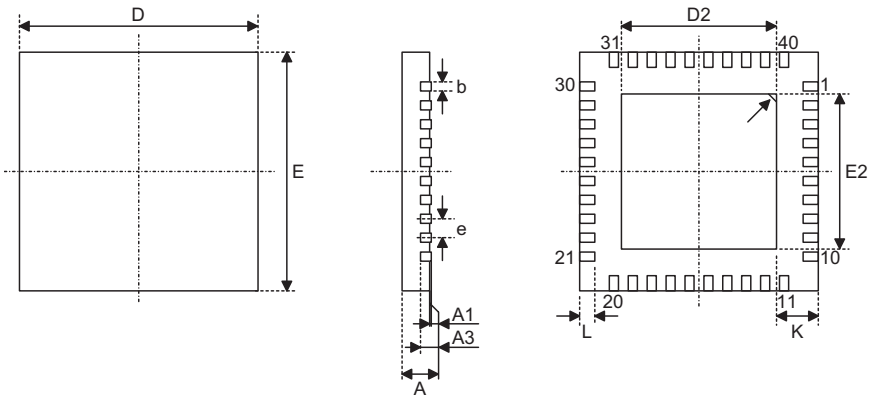
7 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

SAW Type 40-pin QFN (5mm×5mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.006	0.008	0.010
D	—	0.197 BSC	—
E	—	0.197 BSC	—
e	—	0.016 BSC	—
D2	0.126	0.130	0.132
E2	0.126	0.130	0.132
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A3	—	0.200 BSC	—
b	0.150	0.200	0.250
D	—	5.000 BSC	—
E	—	5.000 BSC	—
e	—	0.40 BSC	—
D2	3.20	3.30	3.35
E2	3.20	3.30	3.30
L	0.35	0.40	0.45
K	0.20	—	—