HT32F0008
Datasheet

32-Bit Arm® Cortex®-M0+ Microcontroller,
up to 64 KB Flash and 16 KB SRAM with AES-128,
PDMA, DIV, USART, UART, SPI, I^2C, GPTM,
BFTM, PWM, CRC, RTC, WDT and USB2.0 FS

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1 General Description

The HOLTEK HT32F0008 device is a high performance, low power consumption 32-bit microcontroller based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The device operates at a frequency of up to 60 MHz with a Flash accelerator to obtain maximum efficiency. It provides up to 64 KB of embedded Flash memory for code/data storage and 16 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as PDMA, AES-128, DIV, I^2C, USART, UART, SPI, GPTM, PWM, CRC-16/32, RTC, WDT, USB 2.0 FS, SW-DP (Serial Wire Debug Port), etc., are also implemented in the device. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the device is suitable for use in a wide range of applications, especially in areas such as Data Bridges, sensor hubs and so on.

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 60 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets; single-cycle I/O port; hardware multiplier and low latency interrupt respond time.

On-chip Memory

- 64 KB on-chip Flash memory for instruction/data and options storage
- 16 KB on-chip SRAM
- Supports multiple boot modes

The Arm® Cortex®-M0+ processor accesses and debug accesses share the single external interface to external AHB peripheral. The processor accesses take priority over debug accesses. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 shows the memory map of the HT32F0008 device, including code, SRAM, peripheral, and other pre-defined regions.

Flash Memory Controller – FMC

- Flash accelerator for maximum efficiency
- 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer and cache are provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor:
  - Power On Reset / Power Down Reset – POR/PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by an external signal, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- External 32,768 Hz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to ±2 % accuracy at 3.3 V operating voltage and 25 ˚C operating temperature
- Internal 32 kHz RC oscillator
- Integrated system clock PLL and USB PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control Unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), a HSE clock monitor, clock prescalers, clock multiplexers, APB clock divider and gating circuitry. The AHB, APB and Cortex®-M0+ clocks are derived from the system clock (CK_SYS) which can come from the HSI, HSE or PLL. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source.

Power Management – PWRCU

- Single V_{DD} power supply: 1.65 V to 3.6 V
- Integrated 1.5 V LDO regulator for CPU core, peripherals and memories power supply
- V_{DD} power supply for RTC
- Two power domains: V_{DD}, 1.5 V
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Power-Down

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in the device provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down mode. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge, or both edge
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

I/O Ports – GPIO

- Up to 42 GPIOs
- Port A, B, C, F are mapped as 16 external interrupts – EXTI
- Almost all I/O pins have a configurable output driving current

There are up to 42 General Purpose I/O pins, GPIO, named from PA0 ~ PA15 to PC0 ~ PC7 and PF0 ~ PF1 for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

PWM Generation and Capture Timers – GPTM

- 16-bit up, down, up/down auto-reload counter
- 16-bit programmable prescaler allowing counter clock frequency division by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General Purpose Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation, or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

Pulse Width Modulation – PWM

- 16-bit up and auto-reload counter
- Up to 4 independent channels for each timer
- 16-bit programmable prescaler allowing counter clock frequency division by any factor between 1 and 65536
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output

The Pulse Width Modulator consists of one 16-bit up/down-counter, four 16-bit Compare Registers (CRs), one 16-bit Counter-Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer and output waveform generation such as single pulse generation or PWM output.

Basic Function Timer – BFTM

- 32-bit compare/match count-up counter – no I/O control features
- One shot mode – counting stops after a match condition
- Repetitive mode – restart counter after a match condition

The Basic Function Timer is a simple count-up 32-bit counter designed to measure time intervals and generate a one shot or repetitive interrupts. The BFTM operates in two functional modes, repetitive or one shot mode. In the repetitive mode the BFTM restarts the counter when a compare match event occurs. The BFTM also supports a one shot mode which forces the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-bit down counter with 3-bit prescaler
- Reset event for the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect system failures due to software malfunctions. It includes a 12-bit count-down counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter when the counter value is greater than the WDT delta value. This means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. There is a register write protect function which can be enabled to prevent it from changing the Watchdog Timer configuration unexpectedly.

Real Time Clock – RTC

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real Time Clock, RTC, includes an APB interface, a 24-bit count-up counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the Backup Domain except for the APB interface. The APB interface is located in the V_{DD15} power domain. Therefore, it is necessary to be isolated from the ISO signal that comes from the power control unit when the V_{DD15} power domain is powered off, that is when the device enters the Power-Down mode. The RTC counter is used as a wakeup timer to generate a system resume signal from the Power-Down mode.

Inter-integrated Circuit – I^2C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provide an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode with maskable address

The I^2C is an internal circuit allowing communication with an external I^2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I^2C module provides three data transfer rates: (1) 100 kHz in the Standard mode, (2) 400 kHz in the Fast mode and (3) 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I^2C bus is a bi-directional data line between the master and slave devices and is used for data transmission and reception. The I^2C also has an arbitration detect function and clock synchronization to prevent situations where more than one master attempts to transmit data to the I^2C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave mode
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave mode. The SPI interface uses 4 pins, which are the serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Asynchronous operating baud rate clock frequency up to (f_{PCLK}/16) MHz and synchronous operating rate clock frequency up to (f_{PCLK}/8) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8, or 9-bit character
  - Parity: Even, odd, or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8 × 9 bits for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous data transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes a transmitter FIFO, (TX_FIFO) and receiver FIFO (RX_FIFO). The software can detect a USART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud rate clock frequency up to (f_{PCLK}/16) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8, or 9-bit character
  - Parity: Even, odd, or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Cyclic Redundancy Check – CRC

- Support CRC16 polynomial: 0x8005,
  $X^{16}+X^{15}+X^{2}+1$
- Support CCITT CRC16 polynomial: 0x1021,
  $X^{16}+X^{12}+X^{5}+1$
- Support IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
  $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Supports PDMA to complete a CRC computation of a block of memory

The CRC calculation unit is an error detection technique test algorithm which is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, then this means that the data stream contains a data error.

Peripheral Direct Memory Access – PDMA

- 6 channels with trigger source grouping
- 8-/16-/32-bit width data transfer
- Supports Address increment, decrement or fixed mode
- 4-level programmable channel priority
- Auto reload mode
- Supports trigger source:
  SPI, USART, UART, I^2C, GPTM, PWM, AES and software request

The Peripheral Direct Memory Access controller, PDMA, moves data between the peripherals and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt service routine execution. It improves system performance as the software does not need to connect each data movement operation.

Hardware Divider – DIV

- Signed/unsigned 32-bit divider
- Operation in 8 clock cycles, Load in 1 clock cycle.
- Divide by zero error Flag.

The divider is the truncated division and need software trigger start single by control register

"START" bit , after 8 clock cycles, the divider calculate complete flag will be set to 1, and if divisor register data is zero, divide zero error flag will be set to 1.

Universal Serial Bus Device Controller – USB

- Complies with USB 2.0 full-speed (12 Mbps) specification
- On-chip USB full-speed transceiver
- 1 control endpoint (EP0) for control transfer
- 3 single-buffered endpoints for bulk and interrupt transfer
- 4 double-buffered endpoints for bulk, interrupt and isochronous transfer
- 1,024 bytes EP_SRAM used as the endpoint data buffers

The USB device controller is compliant with the USB 2.0 full-speed specification. There is one control endpoint known as Endpoint 0 and seven configurable endpoints. A 1024-byte SRAM is used as the endpoint buffer. Each endpoint buffer size is programmable using corresponding registers, which provides maximum flexibility for various applications. The integrated USB full-speed transceiver helps to minimize the overall system complexity and cost. The USB functional block also contains the resume and suspend feature to meet the requirements of low-power consumption.

Advanced Encryption Standard – AES-128

- Supports AES Encrypt / Decrypt Function
- Supports AES ECB/CBC/CTR mode
- Supports Key Size 128 bits
- Supports 4 words Initial Vector for CBC and CTR mode
- 4 × 32 bits AES data buffer
- Supports DMA Interface
- Supports Word Data Swap Function

The AES core supports encryption and decryption function. AES only supports 128 bits input data to do encryption or decryption. Hardware does not pad any bits of input data. Software need to do pad action at first.

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watchpoints

Package and Operation Temperature

- 24/33/46-pin QFN, 48-pin LQFP package
- Operation temperature range: -40 ˚C to +85 ˚C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F0008
Main Flash (KB)		63
Option Bytes Flash (KB)		1
SRAM (KB)		16
Timer	GPTM	1
	PWM	2
	BFTM	2
	RTC	1
	WDT	1
Communication	USB	1
	SPI	1
	USART	1
	UART	1
	I^2C	1
CRC-16/32		1
DIV		1
PDMA		6 channels
AES-128		1
EXTI		16
GPIO		Up to 42
CPU Frequency		Up to 60 MHz
Operating Voltage		1.65 V ~ 3.6 V
Operating Temperature		-40 °C ~ 85 °C
Package		24/33/46-pin QFN 48-pin LQFP

Block Diagram

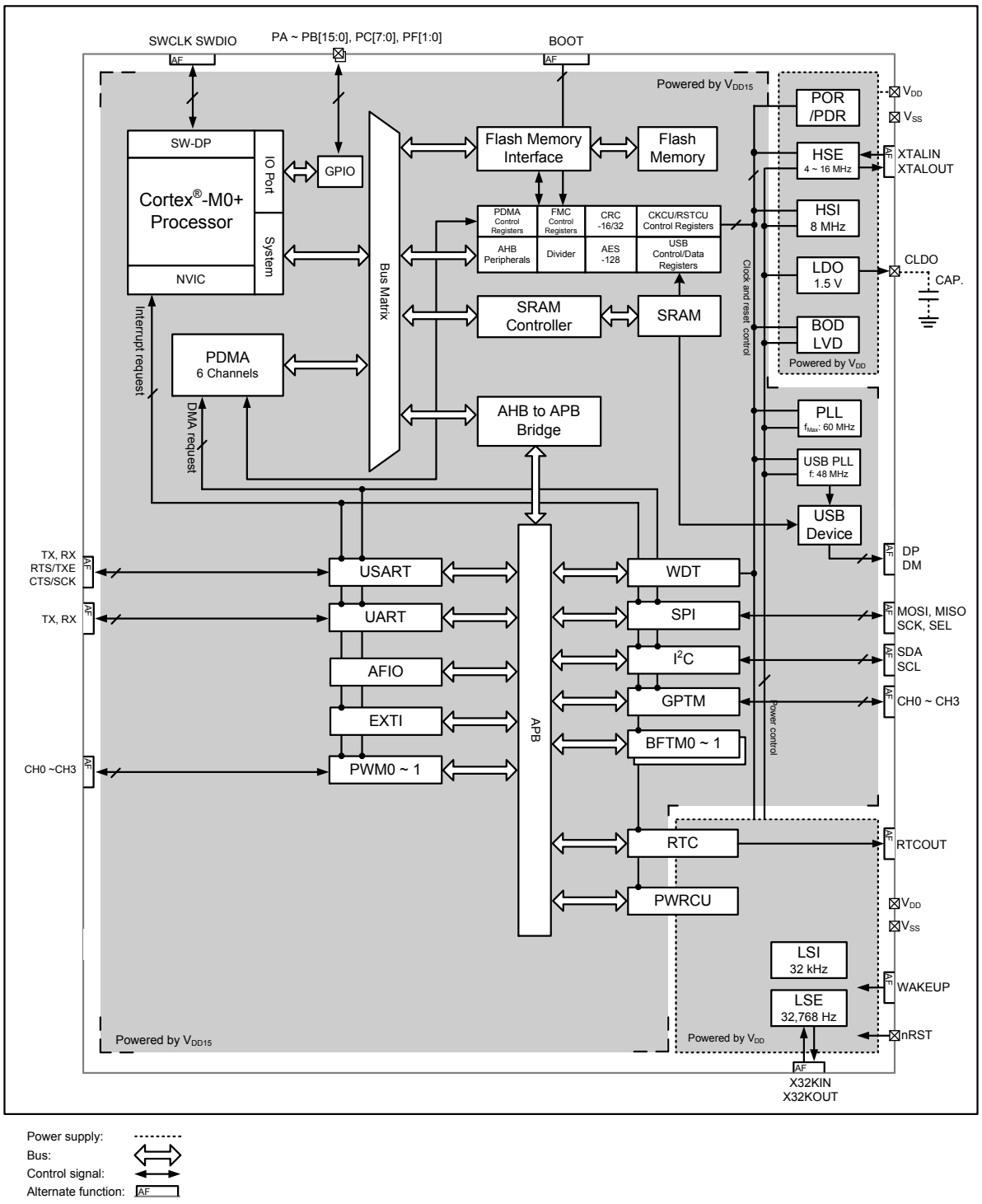


Figure 1. Block Diagram

Memory Map

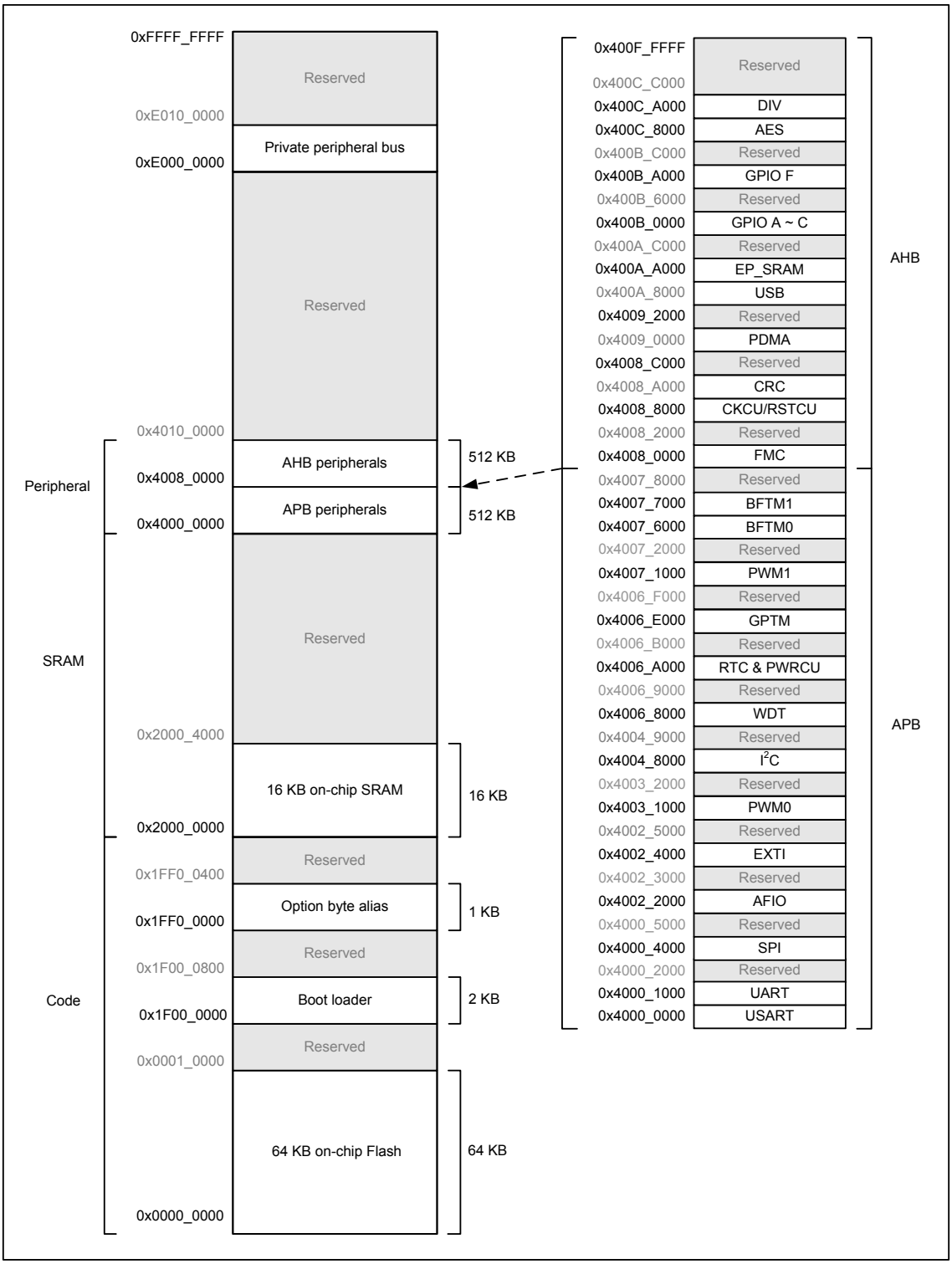


Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART	APB
0x4000_1000	0x4000_1FFF	UART	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI	
0x4000_5000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4003_0FFF	Reserved	
0x4003_1000	0x4003_1FFF	PWM0	
0x4003_2000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^2C	
0x4004_9000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC/PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_0FFF	Reserved	
0x4007_1000	0x4007_1FFF	PWM1	
0x4007_2000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	

Start Address	End Address	Peripheral	Bus
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU/RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x4008_FFFF	Reserved	
0x4009_0000	0x4009_1FFF	PDMA	
0x4009_2000	0x400A_7FFF	Reserved	
0x400A_8000	0x400A_BFFF	USB	
0x400A_C000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIO A	
0x400B_2000	0x400B_3FFF	GPIO B	
0x400B_4000	0x400B_5FFF	GPIO C	
0x400B_6000	0x400B_9FFF	Reserved	
0x400B_A000	0x400B_BFFF	GPIO F	
0x400B_C000	0x400C_7FFF	Reserved	
0x400C_8000	0x400C_9FFF	AES	
0x400C_A000	0x400C_BFFF	DIV	
0x400C_C000	0x400F_FFFF	Reserved	

Clock Structure

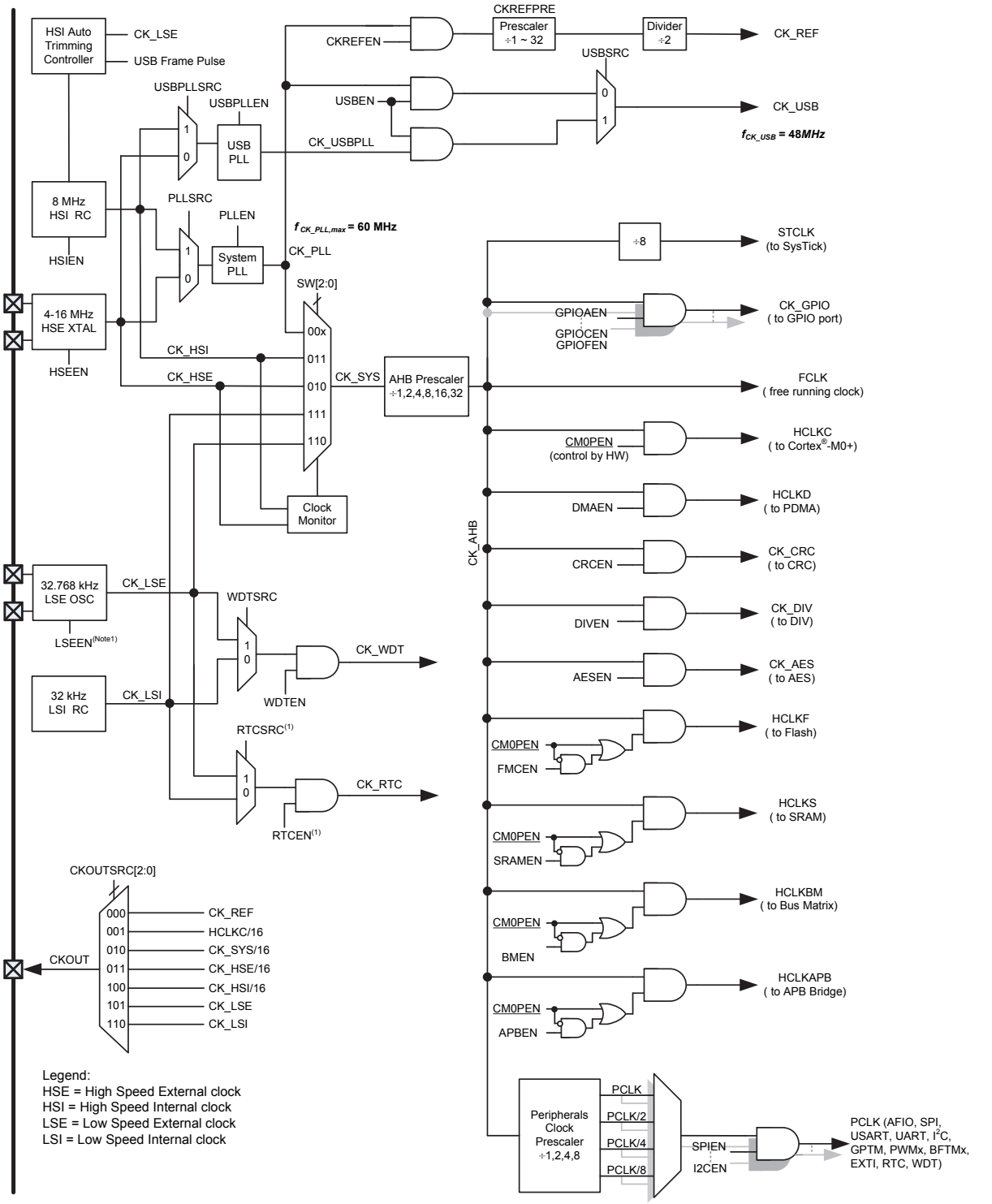


Figure 3. Clock Structure

4 Pin Assignment

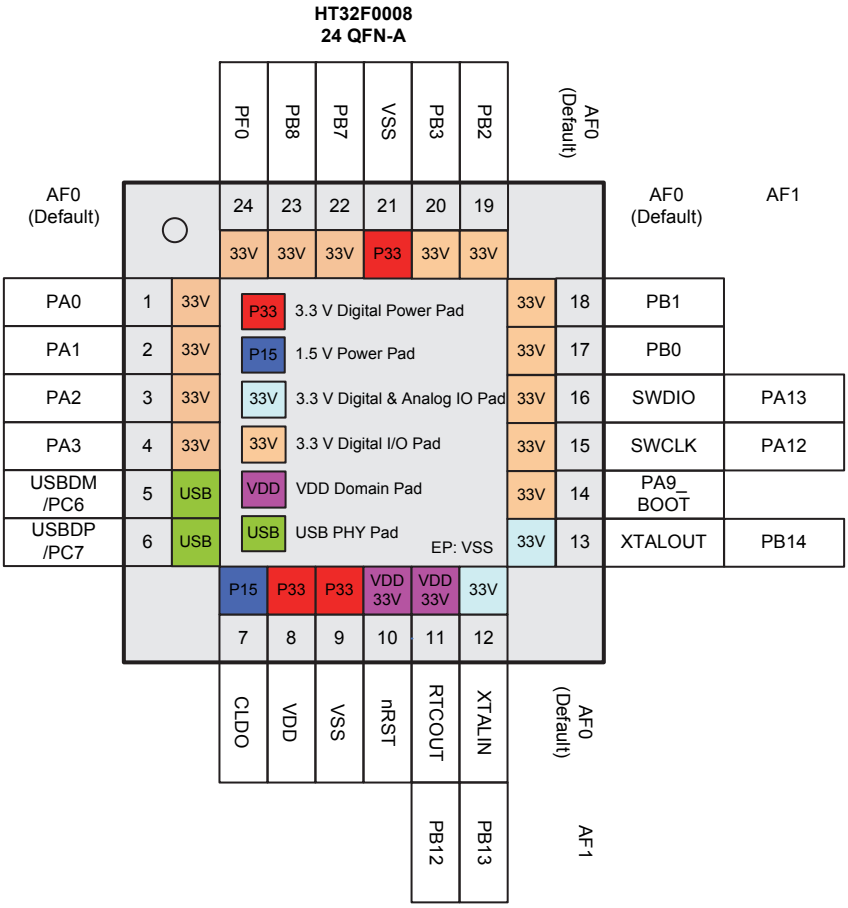


Figure 4. 24-pin QFN Pin Assignment

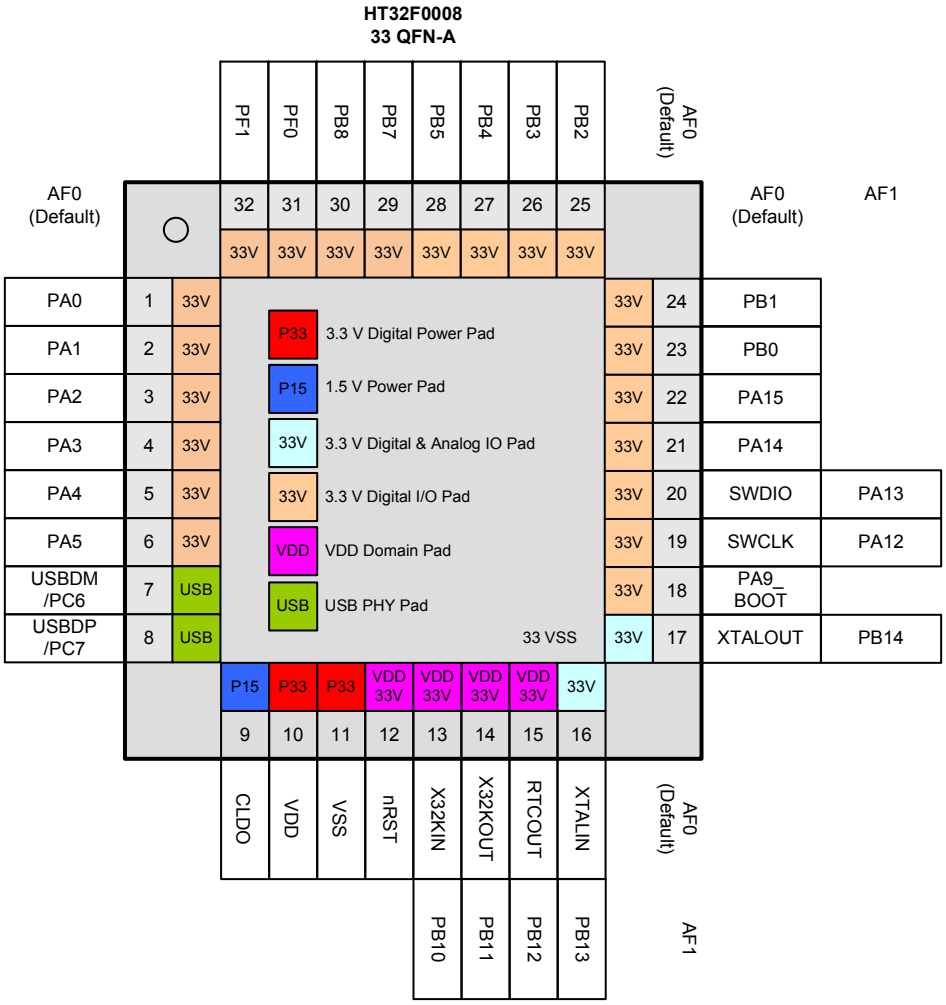


Figure 5. 33-pin QFN Pin Assignment

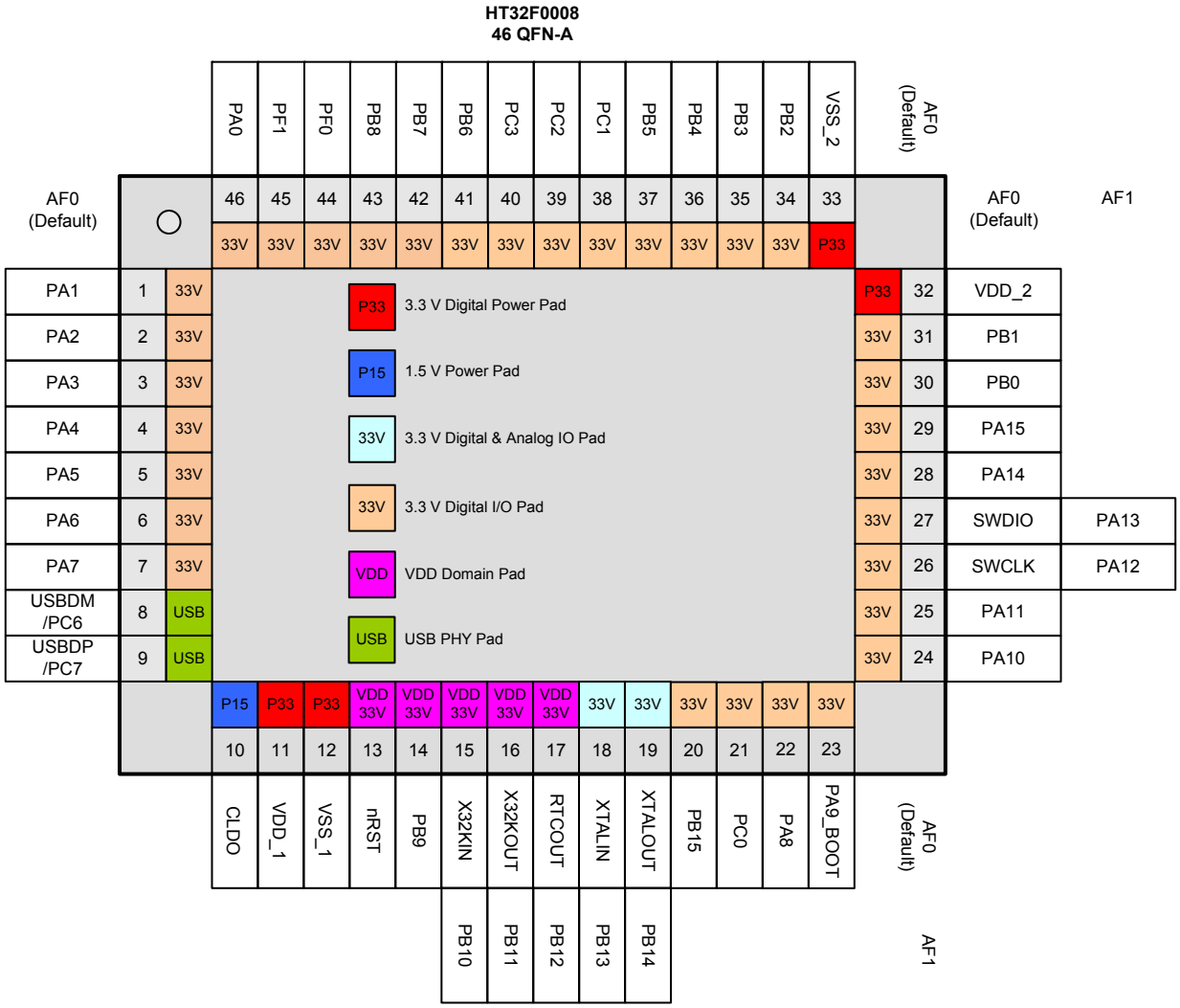


Figure 6. 46-pin QFN Pin Assignment

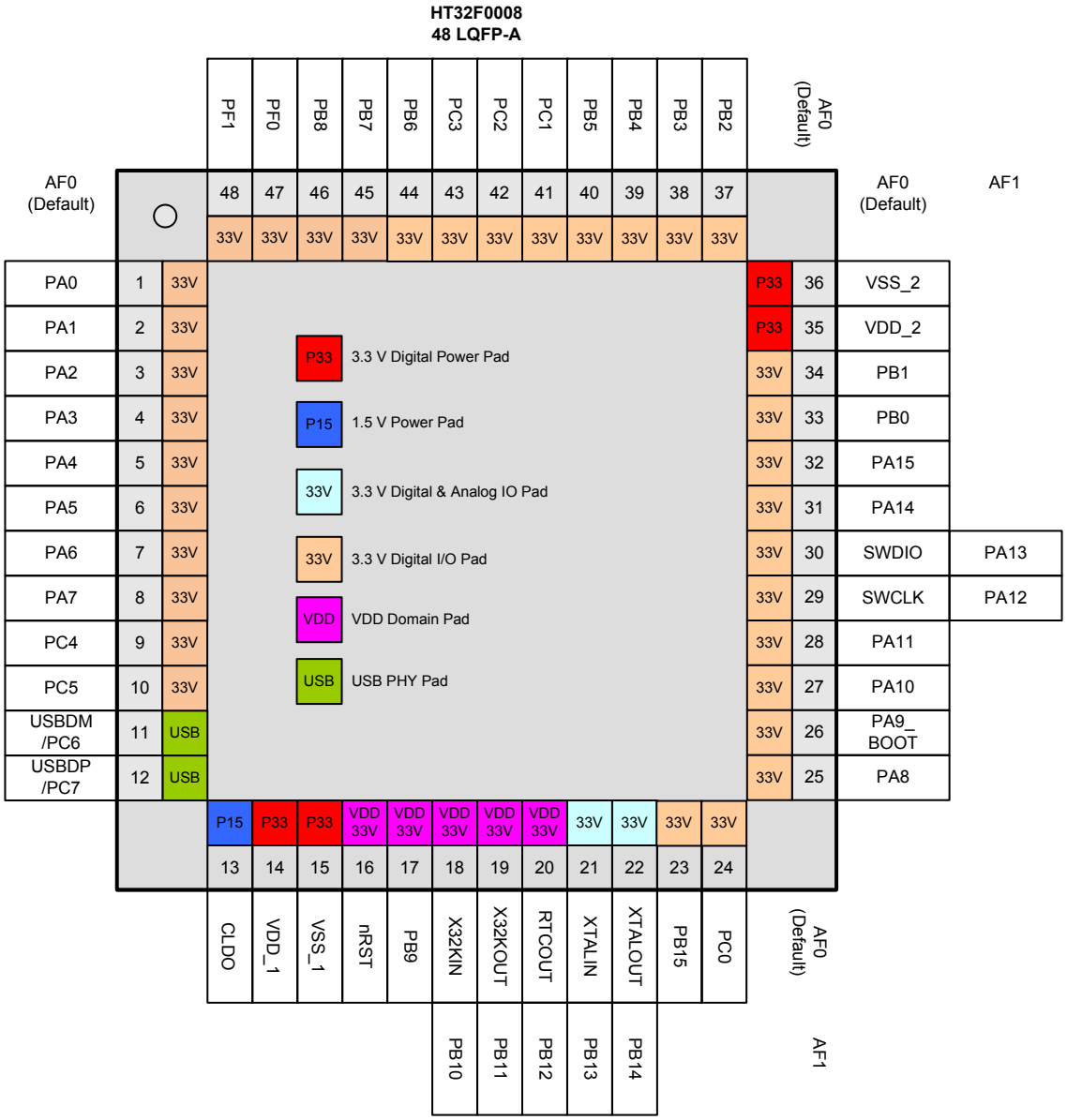


Figure 7. 48-pin LQFP Pin Assignment

Table 3. Pin Assignment for 24/33/46-pin QFN, 48-pin LQFP Package

Package				Alternate Function Mapping															
				AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
48 LQFP	46 QFN	33 QFN	24 QFN	System Default	GPIO	N/A	N/A	GPTM /PWM	SPI	USART /UART	I2C	N/A	N/A	N/A	N/A	N/A	N/A	N/A	System Other
1	46	1	1	PA0				GT_ CH0	SPI_ SCK	USR_ RTS	I2C_ SCL								
2	1	2	2	PA1				GT_ CH1	SPI_ MOSI	USR_ CTS	I2C_ SDA								
3	2	3	3	PA2				GT_ CH2	SPI_ MISO	USR_ TX									
4	3	4	4	PA3				GT_ CH3	SPI_ SEL	USR_ RX									
5	4	5		PA4				GT_ CH0	SPI_ SCK	UR_TX	I2C_ SCL								
6	5	6		PA5				GT_ CH1	SPI_ MOSI	UR_RX	I2C_ SDA								
7	6			PA6				GT_ CH2	SPI_ MISO										
8	7			PA7				GT_ CH3	SPI_ SEL										
9				PC4				PWM1_ CH0		USR_ TX									
10				PC5				PWM1_ CH1		USR_ RX									
11	8	7	5	PC6				GT_ CH0		USR_ TX	I2C_ SCL								
11	8	7	5	USBDM															
12	9	8	6	USBDP															
12	9	8	6	PC7				GT_ CH1		USR_ RX	I2C_ SDA								
13	10	9	7	CLDO															
14	11	10	8	VDD_1															
15	12	11	9	VSS_1															
16	13	12	10	nRST															
17	14			PB9				PWM1_ CH2											
18	15	13		X32KIN	PB10			GT_ CH0	SPI_ SEL	USR_ TX									
19	16	14		X32KOUT	PB11			GT_ CH1	SPI_ SCK	USR_ RX									
20	17	15	11	RTCOUT	PB12			PWM0_ CH0	SPI_ MISO	UR_RX									WAKEUP
21	18	16	12	XTALIN	PB13					UR_TX	I2C_ SCL								
22	19	17	13	XTALOUT	PB14					UR_RX	I2C_ SDA								
23	20			PB15				PWM0_ CH1	SPI_ SEL		I2C_ SCL								
24	21			PC0				PWM0_ CH2	SPI_ SCK		I2C_ SDA								
25	22			PA8				PWM1_ CH3		USR_ TX									
26	23	18	14	PA9_ BOOT				PWM1_ CH0	SPI_ MOSI										CKOUT
27	24			PA10				PWM0_ CH1	SPI_ MOSI	USR_ RX									

Package				Alternate Function Mapping															
				AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
48 LQFP	46 QFN	33 QFN	24 QFN	System Default	GPIO	N/A	N/A	GPTM /PWM	SPI	USART /UART	I2C	N/A	N/A	N/A	N/A	N/A	N/A	N/A	System Other
28	25			PA11				PWM0_ CH2	SPI_ MISO										
29	26	19	15	SWCLK	PA12														
30	27	20	16	SWDIO	PA13														
31	28	21		PA14				PWM0_ CH0	SPI_ SEL	USR_ RTS	I2C_ SCL								
32	29	22		PA15				PWM1_ CH2	SPI_ SCK	USR_ CTS	I2C_ SDA								
33	30	23	17	PB0				PWM0_ CH1	SPI_ MOSI	USR_ TX	I2C_ SCL								
34	31	24	18	PB1				PWM1_ CH1	SPI_ MISO	USR_ RX	I2C_ SDA								
35	32			VDD_2															
36	33	33	21	VSS_2															
37	34	25	19	PB2				PWM0_ CH2	SPI_ SEL	UR_TX									CKIN
38	35	26	20	PB3				PWM1_ CH2	SPI_ SCK	UR_RX									
39	36	27		PB4				PWM0_ CH3	SPI_ MOSI	UR_TX									
40	37	28		PB5				GT_ CH2	SPI_ MISO	UR_RX									
41	38			PC1				PWM0_ CH0	SPI_ SEL	UR_TX									
42	39			PC2				PWM1_ CH0	SPI_ SCK										
43	40			PC3				PWM1_ CH1	SPI_ MOSI	UR_RX									
44	41			PB6				GT_ CH3	SPI_ MISO	UR_TX									
45	42	29	22	PB7				PWM0_ CH3	SPI_ MISO	UR_TX	I2C_ SCL								
46	43	30	23	PB8				PWM1_ CH3	SPI_ SEL	UR_RX	I2C_ SDA								
47	44	31	24	PF0				GT_ CH2											
48	45	32		PF1				GT_ CH3											

Note: The pin number 33 of the 33QFN is located at the exposed pad of the QFN package.

Table 4. Pin Description

Pin Number				Pin Name	Type (1)	IO Structure (2)	Output Driving	Description
48 LQFP	46 QFN	33 QFN	24 QFN					Default Function (AF0)
1	46	1	1	PA0	I/O	33V	4/8/12/16 mA	PA0
2	1	2	2	PA1	I/O	33V	4/8/12/16 mA	PA1
3	2	3	3	PA2	I/O	33V	4/8/12/16 mA	PA2
4	3	4	4	PA3	I/O	33V	4/8/12/16 mA	PA3
5	4	5		PA4	I/O	33V	4/8/12/16 mA	PA4
6	5	6		PA5	I/O	33V	4/8/12/16 mA	PA5
7	6			PA6	I/O	33V	4/8/12/16 mA	PA6
8	7			PA7	I/O	33V	4/8/12/16 mA	PA7
9				PC4	I/O	33V	4/8/12/16 mA	PC4
10				PC5	I/O	33V	4/8/12/16 mA	PC5
11	8		5	PC6	I/O	33V	4/8/12/16 mA	PC6
11	8	7	5	USBDM	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
12	9	8	6	USBDP	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
12	9		6	PC7	I/O	33V	4/8/12/16 mA	PC7
13	10	9	7	CLDO	P	—	—	Core power LDO 1.5 V output It is recommended to connect a 2.2 μF capacitor as close as possible between this pin and VSS_1.
14	11	10	8	VDD_1	P	—	—	Voltage for digital I/O
15	12	11	9	VSS_1	P	—	—	Ground reference for digital I/O
16	13	12	10	nRST (3)	I	33V_PU	—	External reset pin and external wakeup pin in the Power-Down mode
17	14			PB9 (3)	I/O (V_{DD})	33V	4/8/12/16 mA	PB9
18	15	13		PB10 (3)	AI/O (V_{DD})	33V	4/8/12/16 mA	X32KIN
19	16	14		PB11 (3)	AI/O (V_{DD})	33V	4/8/12/16 mA	X32KOUT
20	17	15	11	PB12 (3)	I/O (V_{DD})	33V	4/8/12/16 mA	RTCOUT
21	18	16	12	PB13	AI/O	33V	4/8/12/16 mA	XTALIN
22	19	17	13	PB14	AI/O	33V	4/8/12/16 mA	XTALOUT
23	20			PB15	I/O	33V	4/8/12/16 mA	PB15
24	21			PC0	I/O	33V	4/8/12/16 mA	PC0
25	22			PA8	I/O	33V	4/8/12/16 mA	PA8
26	23	18	14	PA9	I/O	33V_PU	4/8/12/16 mA	PA9_BOOT
27	24			PA10	I/O	33V	4/8/12/16 mA	PA10
28	25			PA11	I/O	33V	4/8/12/16 mA	PA11
29	26	19	15	PA12	I/O	33V_PU	4/8/12/16 mA	SWCLK

Pin Number				Pin Name	Type (1)	IO Structure (2)	Output Driving	Description
48 LQFP	46 QFN	33 QFN	24 QFN					Default Function (AF0)
30	27	20	16	PA13	I/O	33V_PU	4/8/12/16 mA	SWDIO
31	28	21		PA14	I/O	33V	4/8/12/16 mA	PA14
32	29	22		PA15	I/O	33V	4/8/12/16 mA	PA15
33	30	23	17	PB0	I/O	33V	4/8/12/16 mA	PB0
34	31	24	18	PB1	I/O	33V	4/8/12/16 mA	PB1
35	32			VDD_2	P	—	—	Voltage for digital I/O
36	33	33	21	VSS_2	P	—	—	Ground reference for digital I/O
37	34	25	19	PB2	I/O	33V	4/8/12/16 mA	PB2
38	35	26	20	PB3	I/O	33V	4/8/12/16 mA	PB3
39	36	27		PB4	I/O	33V	4/8/12/16 mA	PB4
40	37	28		PB5	I/O	33V	4/8/12/16 mA	PB5
41	38			PC1	I/O	33V	4/8/12/16 mA	PC1
42	39			PC2	I/O	33V	4/8/12/16 mA	PC2
43	40			PC3	I/O	33V	4/8/12/16 mA	PC3
44	41			PB6	I/O	33V	4/8/12/16 mA	PB6
45	42	29	22	PB7	I/O	33V	4/8/12/16 mA	PB7
46	43	30	23	PB8	I/O	33V	4/8/12/16 mA	PB8
47	44	31	24	PF0	I/O	33V	4/8/12/16 mA	PF0
48	45	32		PF1	I/O	33V	4/8/12/16 mA	PF1

Note: 1. I = input, O = output, A = Analog port, P = power supply, PU = pull-up, V_{DD} = V_{DD} Power.
2. 33 V = 3.3 V tolerant.
3. These pins are located at the V_{DD} power domain.

5 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	External Main Supply Voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input Voltage On I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
T_A	Ambient Operating Temperature Range	-40	+85	°C
T_{STG}	Storage Temperature Range	-55	+150	°C
T_J	Maximum Junction Temperature	—	+125	°C
P_D	Total Power Dissipation	—	500	mW
V_{ESD}	Electrostatic Discharge Voltage – Human Body Mode	-4000	+4000	V

Recommended DC Operating Conditions

Table 6. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	I/O Operating Voltage	—	1.65	3.3	3.6	V

On-Chip LDO Voltage Regulator Characteristics

Table 7. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	V_{DD} ≥ 1.65 V Regulator input @ I_{LDO} = 10 mA and voltage variant = ±5 %, After trimming	1.425	1.5	1.57	V
I_{LDO}	Output Current	V_{DD} = 2.0 ~ 3.6 V Regulator input @ V_{LDO} = 1.5 V	—	30	35	mA
		V_{DD} = 1.65 ~ 2.0 V Regulator input @ V_{LDO} = 1.5 V	—	20	25	
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	μF

Power Consumption

Table 8. Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current (Run Mode)	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 60 MHz, f_{PCLK} = 60 MHz, All peripherals enabled	—	14	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 60 MHz, f_{PCLK} = 60 MHz, All peripherals disabled	—	6.8	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 40 MHz, f_{PCLK} = 40 MHz, All peripherals enabled	—	11.2	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 40 MHz, f_{PCLK} = 40 MHz, All peripherals disabled	—	6.5	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 20 MHz, f_{PCLK} = 20 MHz, All peripherals enabled	—	5.8	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 20 MHz, f_{PCLK} = 60 MHz, All peripherals disabled	—	3.2	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL off, f_{HCLK} = 8 MHz, f_{PCLK} = 8 MHz, All peripherals enabled	—	3.8	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL off, f_{HCLK} = 8 MHz, f_{PCLK} = 8 MHz, All peripherals disabled	—	1.4	—	mA
		V_{DD} = 3.3 V, HSI off, PLL off, LSI on, f_{HCLK} = 32 kHz, f_{PCLK} = 32 kHz, All peripherals enabled	—	23	—	μA
		V_{DD} = 3.3 V, HSI off, PLL off, LSI on, f_{HCLK} = 32 kHz, f_{PCLK} = 32 kHz, All peripherals disabled	—	19.5	—	μA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current (Sleep Mode)	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 60 MHz, All peripherals enabled	—	9.0	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 60 MHz, All peripherals disabled	—	1.2	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 40 MHz, All peripherals enabled	—	6.2	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 40 MHz, All peripherals disabled	—	1.0	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 20 MHz, All peripherals enabled	—	3.7	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 20 MHz, All peripherals disabled	—	0.8	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL off, f_{HCLK} = 0 MHz, f_{PCLK} = 8 MHz, All peripherals enabled	—	2.9	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL off, f_{HCLK} = 0 MHz, f_{PCLK} = 8 MHz, All peripherals disabled	—	0.5	—	mA
	Supply Current (Deep-Sleep1 Mode)	V_{DD} = 3.3 V, All clock off (HSI/PLL/f_{HCLK}), LDO in low power mode, LSI on, RTC on	—	16	—	μA
	Supply Current (Deep-Sleep2 Mode)	V_{DD} = 3.3 V, All clock off (HSI/PLL/f_{HCLK}), LDO off DMOS on, LSI on, RTC on	—	4.0	—	μA
	Supply Current (Power-Down Mode)	V_{DD} = 3.3 V, LDO off, DMOS off, LSE on, RTC on, LSI on	—	2.7	—	μA
		V_{DD} = 3.3 V, LDO off, DMOS off, LSE off, RTC off, LSI on	—	1.1	—	μA

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
3. RTC means real time clock.
4. Code = while (1) { 208 NOP } executed in Flash.

Reset and Supply Monitor Characteristics

Table 9. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	T_A = -40 °C~ 85 °C	0.6	—	3.6	V
V_{POR}	Power On Reset Threshold (Rising Voltage On V_{DD})	T_A = -40 °C~ 85 °C	1.40	1.55	1.65	V
V_{PDR}	Power Down Reset Threshold (Falling Voltage On V_{DD})	T_A = -40 °C~ 85 °C	1.27	1.45	1.57	V
$V_{PORHYST}$	POR Hysteresis	—	—	100	—	mV
t_{POR}	Reset Delay Time	V_{DD} = 3.3 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.
3. If the LDO is turned on, the VDD POR has to be in the de-assertion condition. When the VDD POR is in the assertion state then the LDO will be turned off.

Table 10. LVD/BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown Out Detection	After factory-trimmed	V_{DD} Falling edge	1.62	1.68	1.74	V
			V_{DD} Rising edge	1.68	1.74	1.8	
$V_{BODHTST}$	BOD Hysteresis	V_{DD} = 2.0 V	—	—	60	—	mV
V_{LVD}	Voltage of Low Voltage Detection	V_{DD} Falling edge	LVDS = 000	1.67	1.75	1.83	V
			LVDS = 001	1.87	1.95	2.03	V
			LVDS = 010	2.07	2.15	2.23	V
			LVDS = 011	2.27	2.35	2.43	V
			LVDS = 100	2.47	2.55	2.63	V
			LVDS = 101	2.67	2.75	2.83	V
			LVDS = 110	2.87	2.95	3.03	V
			LVDS = 111	3.07	3.15	3.23	V
$V_{LVDHTST}$	LVD Hysteresis	V_{DD} = 3.3 V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 3.3 V	—	—	—	5	μs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 3.3 V	—	—	—	—	μs
I_{DDLVD}	Operation Current (3)	V_{DD} = 3.3 V	—	—	5	15	μA

Note: 1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.
3. Bandgap current is not included.
4. LVDS field is in the PWRCU LVDCSR register.

External Clock Characteristics

Table 11. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	—	1.65	—	3.6	V
f_{HSE}	High Speed External Oscillator Frequency (HSE)	—	4	—	16	MHz
C_{LHSE}	Load Capacitance	V_{DD} = 3.3 V, R_{ESR} = 100 Ω @ 16 MHz	—	—	22	pF
R_{FHSE}	Internal Feedback Resistor Between XTALIN and XTALOUT Pins	—	—	1	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 3.3 V, C_L = 12 pF @ 16 MHz, HSEDR = 0 V_{DD} = 2.4 V, C_L = 12 pF @ 16 MHz, HSEDR = 1	—	—	160	Ω
D_{HSE}	HSE Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	V_{DD} = 3.3 V @ 16 MHz	—	TBD	—	mA
I_{PWDHSE}	HSE Oscillator Power Down Current	V_{DD} = 3.3 V	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	V_{DD} = 3.3 V	—	—	4	ms

Table 12. Low Speed External Clock (LSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	—	1.65	—	3.6	V
f_{CK_LSE}	LSE Frequency	V_{BAK} = 1.65 V ~ 3.6 V	—	32.768	—	kHz
R_F	Internal Feedback Resistor	—	—	10	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{BAK} = 3.3 V	30	—	TBD	kΩ
C_L	Recommended Load Capacitances	V_{BAK} = 3.3 V	6	—	TBD	pF
I_{DDLSE}	Oscillator Supply Current (High Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, $C_L \geq$ 7 pF, V_{DD} = 1.65 V ~ 2.7 V, T_A = -40 °C ~ +85 °C	—	3.3	6.3	μA
	Oscillator Supply Current (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, $C_L <$ 7 pF, V_{DD} = 1.65 V ~ 3.6 V, T_A = -40 °C ~ +85 °C	—	1.8	3.3	μA
	Power Down Current	—	—	—	0.01	μA
t_{suLSE}	Startup Time (Low Current Mode)	f_{CK_LSI} = 32.768 kHz, V_{DD} = 1.65 V ~ 3.6 V	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE / LSE clock in the PCB layout:

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace lengths as short as possible to reduce any parasitic capacitance.

2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep any high frequency signal lines away from the crystal area to prevent any crosstalk adverse effects.

Internal Clock Characteristics

Table 13. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	—	1.65	—	3.6	V
f_{HSI}	HSI Frequency	V_{DD} = 3.3 V, T_A = 25 °C	—	8	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V_{DD} = 3.3 V, T_A = 25 °C	-2	—	2	%
		V_{DD} = 2.5 V ~ 3.6 V, T_A = -40 °C ~ +85 °C	-3	—	3	%
		V_{DD} = 1.65 V ~ 3.6 V T_A = -40 °C ~ +85 °C	-6	—	6	%
Duty	Duty Cycle	f_{HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	Oscillator Supply Current	f_{HSI} = 8 MHz	—	300	500	μA
	Power Down Current		—	—	0.05	μA
t_{suHSI}	Startup Time	f_{HSI} = 8 MHz	—	—	10	μs

Table 14. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	—	1.65	—	3.6	V
f_{LSI}	Low Speed Internal Oscillator Frequency (LSI)	V_{DD} = 3.3 V, T_A = -40 °C ~ +85 °C	21	32	43	kHz
ACC_{LSI}	LSI Frequency Accuracy	After factory-trimmed, V_{DD} = 3.3 V, T_A = 25 °C	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 3.3 V, T_A = 25 °C	—	0.4	0.8	μA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 3.3 V, T_A = 25 °C	—	—	100	μs

PLL Characteristics

Table 15. PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	PLL Output Clock	—	16	—	60	MHz
t_{LOCK}	PLL Lock Time	—	—	200	—	μs

USB PLL Characteristics

Table 16. USB PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	PLL Output Clock	—	16	—	48	MHz
t_{LOCK}	PLL Lock Time	—	—	200	—	μs

Memory Characteristics

Table 17. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number Of Guaranteed Program/Erase Cycles Before Failure (Endurance)	T_A = -40 °C ~ +85 °C	10	—	—	k cycles
t_{RET}	Data Retention Time	T_A = -40 °C ~ +85 °C	10	—	—	Years
t_{PROG}	Word Programming Time	T_A = -40 °C ~ +85 °C	20	—	—	μs
t_{ERASE}	Page Erase Time	T_A = -40 °C ~ +85 °C	2	—	—	ms
t_{MERASE}	Mass Erase Time	T_A = -40 °C ~ +85 °C	10	—	—	ms

I/O Port Characteristics

Table 18. I/O Port Characteristics

V_{DD} = 3.3 V, T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	3.3 V IO	V_I = V_{SS}, On-chip pull-up resister disabled.	—	—	3	μA
		Reset pin		—	—	3	μA
I_{IH}	High Level Input Current	3.3 V IO	V_I = V_{DD}, On-chip pull-down resister disabled.	—	—	3	μA
		Reset pin		—	—	3	μA
V_{IL}	Low Level Input Voltage	3.3 V IO		-0.5	—	V_{DD} × 0.35	V
		Reset pin		-0.5	—	V_{DD} × 0.35	V
V_{IH}	High Level Input Voltage	3.3 V IO		V_{DD} × 0.65	—	V_{DD} + 0.5	V
		Reset pin		V_{DD} × 0.65	—	V_{DD} + 0.5	V
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	3.3 V IO		—	0.12 × V_{DD}	—	mV
		Reset pin		—	0.12 × V_{DD}	—	mV

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{OL}	Low Level Output Current (GPIO Sink Current)	3.3 V IO 4 mA drive, V_{OL} = 0.4 V	4	—	—	mA
		3.3 V IO 8 mA drive, V_{OL} = 0.4 V	8	—	—	mA
		3.3 V IO 12 mA drive, V_{OL} = 0.4 V	12	—	—	mA
		3.3 V IO 16 mA drive, V_{OL} = 0.4 V	16	—	—	mA
I_{OH}	High Level Output Current (GPIO Source Current)	3.3 V I/O 4 mA drive, V_{OH} = V_{DD} - 0.4 V	4	—	—	mA
		3.3 V I/O 8 mA drive, V_{OH} = V_{DD} - 0.4 V	8	—	—	mA
		3.3 V I/O 12 mA drive, V_{OH} = V_{DD} - 0.4 V	12	—	—	mA
		3.3 V I/O 16 mA drive, V_{OH} = V_{DD} - 0.4 V	16	—	—	mA
V_{OL}	Low Level Output Voltage	3.3 V 4 mA drive IO, I_{OL} = 4 mA	—	—	0.4	V
		3.3 V 8 mA drive IO, I_{OL} = 8 mA	—	—	0.4	V
		3.3 V 12 mA drive IO, I_{OL} = 12 mA	—	—	0.4	V
		3.3 V 16 mA drive IO, I_{OL} = 16 mA	—	—	0.4	V
V_{OH}	High Level Output Voltage	3.3 V 4 mA drive IO, I_{OH} = 4 mA	V_{DD} - 0.4	—	—	V
		3.3 V 8 mA drive IO, I_{OH} = 8 mA	V_{DD} - 0.4	—	—	V
		3.3 V 12 mA drive IO, I_{OH} = 12 mA	V_{DD} - 0.4	—	—	V
		3.3 V 16 mA drive IO, I_{OH} = 16 mA	V_{DD} - 0.4	—	—	V
R_{PU}	Internal Pull-Up Resistor	3.3 V I/O, V_{DD} = 3.3 V	—	60	—	kΩ
R_{PD}	Internal Pull-Down Resistor	3.3 V I/O, V_{DD} = 3.3 V	—	60	—	kΩ

PWM/GPTM Characteristics

Table 19. GPTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Frequency	—	—	—	f_{PCLK}	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	f_{TM}
f_{EXT}	External Single Frequency on Channel 1 ~ 4	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	bits

I²C Characteristics

Table 20. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL and SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL and SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time (Note 5)	0	—	0	—	0	—	ns
	SDA Data Hold Time (Note 6)	100	—	100	—	100	—	ns
$t_{VD(SDA)}$	SDA Data Valid Time	—	1.6	—	0.475	—	0.25	μs
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Guaranteed by design, not tested in production.
2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast mode plus, the peripheral clock frequency must be higher than 20 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: COMB_FILTER_En = 0 and SEQ_FILTER = 00.
6. The above characteristic parameters of the I²C bus timing are based on: COMB_FILTER_En = 1 and SEQ_FILTER = 00.

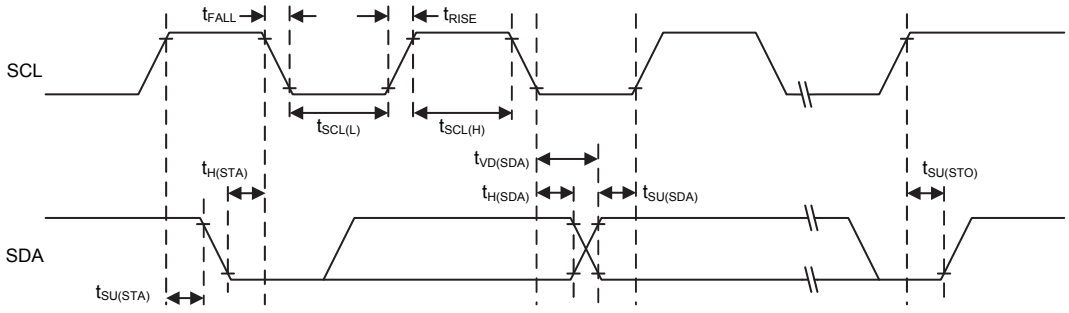


Figure 8. I²C Timing Diagrams

SPI Characteristics

Table 21. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK} ($1/t_{SCK}$)	SPI Master Output SCK Clock Frequency	Master mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High and Low Time	—	$t_{SCK}/2 - 2$	—	$t_{SCK}/2 + 1$	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
f_{SCK} ($1/t_{SCK}$)	SPI Slave Input SCK Clock Frequency	Slave mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	$3 \times t_{PCLK}$	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	$2 \times t_{PCLK}$	—	—	Ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	$3 \times t_{PCLK}$	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: $t_{SCK} = 1/f_{SCK}$; $t_{PCLK} = 1/f_{PCLK}$.
SPI output (input) clock frequency: f_{SCK};
SPI peripheral clock frequency: f_{PCLK}.

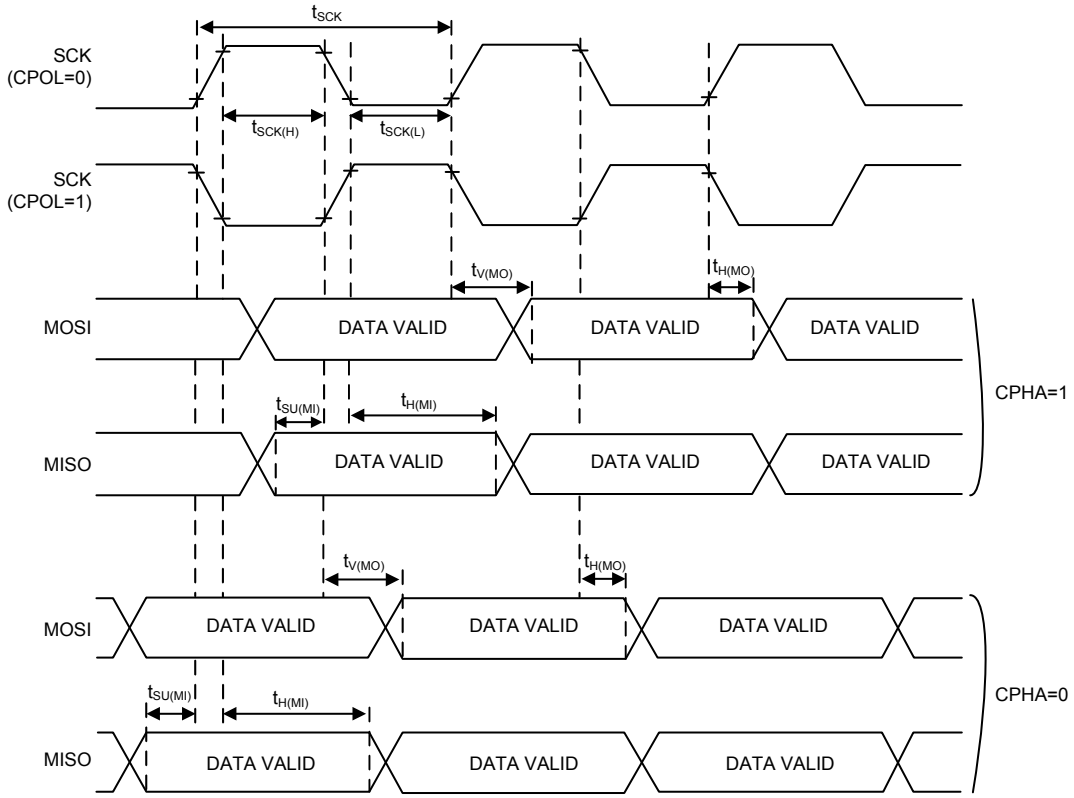


Figure 9. SPI Timing Diagrams – SPI Master Mode

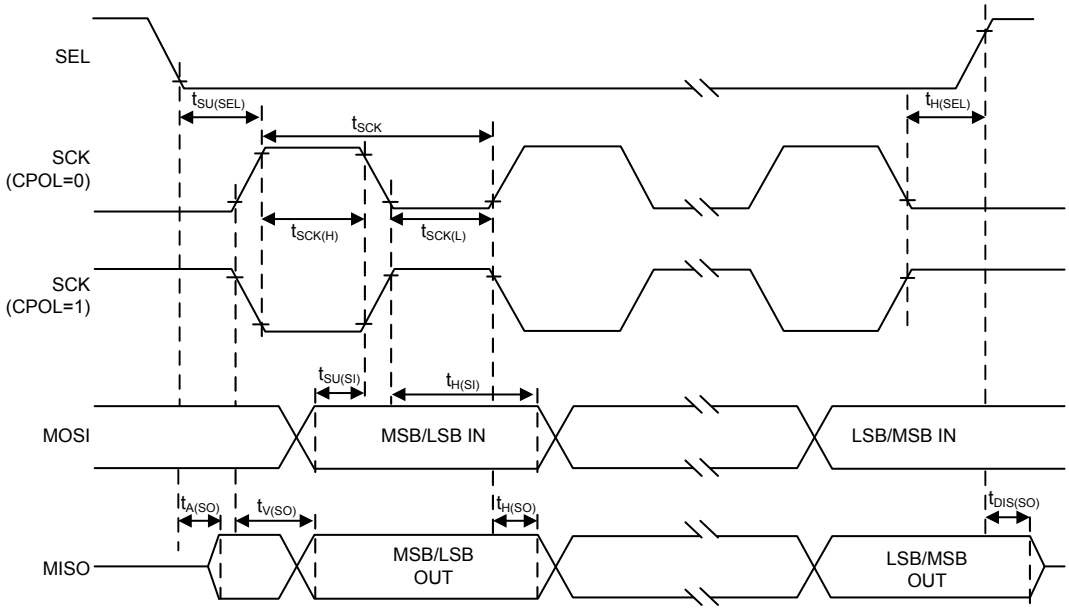


Figure 10. SPI Timing Diagrams – SPI Slave Mode with CPHA=1

USB Characteristics

The USB interface is USB-IF certified - Full Speed.

Table 22. USB DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	USB Operating Voltage	—	3.0	—	3.6	V
V_{DI}	Differential Input Sensitivity	|USBDP – USBDM|	0.2	—	—	V
V_{CM}	Common Mode Voltage Range	—	0.8	—	2.5	V
V_{SE}	Single-Ended Receiver Threshold	—	0.8	—	2.0	V
V_{OL}	Pad Output Low Voltage	R_L of 1.5 kΩ to V_{DD33}	0	—	0.3	V
V_{OH}	Pad Output High Voltage		2.8	—	3.6	V
V_{CRS}	Differential Output Signal Cross-Point Voltage		1.3	—	2.0	V
Z_{DRV}	Driver Output Resistance	—	—	10	—	Ω
C_{IN}	Transceiver Pad Capacitance	—	—	—	20	pF

Note: 1. Guaranteed by design, not tested in production.
2. The USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which will experience degradation in the 2.7 V to 3.0 V V_{DD} voltage range.
3. RL is the load connected to the USB driver USBDP.

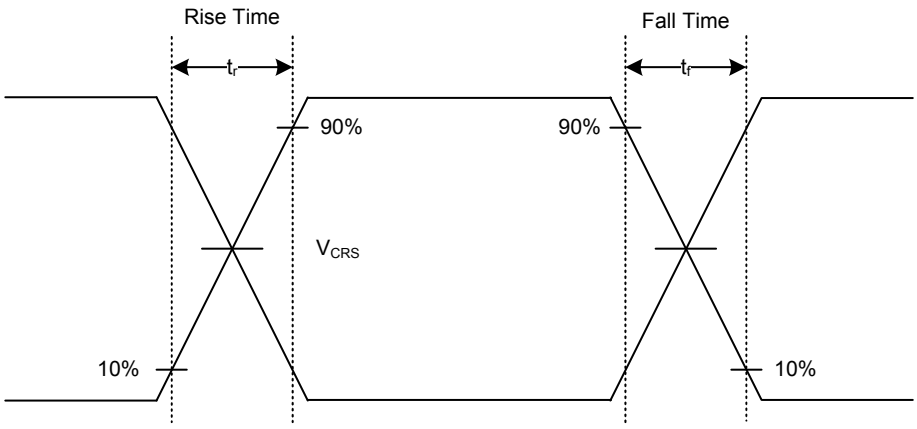


Figure 11. USB Signal Rise Time and Fall Time and Cross-Point Voltage (V_{CRS}) Definition

Table 23. USB AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_r	Rise Time	C_L = 50 pF	4	—	20	ns
t_f	Fall Time	C_L = 50 pF	4	—	20	ns
$t_{r/f}$	Rise Time / Fall Time Matching	$t_{r/f} = t_r / t_f$	90	—	110	%

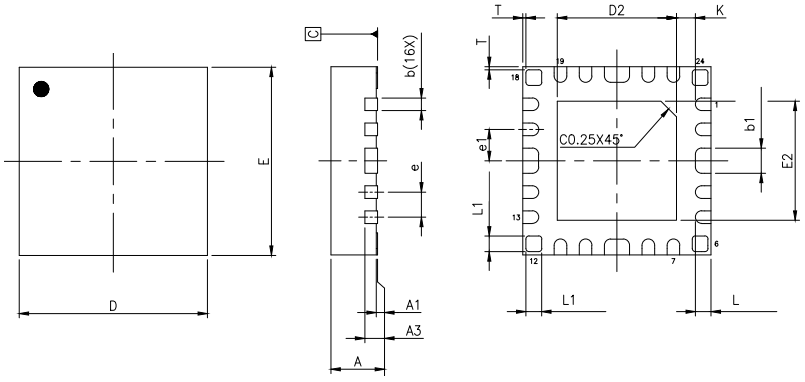
6 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

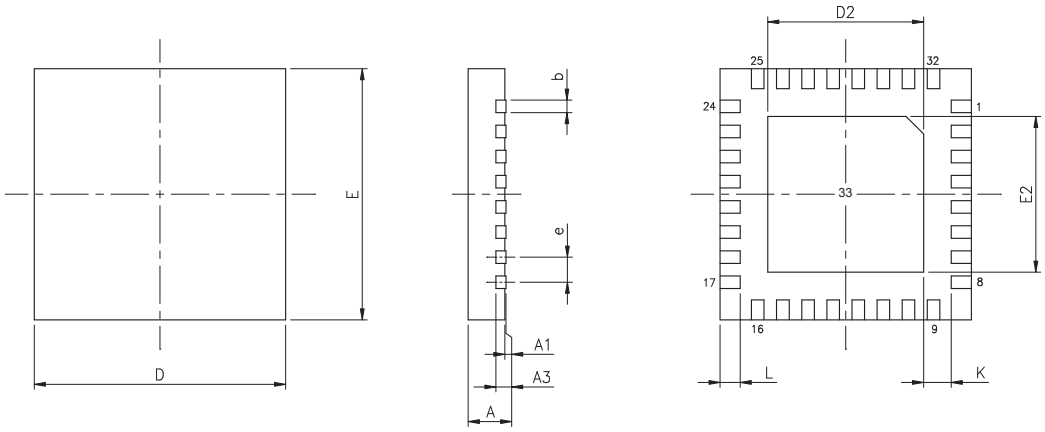
SAW Type 24-pin QFN (3mm×3mm×0.55mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.020	0.022	0.024
A1	0.000	0.001	0.002
A3	—	0.006 BSC	—
b	0.006	0.008	0.010
b1	0.014	0.016	0.018
D	—	0.118 BSC	—
E	—	0.118 BSC	—
e	—	0.016 BSC	—
e1	—	0.020 BSC	—
D2	0.073	0.075	0.077
E2	0.073	0.075	0.077
L	0.006	0.010	0.014
L1	0.008	0.010	0.012
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	—	0.150 BSC	—
b	0.15	0.20	0.25
b1	0.35	0.40	0.45
D	—	3.00 BSC	—
E	—	3.00 BSC	—
e	—	0.40 BSC	—
e1	—	0.50 BSC	—
D2	1.85	1.90	1.95
E2	1.85	1.90	1.95
L	0.15	0.25	0.35
L1	0.20	0.25	0.30
K	0.20	—	—

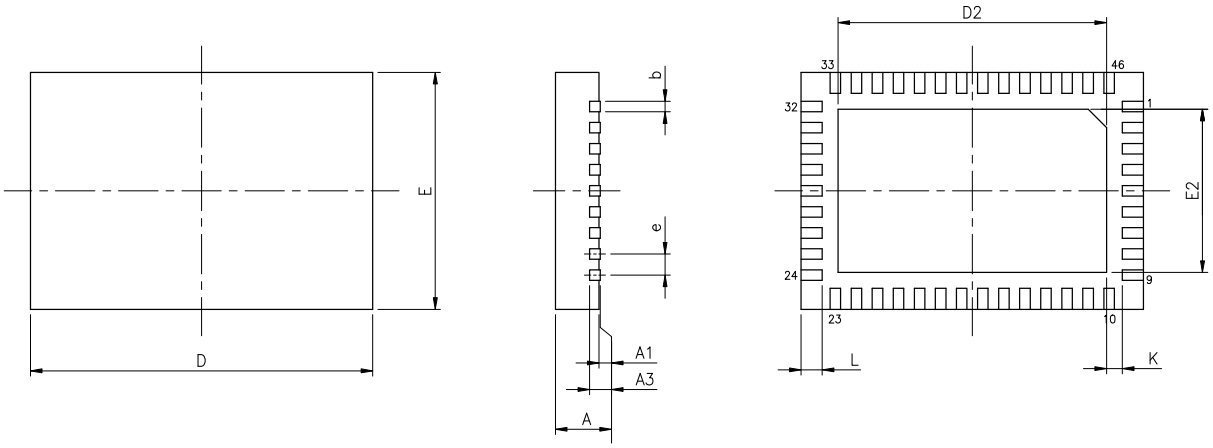
SAW Type 33-pin QFN (4mm×4mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.006	0.008	0.010
D	—	0.157 BSC	—
E	—	0.157 BSC	—
e	—	0.016 BSC	—
D2	0.104	0.106	0.108
E2	0.104	0.106	0.108
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	—	0.203 BSC	—
b	0.15	0.20	0.25
D	—	4.00 BSC	—
E	—	4.00 BSC	—
e	—	0.40 BSC	—
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
L	0.35	0.40	0.45
K	0.20	—	—

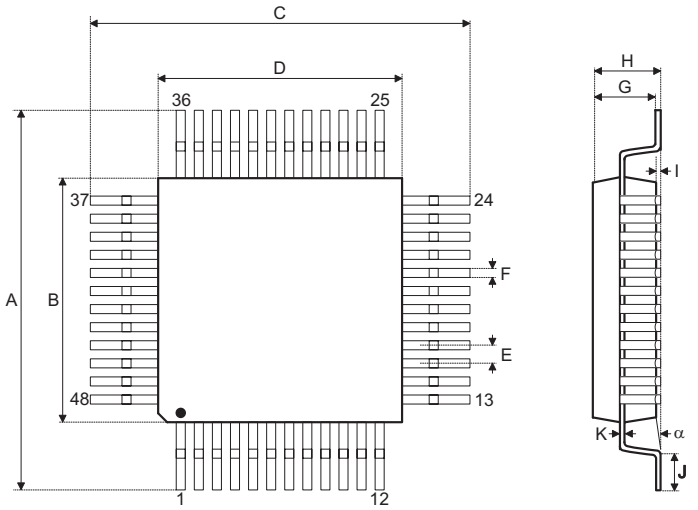
SAW Type 46-pin QFN (6.5mm×4.5mm×0.75mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.006	0.008	0.010
D	—	0.256 BSC	—
E	—	0.177 BSC	—
e	—	0.016 BSC	—
D2	0.199	0.201	0.203
E2	0.120	0.122	0.124
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	—	0.203 BSC	—
b	0.15	0.20	0.25
D	—	6.50 BSC	—
E	—	4.50 BSC	—
e	—	0.40 BSC	—
D2	5.05	5.10	5.15
E2	3.05	3.10	3.15
L	0.35	0.40	0.45
K	0.20	—	—

48-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.020 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.0 BSC	—
B	—	7.0 BSC	—
C	—	9.0 BSC	—
D	—	7.0 BSC	—
E	—	0.5 BSC	—
F	0.17	0.22	0.27
G	1.35	1.4	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°