



Sub-1GHz OOK/FSK/GFSK RF Transmitter

BC2113

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Features

- Frequency band: 315/433/470/868/915MHz
- OOK/FSK/GFSK modulation
- Supports 3-wire or 4-wire SPI interface
- Supports wide input voltage range of 1.8V~3.6V
- Programmable data rate
 - ♦ OOK: 0.5kbps~20kbps
 - ♦ FSK/GFSK: 0.5kbps~250kbps
- TX output power: +20dBm(Max.)
- Low current consumption
 - ♦ 0.25 μ A Deep Sleep mode current with data retention
 - ♦ TX current consumption @ 433.92MHz: 32mA @ 13dBm P_{OUT}
 - ♦ TX current consumption @ 868.3MHz: 35mA @ 13dBm P_{OUT}
- On-chip VCO and Fractional-N synthesizer with integrated loop filter
- Supports low cost 16MHz crystal
- Programmable digital channel filter for optimum performance at various data rates
- On-chip low power RC oscillator for WOT (Wake-On-TX) function
- Physical FIFO buffer: 64 bytes
- Simple FIFO/Block FIFO/Extend FIFO (up to 255 bytes)/Infinite FIFO modes
- Packet handling
 - ♦ FEC (Forward Error Correction)
 - ♦ Data whitening
 - ♦ Manchester encoding
 - ♦ CRC-16 generation/checking
- Auto-Transmit
 - ♦ Auto-Repeat-TX
 - ♦ WOT + Auto-Repeat-TX
- Package type: 16-pin QFN (3mm×3mm)

General Description

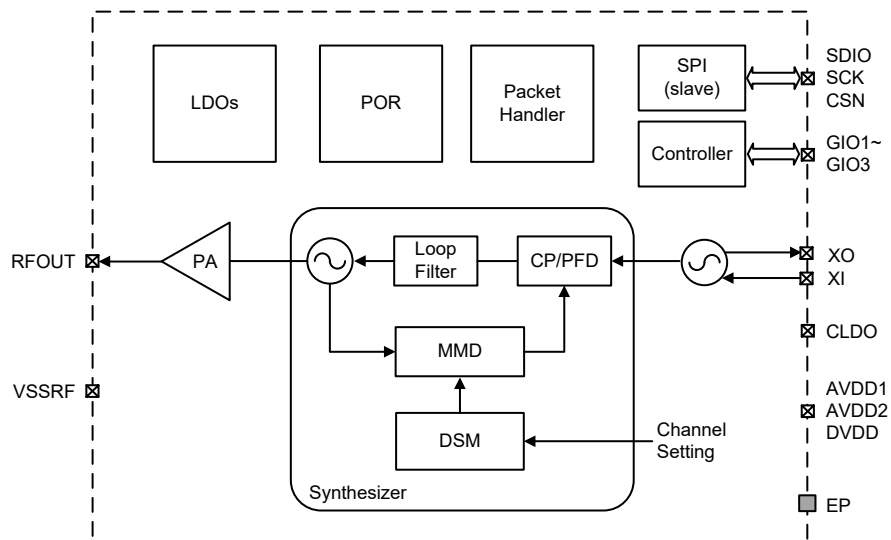
The BC2113 is a high-performance and low-cost OOK/FSK/GFSK transmitter for wireless applications in the 315MHz, 433MHz, 470MHz, 868MHz and 915MHz frequency bands. It incorporates a highly integrated sub-1GHz transmitter, a baseband modulator with programmable FSK/GFSK data rates from 0.5kbps to 250kbps and OOK data rates from 0.5kbps to 20kbps. Data handling features include 64-byte TX FIFO and packet handler module, such as CRC generation, Forward Error Correction, Data Whitening, and Manchester encoding.

The BC2113 is optimized for very low power consumption applications. At 433MHz band, it delivers +13dBm TX output power at 32mA current consumption. A Class-E Power Amplifier can deliver up to +20dBm output power at 433/868MHz bands. A fully integrated Fractional-N synthesizer can support a wide frequency range with a fine resolution. Both the loop filter and the internal programmable load capacitors for the crystal oscillator are integrated on-chip to minimize the requirement for external components.

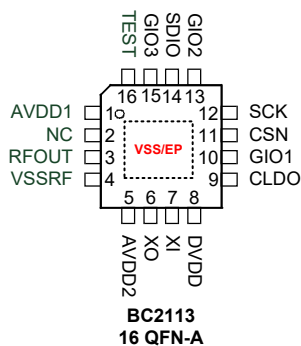
External host MCU can access the BC2113 through a 3-wire or 4-wire SPI interface. The device supports short strobe commands to reduce the loading of the host MCU while maintaining wireless communication link.

Additional link layer features like WOT facilitate microcontroller-based ISM-band wireless link applications.

Block Diagram



Pin Assignment



Pin Description

Pin No.	Pin Name	Type	Description
1	AVDD1	PWR	Analog power supply
2	NC	—	Not connected
3	RFOUT	AO	RF power amplifier output
4	VSSRF	PWR	RF ground
5	AVDD2	PWR	Analog power supply
6	XO	AO	Crystal oscillator output
7	XI	AI	Crystal oscillator input
8	DVDD	PWR	Digital power supply
9	CLDO	PWR	LDO output, connected to a bypass capacitor
10	GIO1	DI/O	Multi-function I/O 1
11	CSN	DI	SPI chip select input, low active
12	SCK	DI	SPI clock input
13	GIO2	DI/O	Multi-function I/O 2
14	SDIO	DI/O	SPI data input/output
15	GIO3	DI/O	Multi-function I/O 3
16	TEST	—	Analog test pin
—	VSS/EP ⁽¹⁾	PWR	Exposed pad, must be connected to ground

Legend: DI: Digital Input; DI/O: Digital Input/Output; AI: Analog Input; AO: Analog Output; PWR: Power

Note: 1. The VSS/EP pin is located at the exposed pad.

2. The backside plate of EP shall be well soldered to ground on PCB, otherwise it will downgrade RF performance.

Absolute Maximum Ratings

Supply Voltage	$V_{SS}-0.3V$ to $V_{SS}+3.6V$
Voltage on I/O Ports	$V_{SS}-0.3V$ to $V_{DD}+0.3V$
Storage Temperature.....	$-60^{\circ}C$ to $150^{\circ}C$
Operating Temperature.....	$-40^{\circ}C$ to $85^{\circ}C$
ESD HBM	$\pm 2kV$

The device is ESD sensitive. HBM (Human Body Mode) is based on MIL-STD-883.

Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C, V_{DD}=3.3V, f_{XTAL}=16MHz, FSK/GFSK modulation with matching circuit and low/high pass filter,
RF output is powered by V_{DD} (3.3V), unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T _{OP}	Operating Temperature	—	-40	—	85	°C
V _{DD}	Supply Voltage	—	1.8	3.3	3.6	V
Digital I/Os						
V _{IH}	High Level Input Voltage	—	0.7×V _{DD}	—	V _{DD}	V
V _{IL}	Low Level Input Voltage	—	0	—	0.3×V _{DD}	V
V _{OH}	High Level Output Voltage	I _{OH} =-5mA	0.8×V _{DD}	—	V _{DD}	V
V _{OL}	Low Level Output Voltage	I _{OL} =5mA	0	—	0.2×V _{DD}	V
Current Consumption						
I _{DeepSleep}	Deep Sleep Mode Current Consumption	—	—	0.25	—	μA
I _{IL}	Idle Mode Current Consumption	LIRC on, X'tal off	—	1.5	—	μA
I _{LightSleep}	Light Sleep Mode Current Consumption	X'tal on	—	0.6	—	mA
I _{Standby}	Standby Mode Current Consumption @ 315/433MHz	X'tal on, Synthesizer on	—	3.4	—	mA
	Standby Mode Current Consumption @ 868/915MHz		—	3.5	—	
I _{TX}	315MHz Band Current Consumption	TX mode @ 0dBm P _{OUT}	—	11	—	mA
		TX mode @ 10dBm P _{OUT}	—	25	—	
		TX mode @ 13dBm P _{OUT}	—	33	—	
		TX mode @ 20dBm P _{OUT}	—	66	—	
	433MHz Band Current Consumption	TX mode @ 0dBm P _{OUT}	—	11	—	mA
		TX mode @ 10dBm P _{OUT}	—	24	—	
		TX mode @ 13dBm P _{OUT}	—	32	—	
		TX mode @ 20dBm P _{OUT}	—	62	—	
	868MHz Band Current Consumption	TX mode @ 0dBm P _{OUT}	—	12	—	mA
		TX mode @ 10dBm P _{OUT}	—	25	—	
		TX mode @ 13dBm P _{OUT}	—	35	—	
		TX mode @ 20dBm P _{OUT}	—	71	—	
	915MHz Band Current Consumption	TX mode @ 0dBm P _{OUT}	—	12	—	mA
		TX mode @ 10dBm P _{OUT}	—	26	—	
		TX mode @ 13dBm P _{OUT}	—	35	—	
		TX mode @ 20dBm P _{OUT}	—	71	—	

A.C. Characteristics

Ta=25°C, V_{DD}=3.3V, f_{XTAL}=16MHz, FSK/GFSK modulation with matching circuit and low/high pass filter,
RF output is powered by V_{DD} (3.3V), unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
RF Characteristics						
f _{RF}	RF Frequency Band	315MHz band	—	315	—	MHz
		433MHz band	—	433.92	—	
		470~510MHz band	—	490	—	
		868MHz band	—	868.3	—	
		915MHz band	—	915	—	
DR	Data Rate	OOK modulation	0.5	—	20	kbps
		FSK/GFSK modulation	0.5	—	250	

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Transmitter						
P _{OUT}	TX Output Power	433MHz band	0	—	20	dBm
		868MHz band	0	—	20	
t _{ST,TX}	TX Settling Time	Light sleep mode to TX mode	—	120	—	μs
S.E.-TX	TX Spurious Emission (P _{OUT} =10dBm)	f < 1GHz	—	—	-36	dBm
		47MHz < f < 74MHz	—	—	-54	
		87.5MHz < f < 118MHz				
		174MHz < f < 230MHz				
		470MHz < f < 862MHz	—	—	-30	
2 nd , 3 rd Harmonic						
LO Characteristics						
f _{LO}	RF Frequency Coverage Range	315MHz band	290	—	335	MHz
		433MHz band	415	—	490	
		470~510MHz band	470	—	510	
		868MHz band	830	—	1000	
		915MHz band	870	—	1050	
f _{STEP}	LO Frequency Resolution	—	—	—	1	kHz
PN _{LO}	315MHz Phase Noise	@ 100kHz offset	—	-90	—	dBc/ Hz
		@ 1MHz offset	—	-110	—	
	433MHz Phase Noise	@ 100kHz offset	—	-89	—	
		@ 1MHz offset	—	-110	—	
	868MHz Phase Noise	@ 100kHz offset	—	-82	—	
		@ 1MHz offset	—	-105	—	
	915MHz Phase Noise	@ 100kHz offset	—	-82	—	
		@ 1MHz offset	—	-105	—	
Crystal Oscillator						
f _{XTAL}	Crystal (X'tal) Frequency ⁽¹⁾	—	—	16	—	MHz
ESR	X'tal Equivalent Series Resistance	—	—	—	100	Ω
C _{LOAD}	X'tal Capacitor Load	—	8	12	16	pF
TOL	X'tal Tolerance ⁽²⁾	—	-20	—	+20	ppm
t _{SU}	X'tal Startup Time ⁽³⁾	49US XO	—	1	—	ms
		3225SMD XO	—	2	—	
Internal Low Frequency Oscillator						
f _{LIRC}	Calibration Frequency	—	—	32768	—	Hz
t _{INI_CAL}	Initial Calibration Time	—	—	4	—	ms

Note: 1. BC2113 can use an external reference clock to drive the XI pin through a coupling capacitor.

2. The value is affected by crystal load, aging, and temperature variation.

When the data rate is 2kbps at 315/433MHz, the crystal shall be selected with ±10ppm tolerance.

When the data rate is 2kbps at 868/915MHz, the crystal shall be selected with ±5ppm tolerance.

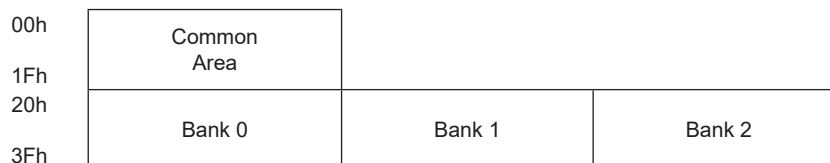
3. The parameter is related to the crystal used.

SPI Characteristics

Ta=-40°C~85°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f _{SCK}	SCK Frequency	—	—	4	8	MHz
t _{SCKH}	SCK High Time	—	62.5	125	—	ns
t _{SCKL}	SCK Low Time	—	62.5	125	—	ns
t _{S_SDIO}	SDIO Input Setup Time	—	62.5	—	—	ns
t _{H_SDIO}	SDIO Input Hold Time	—	62.5	—	—	ns
t _{S_CSN}	CSN Active to SCK Active	—	62.5	—	—	ns
t _{H_CSN}	SCK Inactive to CSN Inactive	—	62.5	—	—	ns

Memory Mapping



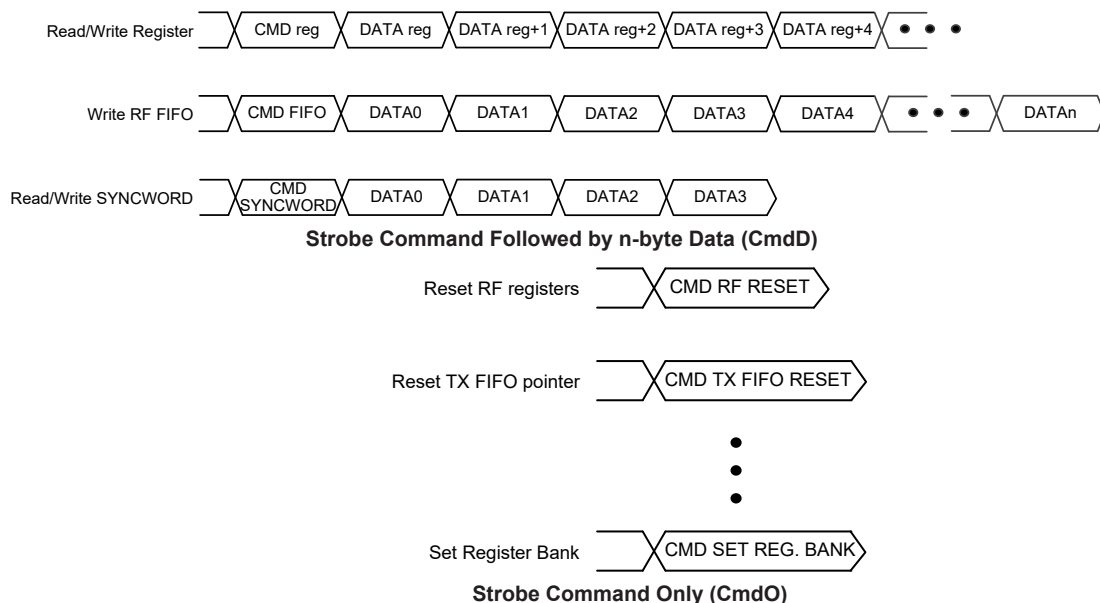
Common Area: It contains a 32-byte space. Accessing addresses 00h~1Fh always means accessing the Common Area regardless of the Bank Pointer configuration.

Bank 0~2: Each bank contains a 32-byte space. They are selected by the Bank Pointer.

The Bank Pointer (BANK[1:0]) which is defined in the Common Area control register, can be set directly by the Set Register Bank strobe command, or can be read/written by the Read/Write Register command.

Control Register Access

The host MCU can access the BC2113 control registers through two command formats: one is a 1-byte command only, referred to as CmdO; the other is a 1-byte command followed by n bytes of data, referred to as CmdD. For details, please refer to the description in the SPI Interface chapter.



SFR Mapping and Bit Definition

The BC2113 is configured and operated through a series of control registers. These registers are mapped to either the Common Area or one of the multiple Bank areas. The following sections describe these registers on a per-area basis.

Common Area Control Registers

All control registers will be set to their initial value by power-on reset (POR). The software reset will set the control registers to their initial value except the FSYCK_EN, FSYCK_DIV[1:0], PWRON, GIO1S[2:0], GIO2S[2:0], PADDS[1:0], GIO3S[3:0], GIOPU[3:1], SPIPU, SDO_TEN bits in the RC1, IO1, IO2 and IO3 registers. These bits keep unchanged after software reset.

Addr.	Name	Bit							
		7	6	5	4	3	2	1	0
00h	CFG1	OOK_EN	—	—	DIR_EN	—	—	BANK[1:0]	
01h	RC1	PWRON	FSYCK_RDY	XCLK_RDY	XCLK_EN	FSYCK_DIV[1:0]		FSYCK_EN	RST_LL
02h	IRQ1	—	—	—	—	—		IRQCPOR	IRQPOR
03h	IRQ2	—	ATXCTIE	FIFOLTIE	—	—	CALCMPIE	—	TXCMPIE
04h	IRQ3	—	ATXCTIF	FIFOLTIF	—	—	CALCMPIF	—	TXCMPIF
05h	RC2	—	—	—	—	—	—	—	XCLK_GEN
06h	IO1	PADDS[1:0]		GIO2S[2:0]			GIO1S[2:0]		
07h	IO2	—	—	—	—	GIO3S[3:0]			
08h	IO3	SDO_TEN	SPIPU	—	—	GIOPU[3:1]			—
09h	FIFO1	—	—	TXFFSA[5:0]					
0Ah	FIFO2	—	—	—	—	FFINF_EN	FFMG_EN	FFMG[1:0]	
0Bh	PKT1	TXPMLEN[7:0]							
0Ch	PKT2	PID[1:0]		TRAILER_EN	WHTFMT[0]	SYNCLEN[1:0]		CRC_RANGE	PREAMB_EN
0Dh	PKT3	MCH_EN	FEC_TYPE[1:0]		SYNC_MCH_EN	PLLEN_EN	PLHAC_EN	PLHLEN	PLH_EN
0Eh	PKT4	WHT_EN	WHTSD[6:0]						
0Fh	PKT5	TXDLEN[7:0]							
12h	PKT8	FEC_NIBBLE	PL_MLB	PLHA[5:0]					
13h	PKT9	PLHEA[7:0]							
14h	MOD1	DTR[7:0]							
15h	MOD2	DTR1[3:0]				DTR[11:8]			
16h	PKT20	—	—	LEN_NID_SWP	NODE_IDEN	NODE_IDLEN[1:0]		DITHER[1:0]	
17h	PKT21	CRC_POLYNOMIAL[7:0]							
18h	PKT22	CRC_POLYNOMIAL[15:8]							
19h	PKT23	NODE_ID_BYTE[31:24]							
1Ah	PKT24	NODE_ID_BYTE[23:16]							
1Bh	PKT25	NODE_ID_BYTE[15:8]							
1Ch	PKT26	NODE_ID_BYTE[7:0]							

Note: The addresses which are not listed in this table are reserved for future use; it is suggested not to change their initial values by any means.

The “Reset” value shown in the following register description tables are the results after a software reset (Strobe command).

• **CFG1: Configuration Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	OOK_EN	—	—	DIR_EN	—	—	BANK[1:0]	
R/W	R/W	—	—	R/W	—	—	R/W	
Reset	0	0	0	0	0	0	0	0

- Bit 7 **OOK_EN**: OOK mode enable
 0: FSK/GFSK mode
 1: OOK mode
 When using OOK modulation, refer to the “OOK Settings” chapter for configuration suggestion.
- Bit 6~5 Reserved, must be “00”
- Bit 4 **DIR_EN**: Direct mode enable
 0: TX data from packet handling hardware
 1: TX data from external MCU directly
- Bit 3~2 Reserved, must be “00”
- Bit 1~0 **BANK[1:0]**: Control register bank selection
 00: Bank 0
 01: Bank 1
 10: Bank 2
 11: Reserved
 This Bank selection can be set by either the Set Register Bank strobe command or register write.

• **RC1: Reset/Clock Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	PWRON	FSYCK_RDY	XCLK_RDY	XCLK_EN	FSYCK_DIV[1:0]		FSYCK_EN	RST_LL
R/W	R/W	R	R	R/W	R/W		R/W	R/W
POR	1	—	—	—	0	0	0	—
Reset	—	0	0	1	—	—	—	0

- Bit 7 **PWRON**: 3.3V power-on flag to indicate the first power-on event
 This bit is only set to 1 by power-on reset and not affected by the software reset strobe command. The user should write 0 to clear this flag, and can also use it to trigger first-time auto calibration in the Light Sleep mode when ACAL_EN=1.

- Bit 6 **FSYCK_RDY**: FSYCK clock ready flag (read only)
 0: Not ready
 1: Ready
 This bit is used to indicate whether the FSYCK clock is ready for operation.
- Bit 5 **XCLK_RDY**: XCLK clock ready flag (read only)
 0: Not ready
 1: Ready
 This bit is used to indicate whether the XCLK debounce counter is full and XCLK is ready for operation. Note that XCLK_RDY may not be stable for a certain period after exiting the Deep Sleep state.
- Bit 4 **XCLK_EN**: XCLK clock enable
 0: Disable
 1: Enable
 Setting this bit high will enable the XCLK path to the baseband block while clearing this bit to zero can save power if required. Note: The XCLK clock should be enabled when writing data to the FIFO.
- Bit 3~2 **FSYCK_DIV[1:0]**: FSYCK clock (XCLK division) selection (only reset by POR)
 00: 1/1 XCLK
 01: 1/2 XCLK
 10: 1/4 XCLK
 11: 1/8 XCLK
- Bit 1 **FSYCK_EN**: FSYCK clock enable (only reset by POR)
 0: Disable
 1: Enable
- Bit 0 **RST_LL**: Low voltage (1.2V) logic reset control
 0: Release reset
 1: Reset

• **IRQ1: Interrupt Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	IRQCPOR	IRQPOR
R/W	—	—	—	—	—	—	R/W	R/W
Reset	0	0	0	0	0	0	0	1

- Bit 7~2 Reserved, must be “000000”
- Bit 1 **IRQCPOR**: IRQ flag clear polarity selection
 0: Clear IRQ flag by writing 0 to the corresponding bit
 1: Clear IRQ flag by writing 1 to the corresponding bit
- Bit 0 **IRQPOR**: IRQ signal polarity selection
 0: Active low
 1: Active high

• **IRQ2: Interrupt Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	—	ATXCTIE	FIFOLTIE	—	—	CALCMPIE	—	TXCMPPIE
R/W	—	R/W	R/W	—	—	R/W	—	R/W
Reset	0	0	0	0	0	0	0	0

- Bit 7 Reserved, must be “0”
- Bit 6 **ATXCTIE**: ATX Cycle Timer (ATXCT Timer) IRQ Enable
 0: Disable
 1: Enable
- Bit 5 **FIFOLTIE**: FIFO Low Threshold IRQ Enable
 0: Disable
 1: Enable

- Bit 4~3 Reserved, must be “00”
- Bit 2 **CALCMPIE**: Calibration Complete IRQ Enable
0: Disable
1: Enable
- Bit 1 Reserved, must be “0”
- Bit 0 **TXCMPIE**: TX Complete IRQ Enable
0: Disable
1: Enable

• **IRQ3: Interrupt Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	—	ATXCTIF	FIFOLTIF	—	—	CALCMPIF	—	TXCMPIF
R/W	—	R/W	R/W	—	—	R/W	—	R/W
Reset	0	0	0	0	0	0	0	0

This register contains active-high IRQ flags indicating which interrupt sources triggered the IRQ. Reading this register returns the flag values. Each flag can be cleared by writing either 0 or 1 to its bit, as determined by the IRQCPOR bit.

- Bit 7 Reserved, must be “0”
- Bit 6 **ATXCTIF**: ATX Cycle Timer (ATXCT Timer) IRQ Flag
0: No request
1: Interrupt request
This flag will be set high when the ATXCT timer is full.
- Bit 5 **FIFOLTIF**: FIFO Low Threshold IRQ Flag
0: No request
1: Interrupt request
When in the Burst TX mode, if this flag is set high, it means that the TX FIFO data length is less than the FFMG setting threshold and the remaining TX data length is greater than the threshold.
- Bit 4~3 Reserved, must be “00”
- Bit 2 **CALCMPIF**: Calibration Complete IRQ Flag
0: No request
1: Interrupt request
If ACAL_EN=0, and the LIRC calibration is enabled by its individual enable bit (LIRCCAL_EN), the IRQ will be triggered upon LIRC calibration completion. If ACAL_EN=1, both VCO and RC calibrations are enabled, and the IRQ will be triggered when both are completed.
- Bit 1 Reserved, must be “0”
- Bit 0 **TXCMPIF**: TX Complete IRQ Flag
0: No request
1: Interrupt request

• **RC2: Reset/Clock Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	XCLK_GEN
R/W	—	—	—	—	—	—	—	R/W
Reset	0	0	0	0	0	0	0	1

- Bit 7~1 Reserved, must be “0000000”
- Bit 0 **XCLK_GEN**: XCLK gating enable
0: Normal XCLK
1: Gating XCLK

• **IO1: I/O Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	PADDS[1:0]		GIO2S[2:0]			GIO1S[2:0]		
R/W	R/W		R/W			R/W		
POR	0	1	0	0	0	0	0	0

Bit 7~6 **PADDS[1:0]**: PAD driving strength selection (only reset by POR)

00: 0.5mA

01: 1mA

10: 5mA

11: 10mA

Bit 5~3 **GIO2S[2:0]**: GIO2 pin function selection (only reset by POR)

000: No function, input

001: SDO, 4-wire SPI data, output

010: Reserved

011: TXD, direct mode TXD, input

100: DTXD, direct mode TXD, output

101: IRQ, interrupt request, output

110: ROSCi, ATX clock external input, input

111: TXD, data monitor, output, only supported in direct mode

Bit 2~0 **GIO1S[2:0]**: GIO1 pin function selection (only reset by POR)

000: No function, input

001: SDO, 4-wire SPI data, output

010: ATXCLK, output

011: TXD, direct mode TXD, input

100: TBCLK, TX bit clock, output

101: IRQ, interrupt request, output

110: ROSCi, ATX clock external input, input

111: TXD, data monitor, output, only supported in direct mode

• **IO2: I/O Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	GIO3S[3:0]			
R/W	—	—	—	—	R/W			
POR	0	0	0	0	0	0	0	0

Bit 7~4 Reserved, must be “0000”

Bit 3~0 **GIO3S[3:0]**: GIO3 pin function selection (only reset by POR)

0000: No function, input

0001: SDO, 4-wire SPI data, output

0010: DTXD, direct mode TXD, output

0011: TXD, direct mode TXD, input

0100: TBCLK, TX bit clock, output

0101: IRQ, interrupt request, output

0110: ROSCi, ATX clock external input, input

0111: TXD, data monitor, output, only supported in direct mode

1000: ATXCLK, output

1001: LIRC clock, output

1010: FSYCK, i.e. 1/1, 1/2, 1/4, 1/8 XCLK, output

1011: LIRCCLK, internal LIRC clock with debounce, output

1100: EPA_EN, external PA enable, output

1101: ATXCCNTF, WOT flag, output

1110: TBCLK, TX bit clock, output

1111: PDB, Power down bar and XO enable, output

• **IO3: I/O Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	SDO_TEN	SPIPU	—	—	GIOPU[3:1]			—
R/W	R/W	R/W	—	—	R/W			—
POR	0	1	1	1	1	1	1	1

Bit 7 **SDO_TEN**: SDO tri-state enable (only reset by POR)

0: Disable

1: Enable

Bit 6 **SPIPU**: 3-wire SPI pull-up enable (only reset by POR)

0: Disable

1: Enable

When this bit is set high, it enables the pull-up for the CSN, SCK and SDIO pins only. If 4-wire SPI is used, note that the pull-up for the SDO pin must be configured separately using GIOPU[3:1].

Bit 5~4 Reserved, must be “11”

Bit 3~1 **GIOPU[3:1]**: GIO pin function pull-up enable control (only reset by POR)

These bits control the pull-up function of the GIO3~GIO1 pins respectively.

Bit 0 Reserved, must be “1”

• **FIFO1: FIFO Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	—	—	TXFFSA[5:0]					
R/W	—	—	R/W					
Reset	0	0	0	0	0	0	0	0

Bit 7~6 Reserved, must be “00”

Bit 5~0 **TXFFSA[5:0]**: TX FIFO start address, used for Block FIFO mode

• **FIFO2: FIFO Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	FFINF_EN	FFMG_EN	FFMG[1:0]	
R/W	—	—	—	—	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	1

Bit 7~4 Reserved, must be “0000”

Bit 3 **FFINF_EN**: FIFO infinite length mode enable

0: Disable

1: Enable

Bit 2 **FFMG_EN**: FIFO length margin detect enable

0: Disable

1: Enable

Bit 1~0 **FFMG[1:0]**: FIFO length margin selection

Threshold of remaining data in TX FIFO:

00: 4 bytes

01: 8 bytes

10: 16 bytes

11: 32 bytes

After the FIFO length margin detect function has been enabled by setting the FFMG_EN bit high and the required FIFO length margin has been selected by setting these bits, when the configured condition occurs the FIFOLTIF flag will be set high. In this case, an IRQ active signal will also be generated if the corresponding IRQ function has been enabled.

• **PKT1: Packet Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	TXPMLEN[7:0]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	1

Bit 7~0 **TXPMLEN[7:0]**: TX preamble length setting value low byte
Preamble length(in words) = {TXPMLENHB[7:0], TXPMLEN[7:0]}+1
When PMLP_EN and PMLPLEN bits are both set to 1, the word length is 2 bytes;
otherwise, the word length is 1 byte. TXPMLENHB[7:0] is located in the PKT19 register.

• **PKT2: Packet Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	PID[1:0]		TRAILER_EN	WHTFMT[0]	SYNCLLEN[1:0]		CRC_RANGE	PREAMB_EN
R/W	R/W		R/W	R/W	R/W		R/W	R/W
Reset	0	0	1	0	0	1	0	1

Bit 7~6 **PID[1:0]**: TX Packet ID

Bit 5 **TRAILER_EN**: Trailer field enable
0: Disable
1: Enable

Bit 4 **WHTFMT[0]**: Whitening format selection bit 0
The data whitening polynomial is selected by WHTFMT[2:0] bits (WHTFMT[2:1] is located in the PKT10 register).
WHTFMT[2:0]=
000: $G(X)=X^7+X^6+X^5+X^4+1$
001: PN7, $G(X)=X^7+X^4+1$
010: PN9-CCITT, $G(X)=X^9+X^5+1$
011: PN9-IBM, $G(X)=X^9+X^5+1$
101: LFSR PN7, $G(X)=X^7+X^4+1$
111: LFSR PN9-IBM2, $G(X)=X^9+X^5+1$
Other values: Reserved

Bit 3~2 **SYNCLLEN[1:0]**: SYNCWORD length setting bit 1~0
Final SYNCWORD length (in bytes) = {SYNCLLEN[1:0], SYNCLLENLB}+1;
SYNCLLENLB is located in the PKT10 register.

Bit 1 **CRC_RANGE**: CRC range selection
0: CRC covers the entire payload
1: CRC covers only the DATA field

Bit 0 **PREAMB_EN**: Preamble field enable
0: Disable
1: Enable

• **PKT3: Packet Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	MCH_EN	FEC_TYPE[1:0]		SYNC_MCH_EN	PLLEN_EN	PLHAC_EN	PLHLEN	PLH_EN
R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	0	0	0	0	0

Bit 7 **MCH_EN**: Manchester encoding enable
0: Disable
1: Enable

- Bit 6~5 **FEC_TYPE[1:0]**: FEC enable control and type selection
 00: FEC disabled
 01: Hamming(7,4)
 10: X^3+X+1
 11: X^3+X^2+1
- Bit **SYNC_MCH_EN**: SYNCWORD Manchester encoding control
 0: SYNCWORD without Manchester encoder
 1: SYNCWORD with Manchester encoder
- Bit 3 **PLEN_EN**: Payload length field enable
 0: Disable
 1: Enable
- Bit 2 **PLHAC_EN**: Payload header address correction enable
 0: Disable
 1: Enable
- Note: The packet handler always inserts the PLHA[5:0] field into the PLH field regardless of this bit setting. Address correction is performed by the receiving device based on the value of this field; the transmitter itself does not perform address checking.
- Bit 1 **PLHLEN**: Payload header length
 0: 1 byte
 1: 2 bytes
- Bit 0 **PLH_EN**: Payload header field enable
 0: Disable
 1: Enable

• **PKT4: Packet Control Register 4**

Bit	7	6	5	4	3	2	1	0
Name	WHT_EN	WHTSD[6:0]						
R/W	R/W	R/W						
Reset	0	0	1	1	0	1	1	0

- Bit 7 **WHT_EN**: Data whitening enable
 0: Disable
 1: Enable
- Bit 6~0 **WHTSD[6:0]**: Data whitening seed bit 6~0 (low 7 bits of the 9-bit seed)
 The higher two bits (WHTSD[8:7]) are located in the PKT15 register. Note: The WHTSD[8:7] bits are used only with 9-bit polynomials (i.e., PN9-CCITT, PN9-IBM, and LFSR PN9-IBM2).

• **PKT5: Packet Control Register 5**

Bit	7	6	5	4	3	2	1	0
Name	TXDLEN[7:0]							
R/W	R/W							
Reset	0	1	0	0	0	0	0	0

- Bit 7~0 **TXDLEN[7:0]**: TX data length (used in burst mode only)
 The transmitting data length in bytes is controlled by TXDLEN[7:0] bits.

• **PKT8: Packet Control Register 8**

Bit	7	6	5	4	3	2	1	0
Name	FEC_NIBBLE	PL_MLB	PLHA[5:0]					
R/W	R/W	R/W	R/W					
Reset	0	0	0	0	0	0	0	0

- Bit 7 **FEC_NIBBLE**: Nibble order for FEC encoding
0: Low nibble (bit 3~0) enters FEC encoder first
1: High nibble (bit 7~4) enters FEC encoder first
- Bit 6 **PL_MLB**: Payload data bit order
0: MSB first
1: LSB first
- Bit 5~0 **PLHA[5:0]**: Payload header address

• **PKT9: Packet Control Register 9**

Bit	7	6	5	4	3	2	1	0
Name	PLHEA[7:0]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

- Bit 7~0 **PLHEA[7:0]**: Payload header extended address

• **MOD1: Modulator Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	DTR[7:0]							
R/W	R/W							
Reset	0	0	0	0	0	1	1	1

- Bit 7~0 **DTR[7:0]**: Data rate divider (DTR) bits [7:0]
The 12-bit DTR value is stored in DTR[11:0] (DTR[11:8] is located in the MOD2 register).

• **MOD2: Modulator Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	DTR1[3:0]				DTR[11:8]			
R/W	R/W				R/W			
Reset	0	0	0	0	0	0	0	0

- Bit 7~4 **DTR1[3:0]**: Data rate divider1 (DTR1)
- Bit 3~0 **DTR[11:8]**: Data rate divider (DTR) bits [11:8]
The 12-bit DTR value is stored in DTR[11:0] (DTR[7:0] is located in the MOD1 register).

$$\text{Data Rate} = \text{NUM_CLK_N} / [8 \times (\text{DTR} + 1) \times (\text{DTR1} + 1)]$$

Here, NUM_CLK_N is used for the M/N algorithm. Its value is configured via registers RC3~RC5 and must not exceed the numeric value of XCLK (i.e., 16,000,000).

In low data rate mode (IIRX8CLK_EN must be set to 0, without pre-filter), it supports data rates from 0.5kbps to 100kbps in 0.1kbps steps.

In high data rate mode (IIRX8CLK_EN must be set to 1, with pre-filter), it supports fixed data rates of 125kbps or 250kbps.

Example: Desired Data Rate=97.1kbps, with DTR1=0.

Find NUM_CLK_N such that $\text{NUM_CLK_N} / [8 \times 97.1k \times (\text{DTR} + 1) \times (\text{DTR1} + 1)]$ is an integer, with $\text{NUM_CLK_N} \leq 16,000,000$.

If DTR=0, then NUM_CLK_N=776,800
 If DTR=1, then NUM_CLK_N=1,553,600
 If DTR=2, then NUM_CLK_N=2,330,400
 If DTR=3, then NUM_CLK_N=3,107,200
 If DTR=20, then NUM_CLK_N=16,312,800 (>16,000,000, cannot be used)

• **PKT20: Packet Control Register 20**

Bit	7	6	5	4	3	2	1	0
Name	—	—	LEN_NID_SWP	NODE_IDEN	NODE_IDLEN[1:0]		DITHER[1:0]	
R/W	—	—	R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	0	0	0

Bit 7~6 Reserved, must be “00”
 Bit 5 **LEN_NID_SWP**: Swap Length and Node ID fields order in the packet
 0: Node ID first, then Length
 1: Length first, then Node ID
 Bit 4 **NODE_IDEN**: Node ID field enable
 0: Disable
 1: Enable
 Bit 3~2 **NODE_IDLEN[1:0]**: Node ID length
 00: 1 byte
 01: 2 bytes
 10: 3 bytes
 11: 4 bytes
 Bit 1~0 **DITHER[1:0]**: Dither value

• **PKT21: Packet Control Register 21**

Bit	7	6	5	4	3	2	1	0
Name	CRC_POLYNOMIAL[7:0]							
R/W	R/W							
Reset	0	0	1	0	0	0	0	1

Bit 7~0 **CRC_POLYNOMIAL[7:0]**: CRC polynomial low byte

• **PKT22: Packet Control Register 22**

Bit	7	6	5	4	3	2	1	0
Name	CRC_POLYNOMIAL[15:8]							
R/W	R/W							
Reset	0	0	0	1	1	0	0	0

Bit 7~0 **CRC_POLYNOMIAL[15:8]**: CRC polynomial high byte
 The 16-bit CRC polynomial is stored in CRC_POLYNOMIAL[15:0] across PKT22 and PKT21 registers.
 0x0000: Bypass CRC field (CRC disabled)
 0x1021: CCITT-16 ($X^{16}+X^{12}+X^5+1$)
 0x8005: IBM-16 ($X^{16}+X^{15}+X^2+1$)
 Default after reset: $X^{12}+X^{11}+X^5+1$

• **PKT23: Packet Control Register 23**

Bit	7	6	5	4	3	2	1	0
Name	NODE_ID_BYTE[31:24]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **NODE_ID_BYTE[31:24]**: Node ID Byte3

• **PKT24: Packet Control Register 24**

Bit	7	6	5	4	3	2	1	0
Name	NODE_ID_BYTE[23:16]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	1

Bit 7~0 **NODE_ID_BYTE[23:16]**: Node ID Byte2

• **PKT25: Packet Control Register 25**

Bit	7	6	5	4	3	2	1	0
Name	NODE_ID_BYTE[15:8]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **NODE_ID_BYTE[15:8]**: Node ID Byte1

• **PKT26: Packet Control Register 26**

Bit	7	6	5	4	3	2	1	0
Name	NODE_ID_BYTE[7:0]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **NODE_ID_BYTE[7:0]**: Node ID Byte0

The maximum 4-byte Node ID is stored in PKT26~PKT23 registers. The Node ID length can be 1, 2, 3, or 4 bytes, selected by NODE_IDLEN[1:0] bits.

Bank 0 Control Registers

All control registers will be set to their initial value by power-on reset (POR). The software reset will set the control registers to their initial value except the RC3, RC4 and RC5 registers which are kept unchanged after software reset.

Addr.	Name	Bit							
		7	6	5	4	3	2	1	0
20h	RC3	NUM_CLK_N[7:0]							
21h	RC4	NUM_CLK_N[15:8]							
22h	RC5	NUM_CLK_N[23:16]							
26h	STA1	—	—	—	—	—	OMST[2:0]		
2Bh	ATX1	ATXCLK_DIV[1:0]		ATXCLKS	—	ATXCTM	ATXM[1:0]		ATX_EN
2Ch	ATX2	ATXCYC[7:0]							
2Dh	ATX3	ATXCYC[15:8]							
2Eh	ATX4	ATXCYC[23:16]							
31h	ATX7	—	—	—	—	—	ATX_WDLY[1:0]		ATXCYCM
33h	ATX9	ATXCT[7:0]							
34h	ATX10	ATXCT[15:8]							
35h	ATX11	ATXCT[23:16]							

Addr.	Name	Bit							
		7	6	5	4	3	2	1	0
36h	PKT10	WHTFMT[2:1]		CRCBYTE0	CRCBIT0	CRCINV	SYNCLENLB	PMLPLEN	PMLP_EN
37h	PKT11	PMLPAT[7:0]							
38h	PKT12	PMLPAT[15:8]							
39h	PKT13	CRCSD[7:0]							
3Ah	PKT14	CRCSD[15:8]							
3Bh	PKT15	WHTSD[8:7]		OOKDT_TS[3:0]				OOKDT_POR	OOKDT_EN
3Ch	PKT16	TXPRI[7:0]							
3Dh	PKT17	TXPRT[7:0]							
3Eh	PKT18							MCHFMT	TXPRM
3Fh	PKT19	TXPMLENHB[7:0]							

Note: The addresses which are not listed in this table are reserved for future use; it is suggested not to change their initial values by any means.

The “Reset” value shown in the following register description tables are the results after a software reset (Strobe command).

• **RC3: Reset/Clock Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	NUM_CLK_N[7:0]							
R/W	R/W							
POR	0	0	0	0	0	0	0	0

Bit 7~0 **NUM_CLK_N[7:0]**: Numerator value lowest byte (only reset by POR)

• **RC4: Reset/Clock Control Register 4**

Bit	7	6	5	4	3	2	1	0
Name	NUM_CLK_N[15:8]							
R/W	R/W							
POR	0	0	1	0	0	1	0	0

Bit 7~0 **NUM_CLK_N[15:8]**: Numerator value medium byte (only reset by POR)

• **RC5: Reset/Clock Control Register 5**

Bit	7	6	5	4	3	2	1	0
Name	NUM_CLK_N[23:16]							
R/W	R/W							
POR	1	1	1	1	0	1	0	0

Bit 7~0 **NUM_CLK_N[23:16]**: Numerator value highest byte (only reset by POR)

The 24-bit numerator value for M/N algorithm is stored in NUM_CLK_N[23:0] across registers RC5, RC4 and RC3. It is used to fine-tune the CLK_NM frequency(f_{CLK_NM}):

$$f_{CLK_NM} = (\text{decimal value of NUM_CLK_N}[23:0]) / f_{XCLK}$$

where $f_{XCLK} = f_{XTAL} = 16\text{MHz}$.

Note: The value of NUM_CLK_N[23:0] must not exceed the numeric value of f_{XCLK} (i.e., 16,000,000).

• **STA1: Status Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	OMST[2:0]		
R/W	—	—	—	—	—	R		
Reset	0	0	0	0	0	0	0	0

Bit 7~3 Reserved, must be “00000”

Bit 2~0 **OMST[2:0]**: Operation mode state indication (read only)

000: Deep Sleep mode

001: Idle mode

010: Light Sleep mode

011: Standby mode

100: TX mode

110: VCO calibration mode

101/111: Undefined

• **ATX1: Auto TX Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	ATXCLK_DIV[1:0]		ATXCLKS	—	ATXCTM	ATXM[1:0]		ATX_EN
R/W	R/W		R/W	—	R/W	R/W		R/W
Reset	1	1	0	0	1	0	0	0

Bit 7~6 **ATXCLK_DIV[1:0]**: ATX clock frequency division selection

00: 1/1, ATXCLK=32768Hz

01: 1/4, ATXCLK=8192Hz

10: 1/8, ATXCLK=4096Hz

11: 1/16, ATXCLK=2048Hz

Bit 5 **ATXCLKS**: ATXCLK clock source selection

0: From the internal LIRC clock

1: From the external ROSCi clock input on the GIO pin

Bit 4 Reserved, must be “0”

Bit 3 **ATXCTM**: Auto TX timer mode selection

0: Single mode, restart ATXCT timer when every ATX occurs.

1: Continuous mode, start ATXCT timer upon receiving Idle command; stop ATXCT timer when ATX_EN=0 or ATXCTM=0 and exit the ATX active period.

Bit 2~1 **ATXM[1:0]**: Auto TX mode selection

00: ATX WOT mode

01: Reserved

10/11: ATX WTM mode

Bit 0 **ATX_EN**: Auto TX enable

0: Disable

1: Enable

Note that the ATX functions are activated by operation state transition from Deep Sleep/Light Sleep mode to Idle mode.

• **ATX2: Auto TX Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	ATXCYC[7:0]							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

Bit 7~0 **ATXCYC[7:0]**: ATXCT timer expire value lowest byte

• **ATX3: Auto TX Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	ATXCYC[15:8]							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

Bit 7~0 **ATXCYC[15:8]**: ATXCT timer expire value medium byte

• **ATX4: Auto TX Control Register 4**

Bit	7	6	5	4	3	2	1	0
Name	ATXCYC[23:16]							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

Bit 7~0 **ATXCYC[23:16]**: ATXCT timer expire value highest byte

The 24-bit ATXCT timer expire value is stored in ATXCYC[23:0] across registers ATX4, ATX3 and ATX2. It is used to configure the wake-up period, which depends on the ATXCYCM bit setting:

- ATXCYCM=0 – BC3601/BC3602 compatible
Wake-up period = (ATXCLK period × ATXCYC[23:0]) + LIRCCLK period, where ATXCYC[23:0]≠0. Default wake-up period is about 2 hours.
- ATXCYCM=1 – BC3603x series compatible
Wake-up period = ATXCLK period × (ATXCYC[23:0]+1), where ATXCYC[23:0]≠0. Default wake-up period is about 2 hours.
The maximum wake-up period can be calculated as 2²⁴ divided by the ATXCLK frequency. For a 32.768kHz LIRC clock with different division factors, the results are as follows:
With a division factor of 1: 2²⁴/(32.768kHz/1)=0.142 hours
With a division factor of 4: 2²⁴/(32.768kHz/4)=0.5689 hours
With a division factor of 8: 2²⁴/(32.768kHz/8)=1.1378 hours
With a division factor of 16: 2²⁴/(32.768kHz/16)=2.2756 hours

• **ATX7: Auto TX Control Register 7**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	ATX_WDLY[1:0]		ATXCYCM
R/W	—	—	—	—	—	R/W		R/W
Reset	0	0	0	0	0	0	1	0

Bit 7~3 Reserved, must be “00000”

Bit 2~1 **ATX_WDLY[1:0]**: ATX wake-up delay time

00: 500μs
01: 1ms
10: 2ms
11: 4ms

Bit 0 **ATXCYCM**: ATXCYC mode selection

Refer to the ATX2~ATX4 register descriptions for the usage of this bit.

• **ATX9: Auto TX Control Register 9**

Bit	7	6	5	4	3	2	1	0
Name	ATXCT[7:0]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **ATXCT[7:0]**: ATXCT timer counter value lowest byte

• **ATX10: Auto TX Control Register 10**

Bit	7	6	5	4	3	2	1	0
Name	ATXCT[15:8]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **ATXCT[15:8]**: ATXCT timer counter value medium byte

• **ATX11: Auto TX Control Register 11**

Bit	7	6	5	4	3	2	1	0
Name	ATXCT[23:16]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **ATXCT[23:16]**: ATXCT timer counter value highest byte

The 24-bit ATX cycle timer value is stored in ATXCT[23:0] across registers ATX11, ATX10 and ATX9.

- Reading ATXCT[23:0] will get the current count value. Due to the limitation of 8-bit SPI data length, reading the ATX9 register will take a snapshot of the whole 24-bit data into the read buffer. Users should read ATX9 through ATX11 continuously (without interruption) to get correct data.
- Writing to ATXCT[23:0] will update the count value. Write to ATX9 first, then ATX10, and finally ATX11. Writing to ATX11 triggers the update of the ATXCT value. This timer update mechanism is used to align the time slot for master and slave devices in a two-way RF system.

• **PKT10: Packet Control Register 10**

Bit	7	6	5	4	3	2	1	0
Name	WHTFMT[2:1]		CRCBYTE0	CRCBIT0	CRCINV	SYNCLLENLB	PMLPLEN	PMLP_EN
R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	0	0

Bit 7~6 **WHTFMT[2:1]**: Whitening format selection bits 2~1

The data whitening polynomial is selected by WHTFMT[2:0] bits (note: WHTFMT[0] is located in the PKT2 register).

WHTFMT[2:0]=

000: $G(X)=X^7+X^6+X^5+X^4+1$

001: PN7, $G(X)=X^7+X^4+1$

010: PN9-CCITT, $G(X)=X^9+X^5+1$

011: PN9-IBM, $G(X)=X^9+X^3+1$

101: LFSR PN7, $G(X)=X^7+X^4+1$

111: LFSR PN9-IBM2, $G(X)=X^9+X^5+1$

Other values: Reserved

Bit 5 **CRCBYTE0**: CRC byte order

0: CRC high byte first

1: CRC low byte first

Bit 4 **CRCBIT0**: CRC bit order

0: CRC high bit first

1: CRC low bit first

Bit 3 **CRCINV**: CRC bit inverse function control

0: Non-inverse

1: Inverse

- Bit 2 **SYNCLLENLB**: SYNCWORD length setting lowest bit
Final SYNCWORD length (in bytes) = {SYNCLLEN[1:0], SYNCLLENLB}+1;
SYNCLLEN[1:0] is located in the PKT2 register.
- Bit 1 **PMLPLEN**: Preamble pattern length selection
0: 1-byte pattern – uses PMLPAT[7:0]
1: 2-byte pattern – uses PMLPAT[15:0], low byte transmitted first
- Bit 0 **PMLP_EN**: Preamble pattern selection
0: Preamble pattern is derived from “NOT(first bit of SYNCWORD) + 1/0 toggle”
Ex: SYNCWORD 1st bit=0, preamble = 01010101 (binary)
 SYNCWORD 1st bit=1, preamble = 10101010 (binary)
1: Preamble pattern is derived from PMLPAT[15:0]

• **PKT11: Packet Control Register 11**

Bit	7	6	5	4	3	2	1	0
Name	PMLPAT[7:0]							
R/W	R/W							
Reset	0	1	0	1	0	1	0	1

Bit 7~0 **PMLPAT[7:0]**: Preamble pattern low byte

• **PKT12: Packet Control Register 12**

Bit	7	6	5	4	3	2	1	0
Name	PMLPAT[15:8]							
R/W	R/W							
Reset	0	1	0	1	0	1	0	1

Bit 7~0 **PMLPAT[15:8]**: Preamble pattern high byte

• **PKT13: Packet Control Register 13**

Bit	7	6	5	4	3	2	1	0
Name	CRCSD[7:0]							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

Bit 7~0 **CRCSD[7:0]**: CRC seed low byte

• **PKT14: Packet Control Register 14**

Bit	7	6	5	4	3	2	1	0
Name	CRCSD[15:8]							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

Bit 7~0 **CRCSD[15:8]**: CRC seed high byte

• **PKT15: Packet Control Register 15**

Bit	7	6	5	4	3	2	1	0
Name	WHTSD[8:7]		OOKDT_TS[3:0]				OOKDT_POR	OOKDT_EN
R/W	R/W		R/W				R/W	R/W
Reset	0	0	0	1	0	1	0	1

Bits 5~0 of this register control the duty-cycle tuning function for OOK mode. It is recommended to refer to the “OOK Settings” chapter for the related configuration.

- Bit 7~6 **WHTSD[8:7]**: Data whitening seed bit 8~7 (high two bits of the 9-bit seed)
The lower 7 bits (WHTSD[6:0]) are located in the PKT4 register. Note: The WHTSD[8:7] bits are used only with 9-bit polynomials (i.e., PN9-CCITT, PN9-IBM, and LFSR PN9-IBM2).
- Bit 5~2 **OOKDT_TS[3:0]**: OOK duty cycle tuning time selection
0000: 2μs
0001: 4μs
0010: 6μs
0011: 8μs
... (step: 2μs)
1100: 26μs
1101: 28μs
1110: 30μs
1111: 32μs
- Bit 1 **OOKDT_POR**: OOK duty cycle tuning polarity
0: Extend 0 duty cycle
1: Extend 1 duty cycle
- Bit 0 **OOKDT_EN**: OOK duty cycle tuning enable
0: Disable
1: Enable

• **PKT16: Packet Control Register 16**

Bit	7	6	5	4	3	2	1	0
Name	TXPRI[7:0]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

- Bit 7~0 **TXPRI[7:0]**: TX packet repeat interval
Interval time (rest time between consecutive packets) = (TXPRI[7:0]+1) × t_{TCLK}

• **PKT17: Packet Control Register 17**

Bit	7	6	5	4	3	2	1	0
Name	TXPRT[7:0]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

- Bit 7~0 **TXPRT[7:0]**: TX packet repeat times
Repeat count = TXPRT[7:0]+1

• **PKT18: Packet Control Register 18**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	MCHFMT	TXPRM
R/W	—	—	—	—	—	—	R/W	R/W
Reset	0	0	0	0	0	0	0	0

- Bit 7~2 Reserved, must be “000000”
- Bit 1 **MCHFMT**: Manchester format
0: IEEE 802.3 Manchester code (0b→10b, 1b→01b)
1: G.E. Thomas Manchester code (0b→01b, 1b→10b)
- Bit 0 **TXPRM**: TX packet repeat mode
0: Send carrier during the rest period between repeated packets
1: Send preamble (toggled 0/1) during the rest period between repeated packets

• **PKT19: Packet Control Register 19**

Bit	7	6	5	4	3	2	1	0
Name	TXPMLENHB[7:0]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **TXPMLENHB[7:0]**: TX preamble length setting value high byte
Preamble length(in words) = {TXPMLENHB[7:0], TXPMLEN[7:0]}+1
When PMLP_EN and PMLPLEN bits are both set to 1, the word length is 2 bytes;
otherwise, the word length is 1 byte. TXPMLEN[7:0] is located in the PKT1 register.

Bank 1 Control Registers

All control registers will be set to their initial value by power-on reset (POR). The software reset will set the control registers to their initial value.

Addr.	Name	Bit								
		7	6	5	4	3	2	1	0	
2Ch	FCF1	IIRX8CLK_EN	—	SFRATIO[1:0]		GFD_COMP[3:0]				
2Dh	FCF2	FSCALE[7:0]								
2Eh	FCF3	GFLT_BPS	FD_INV	GFBT_SEL[1:0]		FSCALE[11:8]				
2Fh	FCF4	CF_B12[7:0]								
30h	FCF5	—						CF_B12[9:8]		
31h	FCF6	CF_B13[7:0]								
32h	FCF7	—						CF_B13[9:8]		
33h	FCF8	CF_A12[7:0]								
34h	FCF9	—						CF_A12[9:8]		
35h	FCF10	CF_A13[7:0]								
36h	FCF11	—						CF_A13[9:8]		
37h	FCF12	CF_B22[7:0]								
38h	FCF13	—						CF_B22[9:8]		
39h	FCF14	CF_B23[7:0]								
3Ah	FCF15	—						CF_B23[9:8]		
3Bh	FCF16	CF_A22[7:0]								
3Ch	FCF17	—						CF_A22[9:8]		
3Dh	FCF18	CF_A23[7:0]								
3Eh	FCF19	—						CF_A23[9:8]		

Note: The addresses which are not listed in this table are reserved for future use; it is suggested not to change their initial values by any means.

The “Reset” value shown in the following register description tables are the results after a software reset (Strobe command).

• **FCF1: Filter Coefficient Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	IIRX8CLK_EN	—	SFRATIO[1:0]		GFD_COMP[3:0]			
R/W	R/W	—	R/W		R/W			
Reset	1	0	0	0	0	1	1	0

Bit 7 **IIRX8CLK_EN**: IIR Pre-filter with 8×XCLK enable
0: Disabled. For data rates of 0.5kbps~100kbps
1: Enabled. For data rates of 125kbps or 250kbps

- Bit 6 Reserved, must be “0”
- Bit 5~4 **SFRATIO[1:0]**: Smooth filter ratio selection
 00: 1/1
 01: 1/16
 10: 1/64
 11: 1/128
- Bit 3~0 **GFD_COMP[3:0]**: Gaussian filter compensation for 101/010 pattern
 [3]: 1/8; [2]: 1/16; [1]: 1/32; [0]: 1/64
 For example:
 0000: no compensation

 1111: value after compensation = $[1+(1/8+1/16+1/32+1/64)]x = (1+0.234375)x$

• **FCF2: Filter Coefficient Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	FSCALE[7:0]							
R/W	R/W							
Reset	1	0	0	1	0	1	0	0

Bit 7~0 **FSCALE[7:0]**: Pre-filter scale low byte

• **FCF3: Filter Coefficient Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	GFLT_BPS	FD_INV	GFBT_SEL[1:0]	FSCALE[11:8]				
R/W	R/W	R/W	R/W	R/W				
Reset	0	1	0	1	0	0	1	0

- Bit 7 **GFLT_BPS**: Gaussian filter bypass
 0: TXD passes through Gaussian filter
 1: TXD bypasses Gaussian filter
 Note: For ACP (Adjacent Channel Power) testing, this bit must be set to 0.
- Bit 6 **FD_INV**: Deviation inverse control
 0: For TXD=0, FC+FD; for TXD=1, FC-FD
 1: For TXD=0, FC-FD; for TXD=1, FC+FD
 Note: FC= Center frequency of the RF channel; FD= Frequency deviation.
- Bit 5~4 **GFBT_SEL[1:0]**: Gaussian filter BT selection
 00: BT=0.3
 01: BT=0.5
 10: BT=0.8
 11: BT=1.0
- Bit 3~0 **FSCALE[11:8]**: Pre-filter scale high byte
 The 12-bit Pre-filter scale value is stored in FSCALE[11:0] (FSCALE[7:0] is located in the FCF2 register).
 • For data rates of 250k or 125k, the Pre-filter is required, and IIRX8CLK_EN must be set to 1. Pre-filter parameters depend on the loop filter shape and are generated by MATLAB.

$$FSCALE[11:0] = \text{round}((\text{Filter_scale} \times h \times f_s / f_{XTAL}) \times 2^{15})$$

 • For data rates in the range of 50k~100k, the Pre-filter and smooth filter are not used and IIRX8CLK_EN must be set to 0.
 • For data rates in the range of 0.5k~50k, the smooth filter is required, and IIRX8CLK_EN must be set to 0.

$$FSCALE[11:0] = \text{round}((h \times f_s / f_{XTAL}) \times 2^{15})$$

 where $h = (2 \times \text{frequency deviation}) / (\text{data rate})$.
 Here “h” is the modulation index, calculated from frequency deviation and data rate.

Note: Recommended settings for the Filter coefficient parameters are provided in the Modulation Architecture chapter.

• **FCF4: Filter Coefficient Control Register 4**

Bit	7	6	5	4	3	2	1	0
Name	CF_B12[7:0]							
R/W	R/W							
Reset	1	1	0	0	1	0	1	0

• **FCF5: Filter Coefficient Control Register 5**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_B12[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	1	0

IIR Coefficient CF_B12[9:0] is located in the FCF4 and FCF5 registers.

• **FCF6: Filter Coefficient Control Register 6**

Bit	7	6	5	4	3	2	1	0
Name	CF_B13[7:0]							
R/W	R/W							
Reset	0	1	1	0	0	0	1	0

• **FCF7: Filter Coefficient Control Register 7**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_B13[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	0	0

IIR Coefficient CF_B13[9:0] is located in the FCF6 and FCF7 registers.

• **FCF8: Filter Coefficient Control Register 8**

Bit	7	6	5	4	3	2	1	0
Name	CF_A12[7:0]							
R/W	R/W							
Reset	0	1	0	1	1	0	0	0

• **FCF9: Filter Coefficient Control Register 9**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_A12[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	1	1

IIR Coefficient CF_A12[9:0] is located in the FCF8 and FCF9 registers.

When the symbol rate is in the range of 50k~0.5k, the smooth filter is used, and CF_A12[9:0] is calculated as: $CF_A12[9:0] = \text{mod}(2^{10} + [(SFRATIO[1:0] - 1) \times 2^8], 2^{10})$

• **FCF10: Filter Coefficient Control Register 10**

Bit	7	6	5	4	3	2	1	0
Name	CF_A13[7:0]							
R/W	R/W							
Reset	1	1	1	0	1	0	0	1

• **FCF11: Filter Coefficient Control Register 11**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_A13[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	1	1

IIR Coefficient CF_A13[9:0] is located in the FCF10 and FCF11 registers.

• **FCF12: Filter Coefficient Control Register 12**

Bit	7	6	5	4	3	2	1	0
Name	CF_B22[7:0]							
R/W	R/W							
Reset	1	0	1	1	0	0	1	1

• **FCF13: Filter Coefficient Control Register 13**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_B22[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	1	1

IIR Coefficient CF_B22[9:0] is located in the FCF12 and FCF13 registers.

• **FCF14: Filter Coefficient Control Register 14**

Bit	7	6	5	4	3	2	1	0
Name	CF_B23[7:0]							
R/W	R/W							
Reset	0	0	1	1	1	1	1	0

• **FCF15: Filter Coefficient Control Register 15**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_B23[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	0	0

IIR Coefficient CF_B23[9:0] is located in the FCF14 and FCF15 registers.

• **FCF16: Filter Coefficient Control Register 16**

Bit	7	6	5	4	3	2	1	0
Name	CF_A22[7:0]							
R/W	R/W							
Reset	1	1	1	0	1	0	0	1

• **FCF17: Filter Coefficient Control Register 17**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_A22[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	1	1

IIR Coefficient CF_A22[9:0] is located in the FCF16 and FCF17 registers.

• **FCF18: Filter Coefficient Control Register 18**

Bit	7	6	5	4	3	2	1	0
Name	CF_A23[7:0]							
R/W	R/W							
Reset	0	0	1	1	1	0	0	1

• **FCF19: Filter Coefficient Control Register 19**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_A23[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	0	0

IIR Coefficient CF_A23[9:0] is located in the FCF18 and FCF19 registers.

The FCF4~FCF19 registers define eight groups of IIR coefficients, their recommended settings are listed below.

f_{XTAL}	16MHz	16MHz	16MHz	16MHz	16MHz
f_s (bps)	250k	125k	100k~10.1k	10k~2.1k	2k~0.5k
FD	93.75kHz	46.875kHz	18.75kHz	40kHz	8kHz
D_K[19:0]	FC×ODDIV/ f_{XTAL} (take decimal number)				
D_N[6:0]	FC×ODDIV/ f_{XTAL} (take integer number)				
IIRX8CLK_EN	1	1	0	0	0
SFRATIO[1:0](hex.)	0	0	0	1	3
FSCALE[11:0] (hex.)	294	119	4C	A4	20
CF_B12[9:0] (hex.)	2CA	01D	0	0	0
CF_B13[9:0] (hex.)	062	346	0	0	0
CF_A12[9:0] (hex.)	358	022	0	310	302
CF_A13[9:0] (hex.)	3E9	331	0	0	0
CF_B22[9:0] (hex.)	3B3	386	0	0	0
CF_B23[9:0] (hex.)	03E	012	0	0	0
CF_A22[9:0] (hex.)	3E9	008	0	0	0
CF_A23[9:0] (hex.)	039	008	0	0	0

FC: RF Central Frequency (Example:433.92MHz)

FD: Frequency deviation

Bank 2 Control Registers

The registers in Bank 2 that must be set after a POR or software reset are listed below. For registers or bit fields marked as Setting in the table, detailed descriptions are not provided in this document; please ensure they are configured according to the Recommended Settings Table provided below.

Addr.	Name	Bit							
		7	6	5	4	3	2	1	0
20h	OM	PWR_SOFT	BAND_SEL[1:0]	—	ACAL_EN	RTX_EN	RTX_SEL	SX_EN	
22h	SX1	—	D_N[6:0]						
23h	SX2	D_K[7:0]							
24h	SX3	D_K[15:8]							
25h	SX4	—			D_K[19:16]				
26h	CP1	Setting							
27h	CP2	Setting							
28h	CP3	Setting							
29h	OD1	Setting							
2Dh	VC3	Setting							
32h	TX2	—		CT_PAD [5:0]					
33h	TX3	Setting							
39h	LD1	Setting			CT_XOLDO [1:0]			Setting	
3Ah	LD2	Setting							
3Bh	LD3	Setting							
3Ch	XO1	XSHIFT[1:0]		—	XO_TRIM[4:0]				
3Dh	XO2	—			XO_SW	—			
3Eh	XO3	LIRCCAL_EN	LIRC_OW	LIRC_OP[4:0]					LIRC_EN

Must Set Registers in Bank 2

Note: 1. The registers listed in the following table must be set to the corresponding values. For detailed descriptions, please consult Holtek technical support.

Address	Name	Value	
		433MHz	868MHz
26h	CP1	03h	
27h	CP2	44h	
28h	CP3	50h	
29h	OD1	84h	80h
2Dh	VC3	14h	18h
33h	TX3	41h or 01h(OOK)*	
39h	LD1	9Ch	
3Ah	LD2	54h	
3Bh	LD3	5Ah	
3Ch	XO1	03h	

*: If using OOK mode, the TX3 register must be set to 01h.

Recommended Settings Table

- The addresses which are not listed in the Must-Set table are reserved for future use; it is suggested not to change their initial values by any means.
- The LIRC_OW, LIRC_OP[4:0], and LIRC_EN bits in the XO3 register are only reset by POR and kept unchanged after software reset.

The “Reset” value shown in the following register description tables are the results after a software reset (Strobe command).

• **OM: Operation Mode Control Register**

Bit	7	6	5	4	3	2	1	0
Name	PWR_SOFT	BAND_SEL[1:0]		—	ACAL_EN	TX_EN	TX_SEL	SX_EN
R/W	R/W	R/W		—	R/W	R/W	R/W	R/W
Reset	0	0	1	0	0	0	0	0

- Bit 7 **PWR_SOFT**: RF operation mode selection
0: RF normal operation mode
1: RF engineering mode
- Bit 6~5 **BAND_SEL[1:0]**: Band selection
00: 315MHz band, ODDIV=4
01: 433MHz band, ODDIV=2
10: 470~510MHz band, ODDIV=2
11: 868/915MHz band, ODDIV=1
- Bit 4 Reserved, must be “0”
- Bit 3 **ACAL_EN**: VCO and RC auto calibration enable
0: Disable
1: Enable
When this bit is set high, both the VCO and RC calibrations will be enabled. When the VCO and RC calibrations are completed, this bit will be cleared to zero by hardware.
- Bit 2 **TX_EN**: TX mode enable
0: Disable
1: Enable
Before setting this bit to 1 to enable TX mode, the TX mode must first be selected by setting TX_SEL=1.
- Bit 1 **TX_SEL**: TX mode selection
0: Reserved
1: TX mode
- Bit 0 **SX_EN**: Synthesizer enable (standby mode enable control)
0: Disable
1: Enable
Setting this bit high will enable the PFD, CP and VCO circuits.

• **SX1: Fractional-N Synthesizer Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	—	D_N[6:0]						
R/W	—	R/W						
Reset	0	0	1	1	0	1	1	0

- Bit 7 Reserved, must be “0”
- Bit 6~0 **D_N[6:0]**: Integer part of the RF channel frequency division ratio
The fractional part of the division ratio is a 20-bit value stored in D_K[19:0] across SX2~SX4 registers. $D_N[6:0] = \text{floor}(f_{RF} \times \text{ODDIV} / f_{XTAL})$
For example, with XO=16MHz and RF band =433.92MHz, and ODDIV=2:
→ $(433.92\text{MHz} \times 2) / 16\text{MHz} = 54.24$
→ D_N=54
→ Dec2Hex(54)=0x36
→ Dec2Bin(54)=011_0110

• **SX2: Fractional-N Synthesizer Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	D_K[7:0]							
R/W	R/W							
Reset	0	0	0	0	1	0	1	0

Bit 7~0 **D_K[7:0]**: Fractional part of RF channel frequency division ratio – lowest byte

• **SX3: Fractional-N Synthesizer Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	D_K[15:8]							
R/W	R/W							
Reset	1	1	0	1	0	1	1	1

Bit 7~0 **D_K[15:8]**: Fractional part of RF channel frequency division ratio – medium byte

• **SX4: Fractional-N Synthesizer Control Register 4**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	D_K[19:16]			
R/W	—	—	—	—	R/W			
Reset	0	0	0	0	0	0	1	1

Bit 7~4 Reserved, must be “0000”

Bit 3~0 **D_K[19:16]**: Fractional part of RF channel frequency division ratio – highest byte
The fractional part of the division ratio is a 20-bit value stored in D_K[19:0] across SX2~SX4 registers. The integer part is stored in D_N[6:0] in SX1 register.

$$D_K[19:0] = \text{floor}(((f_{RF} \times \text{ODDIV}) / f_{XTAL}) - D_N[6:0]) \times 2^{20}$$

For example, with XO=16MHz and RF band=433.92MHz, and ODDIV=2:

$$\rightarrow (433.92\text{MHz} \times 2) / 16\text{MHz} = 54.24$$

$$\rightarrow D_K = 0.24 \times 2^{20} = 251658$$

$$\rightarrow \text{Dec2Hex}(251658) = 0x3D70A$$

$$\rightarrow \text{Dec2Bin}(251658) = 0011_1101_0111_0000_1010$$

• **TX2: TX Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	—	—	CT_PAD[5:0]					
R/W	—	—	R/W					
Reset	0	0	1	1	0	0	0	0

Bit 7~6 Reserved, must be “00”

Bit 5~0 **CT_PAD[5:0]**: TX PAD linear power control

0x3A: 19dBm

0x37: 17dBm

0x2E: 13dBm

0x25: 10dBm

0x0E: 0dBm

0x00: -10dBm

Others: Reserved

• **LD1: LDO Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	Setting				CT_XOLDO[1:0]		Setting	
R/W	—	—	—	—	R/W		—	—
Reset	0	1	0	1	0	1	0	0

Bit 7~4 **Setting:** these bits must be set to “1001”

Bit 3~2 **CT_XOLDO[1:0]:** XO LDO setting

Note: CT_XOLDO[1:0] must be set to “11” before entering Light Sleep mode.

Bit 1~0 **Setting:** these bits must be set to “00”

The recommended set value for this register can refer to the table at the beginning of Bank 2 Control Registers section.

• **XO1: XO Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	XSHIFT[1:0]		—	XO_TRIM[4:0]				
R/W	R/W		—	R/W				
Reset	0	0	0	1	0	0	0	0

Bit 7~6 **XSHIFT[1:0]:** Coarse tune of the internal capacitor load for the crystal

Bit 5 Reserved, must be set to “0”

Bit 4~0 **XO_TRIM[4:0]:** Fine tune of the internal capacitor load for the crystal

The recommended set value for this register can refer to the table at the beginning of Bank 2 Control Registers section.

• **XO2: XO Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	XO_SW	—	—	—	—
R/W	—	—	—	R/W	—	—	—	—
Reset	0	0	0	0	0	0	1	1

Bit 7~5 Reserved, must be “000”

Bit 4 **XO_SW:** Crystal oscillator load capacitance switch

0: About 12~16pF

1: About 8~12pF

Bit 3~0 Reserved, must be “0011”

• **XO3: XO Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	LIRCCAL_EN	LIRC_OW	LIRC_OP[4:0]					LIRC_EN
R/W	R/W	R/W	R/W					R/W
POR	0	0	0	1	1	0	1	0
Reset	0	—	—	—	—	—	—	—

Bit 7 **LIRCCAL_EN:** LIRC calibration enable

0: Disable

1: Enable

Bit 6 **LIRC_OW:** LIRC overwrite control (only reset by POR)

0: LIRC_OP[4:0] from calibration engine

1: LIRC_OP[4:0] from control register

- Bit 5~1 **LIRC_OP[4:0]**: LIRC trim (only reset by POR)
 Writing to LIRC_OP[4:0] is effective only when LIRC_OW=1.
 The value read from LIRC_OP[4:0] depends on LIRC_OW: If LIRC_OW=0, returns the value from the calibration engine; If LIRC_OW=1, returns the value written by software.
- Bit 0 **LIRC_EN**: LIRC enable (only reset by POR)
 0: Disable
 1: Enable

Special Function Description

The BC2113 integrates a baseband modulator and a flexible packet handler with 64-byte TX FIFO, supporting FSK/GFSK data rates from 0.5kbps to 250kbps and OOK data rates from 0.5kbps to 20kbps. The packet handler enables flexible implementation of various packet formats with multiple encoding and processing functions, including CRC generation, Forward Error Correction (FEC), Data Whitening, and Manchester encoding.

The chip also integrates a Fractional-N synthesizer with fine frequency resolution, an on-chip loop filter, and programmable crystal load capacitors to minimize external component requirements. Communication with an external host MCU is accomplished through a 3-wire or 4-wire SPI interface, with support for short strobe commands to reduce host MCU overhead. In addition, features such as Wake-On-TX (WOT) and auto-repeat transmission facilitate efficient low-power duty-cycle operation.

SPI Interface

The BC2113 communicates with a host MCU via a 3-wire SPI interface (CSN, SCK, SDIO) or a 4-wire SPI interface (SDO from GION pin selectable) with a data rate up to 8Mbps. An SPI transmission is an $(8+8 \times n)$ -bit sequence which consists of an 8-bit command and n 8-bit data, where n can be 0 or any natural number. If the number n exceeds the address boundary, the address will return to zero. The host MCU should pull the CSN (SPI chip select) pin low in order to access the BC2113. Using the SPI interface, the host MCU can access the control registers and issue strobe commands. When writing data to the BC2113, the SPI data will be latched into the registers at the rising edge of the SCK signal. When reading data from the BC2113 registers, the bit data will be transferred at the falling edge of the SCK signal after the target register address has been input.

Command (8 bits)								Data (8 bits)							
C7	C6	C5	C4	C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0

SPI Command Format

SPI Command Definition

Two kinds of command are defined. One is 1-byte command only (named CmdO), and the other is 1-byte command followed by n -byte data (named CmdD).

The following table summarizes the strobe commands supported by the BC2113.

C7	C6	C5	C4	C3	C2	C1	C0	Description	CmdO	CmdD
0	1	A5	A4	A3	A2	A1	A0	Write to control registers		√
1	1	A5	A4	A3	A2	A1	A0	Read from control registers		√
0	0	1	x	x	x	B1	B0	Set register bank	√	
0	0	0	1	0	0	0	0	Write SYNCWORD command		√
1	0	0	1	0	0	0	0	Read SYNCWORD command		√
0	0	0	1	0	0	0	1	TX FIFO write command		√

C7	C6	C5	C4	C3	C2	C1	C0	Description	CmdO	CmdD
1	0	0	1	1	1	1	1	Read Chip ID command		√
0	0	0	0	1	0	0	0	Software reset command	√	
0	0	0	0	1	0	0	1	TX FIFO address pointer reset command	√	
0	0	0	0	1	0	1	0	Deep Sleep mode	√	
0	0	0	0	1	0	1	1	Idle mode	√	
0	0	0	0	1	1	0	0	Light Sleep mode	√	
0	0	0	0	1	1	0	1	Standby mode	√	
0	0	0	0	1	1	1	0	TX mode	√	

A5~A0: The address of control registers;

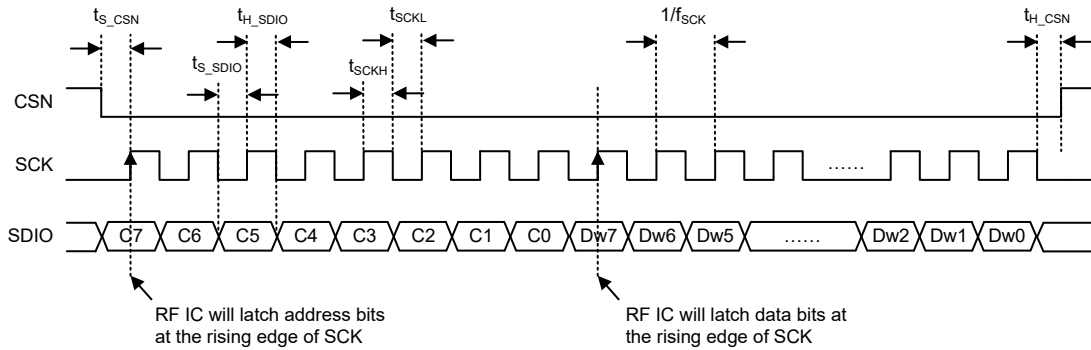
x: Hardware doesn't care but it is recommended to set to 0 by software;

B1~B0: The Bank number.

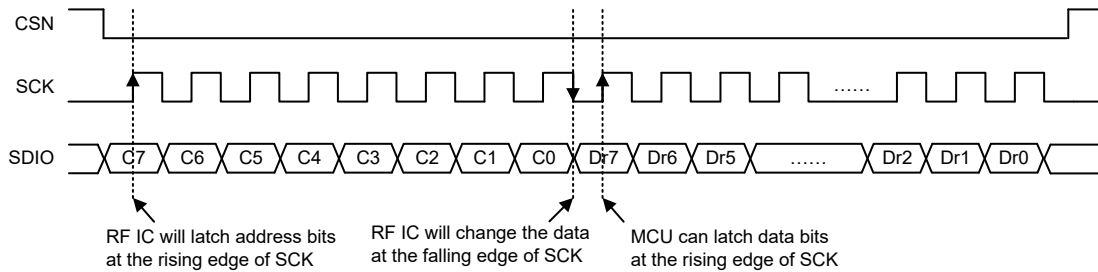
Note: 1. The chip supports multi-byte read/write operations, and the address is increased automatically after each read or write operation.

2. Multi-byte read/write is allowed with a single read/write command during one CSN enabled (CSN low) cycle.

SPI Timing



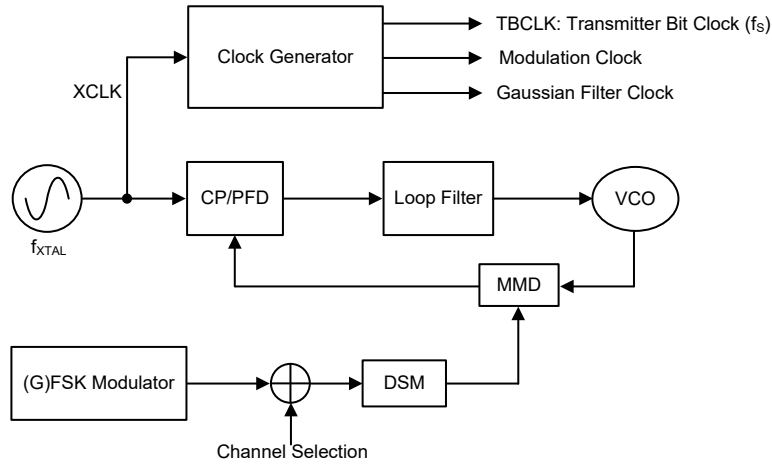
3-Wire SPI Interface Write 1-byte Data Operation



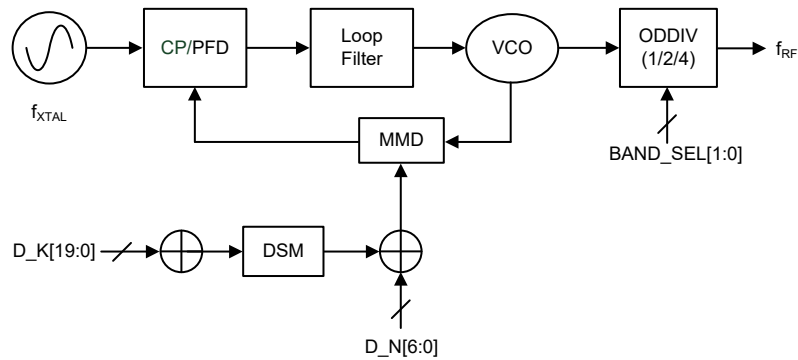
3-Wire SPI Interface Read 1-byte Data Operation

System Clock

The main system clock of the BC2113 comes from the crystal oscillator. All internal operation clocks of various functional blocks are derived from the crystal oscillator.



Frequency Synthesizer



The RF transmitter frequency is generated by a high resolution fractional-N Delta Sigma frequency synthesizer. By appropriate settings of the configuration parameters D_N[6:0] and D_K[19:0], a low-noise LO frequency can be generated to comply with various radio regulatory standards including ETSI EN, FCC, etc.

$$D_N[6:0] = \text{floor}\left(\frac{f_{RF} \times \text{ODDIV}}{f_{XTAL}}\right)$$

$$D_K[19:0] = \text{floor}\left(\left(\frac{f_{RF} \times \text{ODDIV}}{f_{XTAL}} - D_N[6:0]\right) \times 2^{20}\right)$$

Modulation Architecture

A summary of the modulation architecture is shown below.

IIRX8CLK_EN	1	0
TBCLK	$\frac{XCLK}{(DTR+1) \times 8 \times 8}$	$\frac{NUM_CLK_N}{(DTR+1) \times 8 \times (DTR+1)}$
Pre-Filter	Required	Not required
Smooth Filter	Fixed 8 cycles	1~8 cycles
High Data Rate (125kbps/250kbps)	CF_B12[9:0]/CF_B13[9:0]/ CF_B22[9:0]/CF_B23[9:0]/ CF_A12[9:0]/CF_A13[9:0]/ CF_A22[9:0]/CF_A23[9:0]	Not supported
	SFRATIO[1:0]=00	SFRATIO[1:0]=00
Low Data Rate (0.5kbps~100kbps, by 0.1kbps step)	- CF_B12[9:0]/CF_B13[9:0]/CF_B22[9:0]/CF_B23[9:0]/CF_A13[9:0]/ CF_A22[9:0]/CF_A23[9:0] all must be set to 0x000. - Set (SFRATIO[1:0], CF_A12[9:0]) = (0x0,0x000) or (0x1,0x310) or (0x2, 0x304) or (0x3,0x302) (choose 1 from 4)	

Remark: All settings listed above refer to the table below for detailed recommended values.

f _{X_{TAL}}	16MHz	16MHz	16MHz	16MHz	16MHz
f _s (bps)	250k	125k	100k~10.1k	10k~2.1k	2k~0.5k
FD (Customer Setting when data_rate ≤ 100kbps)	93.75kHz	46.875kHz	18.75kHz	40kHz	8kHz
D_K[19:0]	FC×ODDIV/f _{X_{TAL}} (take decimal number)				
D_N[6:0]	FC×ODDIV/f _{X_{TAL}} (take integer number)				
IIRX8CLK_EN	1	1	0	0	0
SFRATIO[1:0](hex.)	0	0	0	1	3
FSCALE[11:0] (hex.)	294	119	4C	A4	20
CF_B12[9:0] (hex.)	2CA	01D	0	0	0
CF_B13[9:0] (hex.)	062	346	0	0	0
CF_A12[9:0] (hex.)	358	022	0	310	302
CF_A13[9:0] (hex.)	3E9	331	0	0	0
CF_B22[9:0] (hex.)	3B3	386	0	0	0
CF_B23[9:0] (hex.)	03E	012	0	0	0
CF_A22[9:0] (hex.)	3E9	008	0	0	0
CF_A23[9:0] (hex.)	039	008	0	0	0

FC: RF Central Frequency (Example:433.92MHz)

FD: Frequency deviation

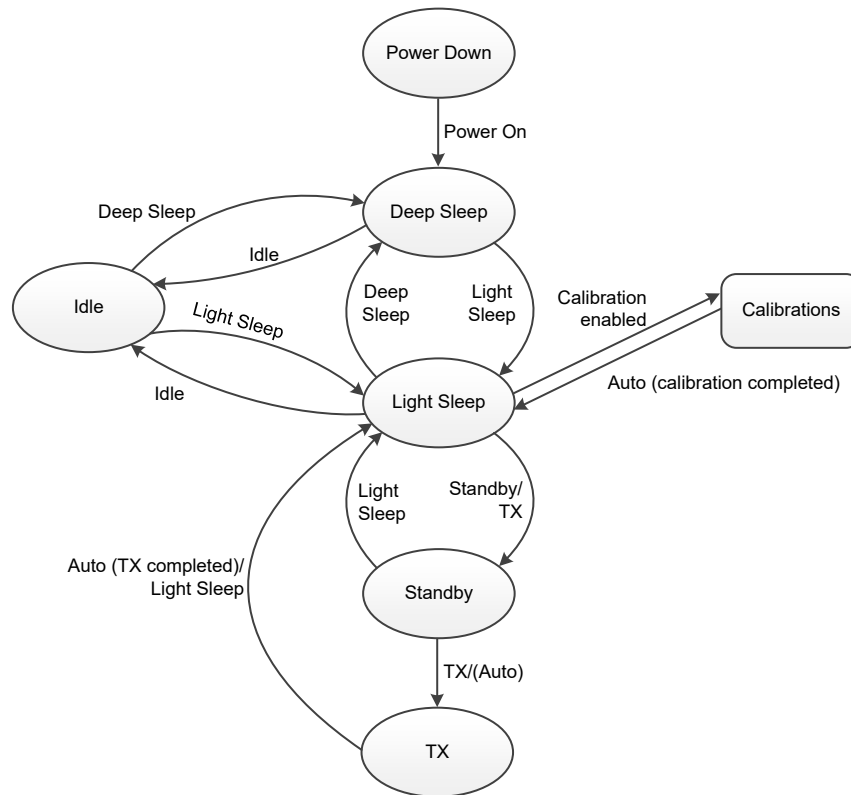
State Machine

There are six operating modes in the BC2113 from the viewpoint of current consumption. The operation modes and the on/off states of key functions in each mode are listed in the table below. The host MCU can control the chip to switch to different operating modes by sending a simple strobe command.

Mode	Register Retention	3.3V	LIRC	Regulator	XO	Standby +VCO	TX	Strobe Command
Power Down	No	OFF	OFF	OFF	OFF	OFF	OFF	—
Deep Sleep	Yes	ON	OFF	OFF	OFF	OFF	OFF	0000_1010
Light Sleep	Yes	ON	OFF	ON	ON	OFF	OFF	0000_1100
Idle	Yes	ON	ON	OFF	OFF	OFF	OFF	0000_1011
Standby	Yes	ON	OFF	ON	ON	ON	OFF	0000_1101
TX	Yes	ON	OFF	ON	ON	ON	ON	0000_1110

FIFO Mode (DIR_EN=0) State Machine

If the DIR_EN bit is cleared to 0, the BC2113 mode switching is implemented by a strobe command from the host MCU and the TX data are derived from the packet handling hardware.

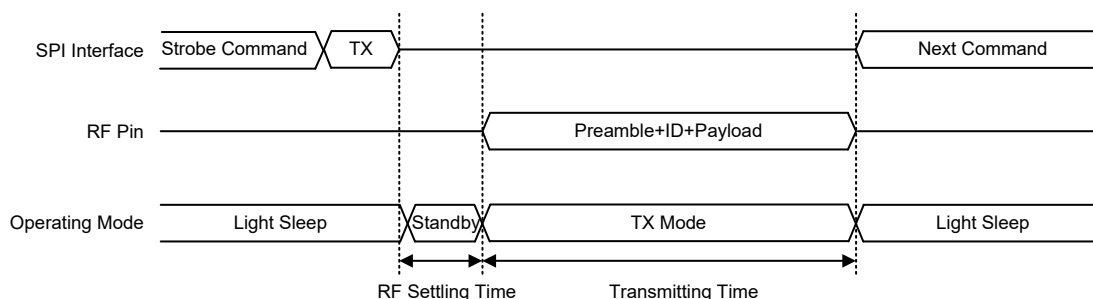


FIFO Mode State Diagram

After power-on and internal power-on reset, the BC2113 enters Deep Sleep mode and waits for further strobe commands from the host MCU. If a Light Sleep command is received, the BC2113 enables the internal LDO, starts the XO, and enters Light Sleep mode. In this state, the host MCU can have the BC2113 execute VCO/RC or LIRC calibrations if necessary. For normal TX operations, the host MCU can issue a TX command to the BC2113. After receiving the TX command, the BC2113 first enters Standby mode which lasts a certain period (TX settling time). After the settling

time has elapsed, the BC2113 will finally enter TX mode. It will stay in the TX mode until the TX completion event occurs, after which the chip will automatically return to Light Sleep mode.

For low power periodical wireless transmission, BC2113 supports a low-power Idle mode in which the LIRC and wake-up timer are turned on. By setting the timer appropriately and issuing the Idle mode command, BC2113 will turn off the LDO and XO and enter Idle mode. The wake-up timer starts counting after ATX_EN is set to 1. The chip stays in the Idle mode until the timer expires, and then an IRQ is asserted on the GIO pin to wake up the host MCU. The host MCU can then have BC2113 enter Light Sleep mode and continue to execute normal TX operations. After TX completion, the host MCU can issue the Idle command to have BC2113 return to the Idle mode.



Note: Calibration time: $\sim 152\mu\text{s}@433\text{MHz}$ / $\sim 96\mu\text{s}@868\text{MHz}$.

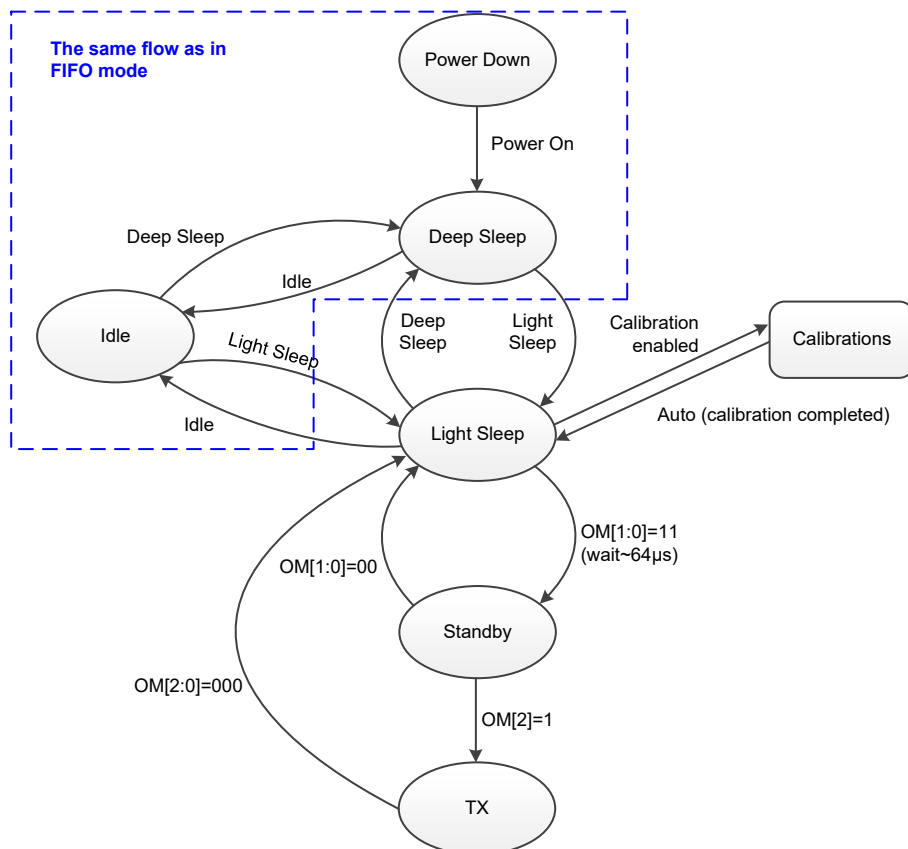
TX Timing in FIFO Mode

Direct Mode (DIR_EN=1) State Machine

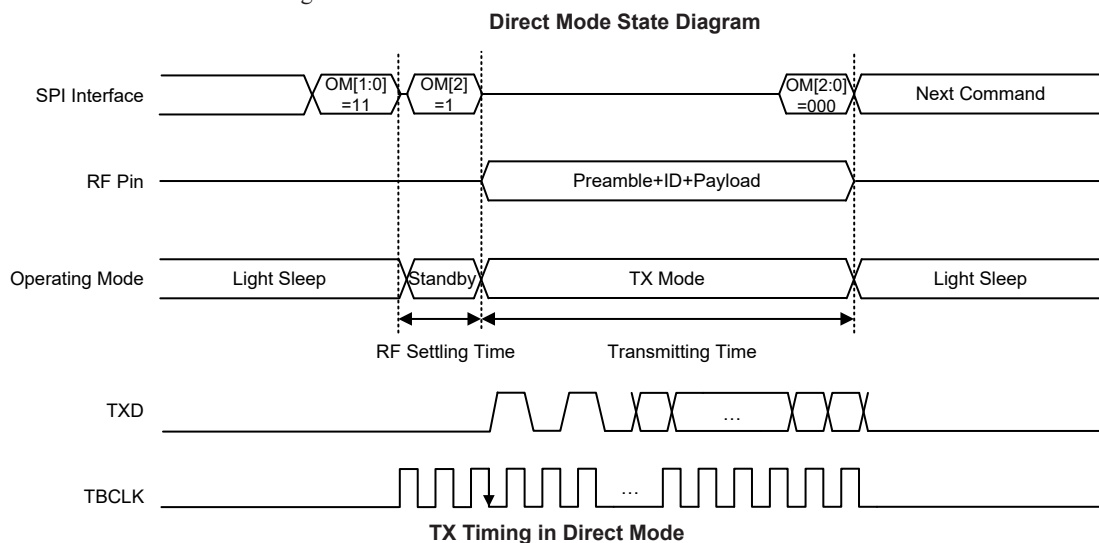
If the DIR_EN bit is set to 1, the BC2113 TX data is derived directly from the host MCU. To simplify the data bit clock synchronization between the BC2113 and the host MCU, the BC2113 outputs the TBCLK signal on a GIO pin (The TBCLK pin function must first be selected by setting the corresponding GIOs field). The TBCLK is in 50/50 duty cycle. In transmitting mode, the host MCU outputs bit data after the falling edge of TBCLK, and the BC2113 samples the TX bit data on the rising edge of TBCLK. The host MCU can assign BC2113 another GIO pin as the TXD (TX bit data) input pin by setting the corresponding GIOs field.

For TX operations in Direct Mode, the host MCU must first set bits 1~0 of the BC2113's OM register to 1 (i.e., set TX_SEL and SX_EN to 1) to select TX mode and have the BC2113 enter standby mode first. Then it sets bit 2 of the same register to 1 (i.e., set TX_EN to 1) to have the BC2113 start TX data transmission. When the host MCU sets bits 2~0 of the OM register to "000", the BC2113 will return to Light Sleep mode.

In Direct Mode, the transmission data length has no limit.



Note: In the diagram, OM[1:0], OM[2], and OM[2:0] denote the corresponding bits or bit fields of the OM register.



Calibration

There are three calibration functions, VCO, RC and LIRC calibrations, allowing users to select proper settings to compensate for PVT (Process-Voltage-Temperature) variations.

VCO and RC Calibration

The chip has a control bit, ACAL_EN, to enable the VCO and RC calibration functions at the same time. After the calibrations are completed, the ACAL_EN bit is cleared to zero by hardware. The host MCU can poll the ACAL_EN bit status or use the calibration complete interrupt flag CALCMPIF to check the calibration status.

LIRC Calibration

The chip contains an internal low frequency RC oscillator (32768Hz) that provides the clock source for the wake-up timer (ATXCT) in Idle mode. In order to compensate for the PVT (Process-Voltage-Temperature) variation error (up to $\pm 10\%$) that affects the LIRC accuracy, the host MCU can trigger LIRC calibration to improve the wake-up timer accuracy error to be less than $\pm 1\%$.

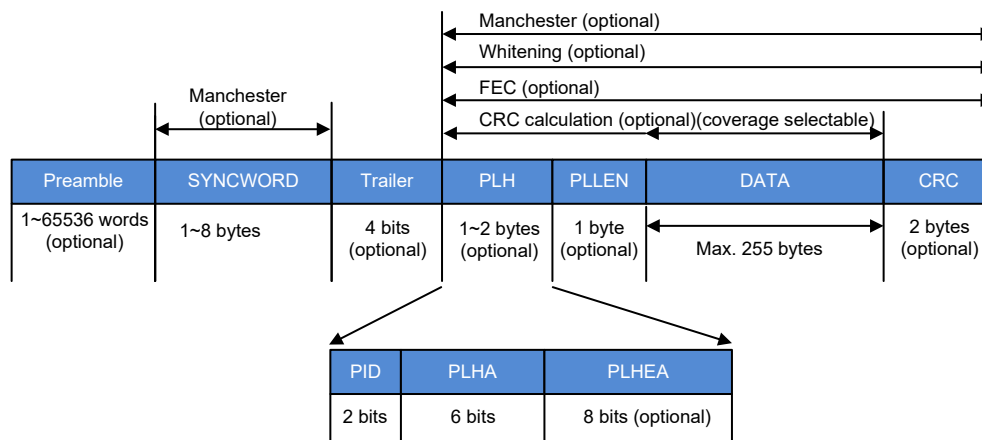
The host MCU needs to configure LIRC_OW=0 and LIRC_EN=1 before the LIRC calibration. Then, while the chip is in Light Sleep mode, the host MCU sets LIRCCAL_EN to 1 to start the LIRC calibration. The LIRCCAL_EN bit is reset to 0 by hardware on the completion of LIRC calibration. The LIRC calibration process would take about 4ms.

Packet Handler

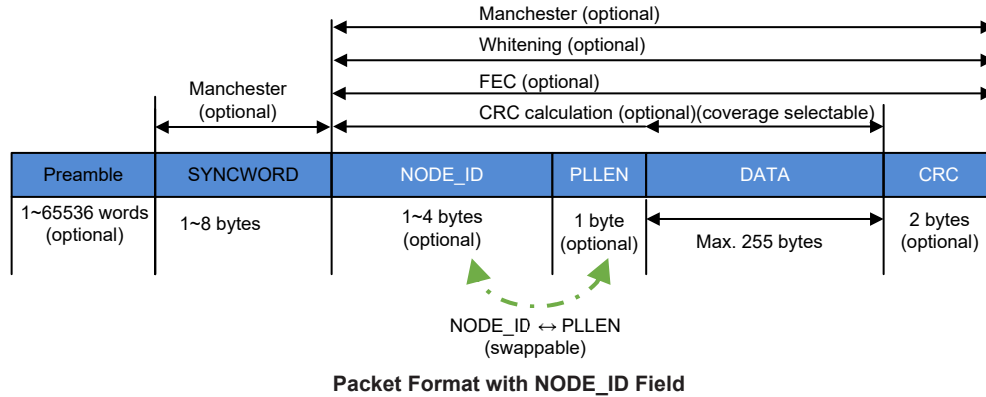
The packet handler is used to move the transmitting data out of FIFO and implement channel coding according to the packet format, then send the packet to the modulator. The packet handler performs several tasks such as Preamble and SYNCWORD insertion, Forward Error Correction, CRC calculation, whitening and Manchester encoding.

Packet Format

Two format examples are shown below for illustration: one with the PLH field, and the other with the NODE_ID field. For more detailed format setting suggestions, please refer to the Packet Format Setting Suggestions section.



Packet Format with PLH Field



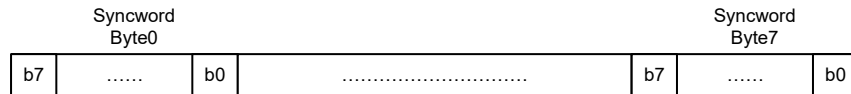
Preamble

The packet may optionally include a preamble field (controlled by PREAMB_EN). When enabled, the packet starts with a preamble with a length of 1~65536 words, set by {TXPMLENHB[7:0], TXPMLLEN[7:0]}+1. The word length is determined by the preamble mode. There are two preamble modes selected by PMLP_EN.

- PMLP_EN=0 – Auto preamble pattern mode (compatible with BC3601/02/03/02A/03A)
 The first bit of the preamble pattern equals the inverted value of the first transmitted bit of the SYNCWORD, and then the pattern toggles (1/0). In this mode, word length = 1 byte.
- PMLP_EN=1 – User-defined preamble pattern mode
 The preamble pattern is defined by PMLPAT[15:0]; the word length is defined by PMLPLEN.
 PMLPLEN=0, preamble pattern = PMLPAT[7:0]; word length = 1 byte
 PMLPLEN=1, preamble pattern = PMLPAT[15:0]; word length = 2 bytes

SYNCWORD

The SYNCWORD length is configurable from 1~8 bytes, set by {SYNCLLEN[1:0], SYNCLLENLB}+1.



Syncword Format

Note: The writing order is the same as the air Packet transmission order.

Example (4-byte Syncword): Byte0=0x12, Byte1=0x34, Byte2=0x56, Byte3=0x78.

Syncword writing order: Byte0 → Byte1 → Byte2 → Byte3

Air Packet transmission order: Byte0 → Byte1 → Byte2 → Byte3

The over-air bit sequence for this example is: 00010010 00110100 01010110 01111000

Trailer

The trailer field is optional and has a fixed length of 4 bits. It is enabled by TRAILER_EN bit.

PLH (Payload Header)

The PLH field is optional and enabled by PLH_EN bit. Its length can be 1 or 2 bytes set by PLHLEN. When PLHLEN=0, the PLH field={PID[1:0], PLHA[5:0]}; when PLHLEN=1, the PLH field={PID[1:0], PLHA[5:0], PLHEA[7:0]}. The function of PLHA[5:0] is controlled by PLHAC_EN. If PLHAC_EN=0, PLHA[5:0] can be used as user-defined software flags. This feature can be used to support broadcast function among devices that share the same SYNCWORD but have different PLH address bits.

PLLEN (Payload Length)

The PLLEN field is optional and enabled by PLLEN_EN. Its length is fixed to 1 byte. When enabled, the length of the DATA field is determined by the value carried in the PLLEN field. In TX mode, the transmitter sends the TXDLEN[7:0] defined bytes of data from TX FIFO and the TXDLEN[7:0] is automatically latched into the PLLEN field.

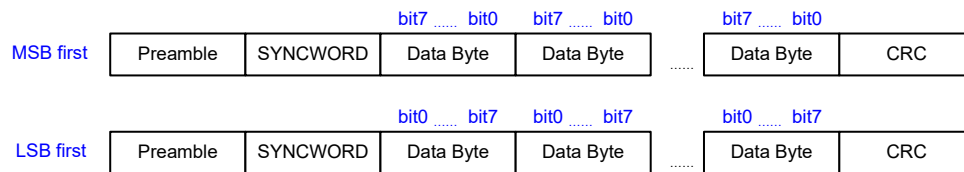
NODE_ID

The NODE_ID field is optional and enabled by NODE_IDEN. Its function is similar to the PLH field, and its length can be 1~4 bytes, set by NODE_IDLEN[1:0]. The order of the NODE_ID and PLLEN fields in the packet can be swapped, controlled by the LEN_NID_SWP bit. Regardless of which field comes first, the value of PLLEN always indicates the byte number of the DATA field. The NODE_ID value can be configured by registers.

NODE_ID_BYTE[7:0]	NODE_ID_BYTE[15:8]	NODE_ID_BYTE[23:16]	NODE_ID_BYTE[31:24]
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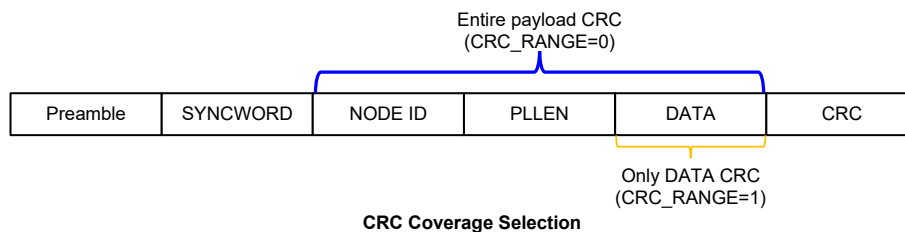
DATA

The DATA field length is determined by TXDLEN[7:0]. The maximum length is 255 bytes in the Extend FIFO Mode. In the special case of Infinite FIFO Mode, the length can exceed 255 bytes. The payload data bit order is configurable by the PL_MLB bit: the data bytes can be chosen to send with MSB (bit7) or LSB (bit0) first.



CRC

The CRC field is optional, but it is recommended to always enable the CRC function to ensure data integrity. The CRC polynomial is set by CRC_POLYNOMIAL[15:0]. When CRC_POLYNOMIAL[15:0] is set to all zeros, the CRC function is disabled in the Packet Format. The CRC_RANGE bit selects whether the CRC covers the entire payload or only the DATA field.



Two common CRC polynomials are supported by setting CRC_POLYNOMIAL[15:0] accordingly:

0x1021: CCITT-16-CRC ($G(X)=X^{16}+X^{12}+X^5+1$)

0x8005: IBM-16-CRC ($G(X)=X^{16}+X^{15}+X^2+1$)

FEC

The FEC data encode function is controlled by FEC_TYPE[1:0]. When these bits are set to 00, the FEC function is disabled. When set to non-zero values, FEC is enabled and different polynomials can be selected. For example, when set to 01, it uses Hamming(7,4) code, which corrects single-bit errors and detects multiple-bit errors for each 4-bit data. After FEC, each original byte becomes $(4+3) \times 2 = 14$ bits.

The following table shows the bit mapping for each 4-bit nibble (before encoding) and the parity bit (P2, P1, P0) calculation using Hamming(7,4) code. The nibble order for FEC encoding is selectable by the FEC_NIBBLE bit, i.e., whether the low nibble or the high nibble enters the FEC encoder first.

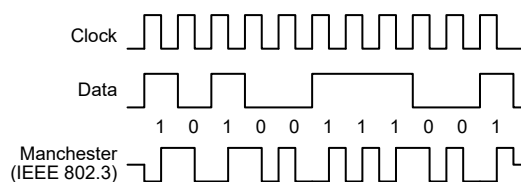
Bit	7	6	5	4	3	2	1
Transmitted Bit	D3	D2	D1	P2	D0	P1	P0
P0	Y	N	Y	N	Y	N	Y
P1	Y	Y	N	N	Y	Y	N
P2	Y	Y	Y	Y	N	N	N

Data Whitening

The data whitening function is optional and enabled by the WHT_EN. The whitening format is selected by WHTFMT[2:0], and the seed is set by WHTSD[8:0].

Manchester Code

The Manchester encoding function is optional. Manchester encoding for the payload is enabled by the MCH_EN bit, while that for the SYNCWORD is separately controlled by the SYNC_MCH_EN bit. The chip supports two Manchester encoding formats: IEEE 802.3 Manchester encoding (10=data 0, 01=data 1) and G.E. Thomas Manchester encoding(01=data 0, 10=data 1). The encoding format is selected by the MCHFMT bit. After Manchester encoding, each original data bit is expanded into two bits.



Manchester Code Example

Packet Format Setting Suggestions

The BC2113 provides flexible format settings. Several suggestions are listed below. Users may refer to these and select the suitable format for their application.

- Note: 1. When CRC_POLYNOMIAL[15:0] is set to 16'b0, the CRC field is not present in the packet.
 2. If NODE_IDEN=1 (NODE_ID field enabled), then the Header and Trailer fields will not be present in the packet, regardless of whether they are enabled.
 3. "x" means "don't care"(the bit value does not affect the function in that configuration).
 4. In the format setting examples, the PREAMB_EN bit is always 1, so the Preamble field is always present in the packet.

Setting 1

PLEN_EN	PLHLEN	PLH_EN	TRAILER_EN	NODE_IDEN	NODE_IDLEN[1:0]	LEN_NID_SWP	CRC_POLYNOMIAL[15:0]
0	x	0	0	0	x	x	Non-zero

Then the fields in a packet are as follows:

Preamble	SYNCWORD	DATA	CRC
----------	----------	------	-----

Setting 2

PLLEN_EN	PLHLEN	PLH_EN	TRAILER_EN	NODE_IDEN	NODE_IDLEN[1:0]	LEN_NID_SWP	CRC_POLYNOMIAL[15:0]
1	x	0	0	0	x	x	Non-zero

Then the fields in a packet are as follows:

Preamble	SYNCWORD	PLEN	DATA	CRC
----------	----------	------	------	-----

Setting 3

PLLEN_EN	PLHLEN	PLH_EN	TRAILER_EN	NODE_IDEN	NODE_IDLEN[1:0]	LEN_NID_SWP	CRC_POLYNOMIAL[15:0]
0	x	x	x	1	1~4	x	Non-zero

Then the fields in a packet are as follows:

Preamble	SYNCWORD	NODE_ID	DATA	CRC
----------	----------	---------	------	-----

Setting 4

PLLEN_EN	PLHLEN	PLH_EN	TRAILER_EN	NODE_IDEN	NODE_IDLEN[1:0]	LEN_NID_SWP	CRC_POLYNOMIAL[15:0]
1	x	x	x	1	1~4	0	Non-zero

Then the fields in a packet are as follows:

Preamble	SYNCWORD	NODE_ID	PLEN	DATA	CRC
----------	----------	---------	------	------	-----

Setting 5

PLLEN_EN	PLHLEN	PLH_EN	TRAILER_EN	NODE_IDEN	NODE_IDLEN[1:0]	LEN_NID_SWP	CRC_POLYNOMIAL[15:0]
1	x	x	x	1	1~4	1	Non-zero

Then the fields in a packet are as follows:

Preamble	SYNCWORD	PLEN	NODE_ID	DATA	CRC
----------	----------	------	---------	------	-----

Setting 6

PLLEN_EN	PLHLEN	PLH_EN	TRAILER_EN	NODE_IDEN	NODE_IDLEN[1:0]	LEN_NID_SWP	CRC_POLYNOMIAL[15:0]
1	1	1	0	0	x	x	Non-zero

Then the fields in a packet are as follows:

Preamble	SYNCWORD	PLH	PLEN	DATA	CRC
----------	----------	-----	------	------	-----

Setting 7

PLLEN_EN	PLHLEN	PLH_EN	TRAILER_EN	NODE_IDEN	NODE_IDLEN[1:0]	LEN_NID_SWP	CRC_POLYNOMIAL[15:0]
1	x	0	1	0	x	x	Non-zero

Then the fields in a packet are as follows:

Preamble	SYNCWORD	Trailer	PLEN	DATA	CRC
----------	----------	---------	------	------	-----

FIFO Operation Modes

In Burst mode, data transmission to the RF transmitter is derived from FIFO that is pre-written by the host MCU. There are 4 FIFO modes to support various applications: Simple FIFO mode, Block FIFO mode, Extend FIFO mode, and Infinite FIFO mode.

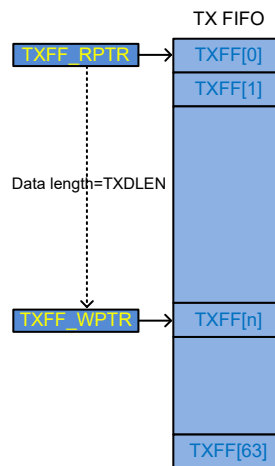
FIFO Reset

To use the FIFO in the burst mode, issue the TX FIFO address pointer reset command to reset the FIFO pointer and buffer. After that, the FIFO is in the same state as after reset.

Programming procedure:

This procedure is for general applications where the TX data length ≤ 64 bytes.

1. Reset TX FIFO address pointer by the SPI reset TX FIFO command.
2. TXFFSA[5:0] must be cleared to 0.
3. Fill out TX FIFO by the SPI TX FIFO write command.
4. Set TXDLEN[7:0] to control the TX length in bytes.
5. Re-transmitting TX packet with the same data will auto-reset TXFF_RPTR to 0.



Simple FIFO Mode

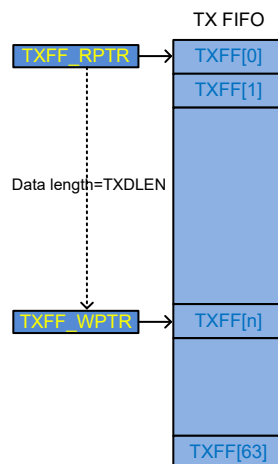
This FIFO mode is used in general applications. The data length should not exceed 64 bytes. To use the simple FIFO mode, the host MCU must write the transmitting data to FIFO by the SPI TX FIFO write command. The transmission order is: the first written byte is sent first, and within each byte, the MSB is sent first. Users should determine all transmitting data packet format including the preamble, SYNCWORD and packet encoding such as FEC, CRC, whitening. After the FIFO data filling is completed, set TXDLEN[7:0] to the desired transmitting length in bytes. Then issue the TX command to start the transmission. After the current transmitting is completed, the data will be kept in FIFO to wait for the next transmission.

Programming procedure:

This procedure is for general applications where the TX data length ≤ 64 bytes.

1. Reset TX FIFO address pointer by the SPI reset TX FIFO command.
2. TXFFSA[5:0] must be cleared to 0.
3. Fill out TX FIFO by the SPI TX FIFO write command.
4. Set TXDLEN[7:0] to control the TX length in bytes.

5. Issue the TX command to start transmission.
6. Check TX complete IRQ to confirm transmission completion.

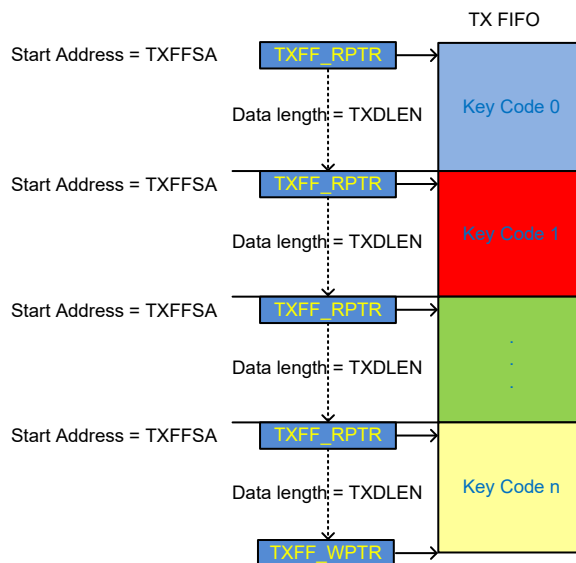


Block FIFO Mode

The Block FIFO mode is used to support multi-key code applications. Users should write all the key codes to FIFO first. When a key is pressed, the host MCU detects it and will set TXFFSA[5:0] to the target key code start address and set TXDLEN[7:0] to indicate the key code length and issue the TX command to start the transmission. The maximum FIFO length is limited to 64 bytes.

Programming procedure:

1. Write key codes for all keys (0~n) to the TX FIFO by the SPI TX FIFO write command.
2. When a key is pressed, the host MCU will set TXFFSA[5:0] to the FIFO start address of the corresponding key code.
3. Set TXDLEN[7:0] for key code length.
4. Issue the TX command to start transmission.
5. Check the TX complete IRQ to confirm transmission completion.



Extend FIFO Mode

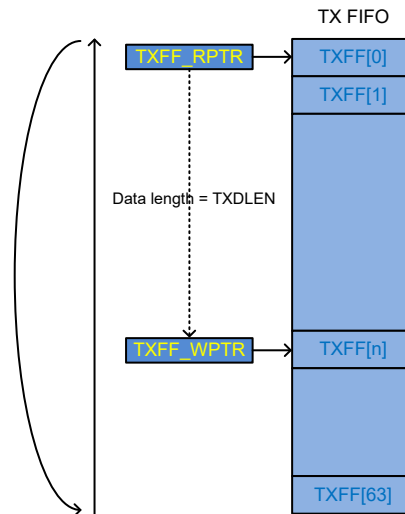
The Extend FIFO mode is used for transmissions with a long payload data packet. The maximum length is 255 bytes. As the physical FIFO length is 64 bytes, to extend the available transmitting length in one packet, a handshake mechanism is needed between the host MCU and the FIFO controller.

Set FFMG[1:0] to determine the FIFO data length margin and set FFMG_EN to enable the margin detection function to inform the MCU when the TX FIFO data fullness level is less than the margin and the remaining data to be transmitted exceeds this margin. The MCU should write data to TX FIFO fast enough when receiving this reminder signal to avoid transmission being terminated by TX FIFO data length dropping to zero.

Programming procedure:

The Extend FIFO mode supports FIFO length exceeding physical FIFO length of 64 bytes and is limited to 255 bytes.

1. Set FFMG_EN to enable the FIFO depth low threshold detection function and set FFMG[1:0] to select the threshold to 4, 8, 16 or 32 bytes.
2. Set the FIFOLTIE bit to 1 to enable the FIFO low threshold IRQ.
3. Set GIONs field (n=1~3) = 0x5 to output IRQ signal on a GIO pin.
4. The MCU detects the IRQ signal. If an active IRQ signal is detected, the MCU will move data into TX FIFO with a data length not exceeding (64 minus the threshold value). Then the MCU clears the FIFO low threshold IRQ flag FIFOLTIF and repeats the same routine until all TX data are completely written to TX FIFO.



Infinite FIFO Mode

Programming procedure:

1. Set FFINF_EN to 1 to enable the Infinite FIFO mode.
2. The handshaking and IRQ function are identical with the Extend FIFO mode.
3. If an active IRQ signal is detected, the MCU continues to write TX data to TX FIFO with a data length not exceeding (64 minus the threshold value). Then the MCU clears the FIFO low threshold IRQ flag and repeats the same routine until it wants to terminate the infinite FIFO mode. To terminate the infinite FIFO mode, after receiving IRQ and moving data to TX FIFO, the

MCU should clear FFINF_EN to zero and set TXDLEN[7:0] to the remaining data length if the remaining transmitting length is less than 192 bytes and longer than 64 bytes. The transmission will be terminated when all of the target data are transmitted completely.

ATX Mode: Auto-Transmit

There is a special ATX operation mode in the BC2113 to reduce the external host's load, which is the WOT (Wake-On-TX) function. It needs to work together with an Idle mode timer (ATXCT timer) that operates at a low frequency. The low frequency clock can be sourced from the internal LIRC or from the external ROSC_i clock by setting the ATXCLKS bit in the ATX1 register. The timeout value of the ATXCT timer is set by the ATXCYC[23:0] bits and can be configured up to 2 hours.

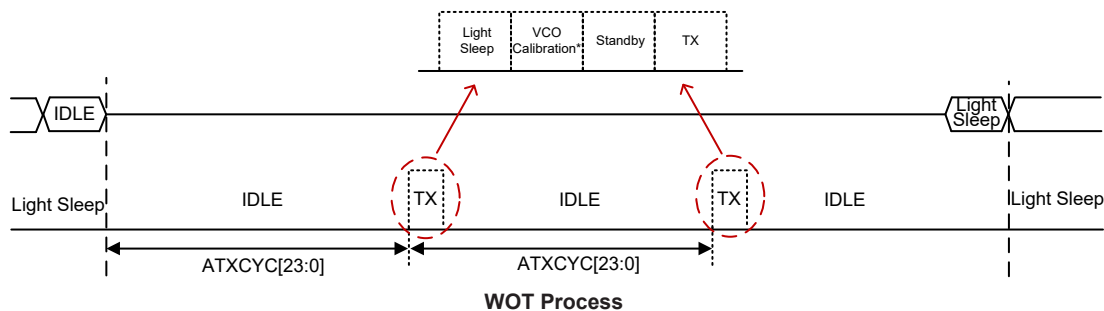
There are two operation modes for the ATXCT timer, selected by the ATXCTM bit. Clearing the ATXCTM bit to 0 will select the single mode, where the ATXCT timer will restart upon every ATX transmission when entering the Idle state. The ATXCT timer will stop and leave the ATX mode upon receiving the Light Sleep command. Setting the ATXCTM bit to 1 will select the continuous mode, where the ATXCT timer will start to operate upon receiving the Idle command and continuously run until either the ATX_EN bit or the ATXCTM bit is cleared to zero.

WOT (Wake-On-TX) Function

When the WOT function is enabled by setting the ATX_EN bit to 1 and the ATXM[1:0] bits to 00b, the BC2113 will periodically wake up from the Idle mode and transmit TX FIFO contents without requiring host MCU intervention. The chip starts the WOT process upon receiving the Idle strobe command from the MCU and stops the WOT process upon receiving the Light Sleep strobe command from the MCU.

The ATXCYC[23:0] bits are used to set the wake-up period for the WOT function. At the moment of timer expiration, the wake-up timer will trigger the BC2113 to leave the Idle state and enter the active state to transmit data. At the same time, the value of ATXCYC[23:0] is reloaded into the timer's counter. After finishing the TX operation, the chip will return to the Idle mode and stay in this state until the next wake-up timer expiration. In the active state, the device performs only one wake-up transmission by default.

Note: 1. VCO Calibration time: ~152μs@433MHz / ~96μs@868MHz
2. All TX processes shown in the figure below must go through the following steps:
Light Sleep→VCO Cal.→Standby



WTM (Wake-up Timer Mode)

The BC2113 can be set as a programmable timer to output a periodical waveform on GION pins. Users can use this signal to wake up the host MCU. After the WTM mode is enabled by setting ATX_EN=1 and ATXM=10b/11b, the BC2113 starts the WTM mode upon receiving the Idle strobe command from the host MCU and stops the WTM mode upon receiving the Light Sleep strobe command. The device will stay in the Idle mode for the whole WTM process.

Auto-Repeat-TX

The BC2113 supports Auto-Repeat-TX function, which is implemented by hardware after the related registers are set. Users need to set the number of repeat transmissions using the TXPRT[7:0] bits. The rest period (time interval) between consecutive packets when repeatedly sending the packet in TX mode can be configured using the TXPRI[7:0] bits, and the output mode during this rest period can also be selected using the TXPRM bit.

OOK Settings

The OOK modulation mode is available in both Direct mode and FIFO mode. The following registers must be set before using it.

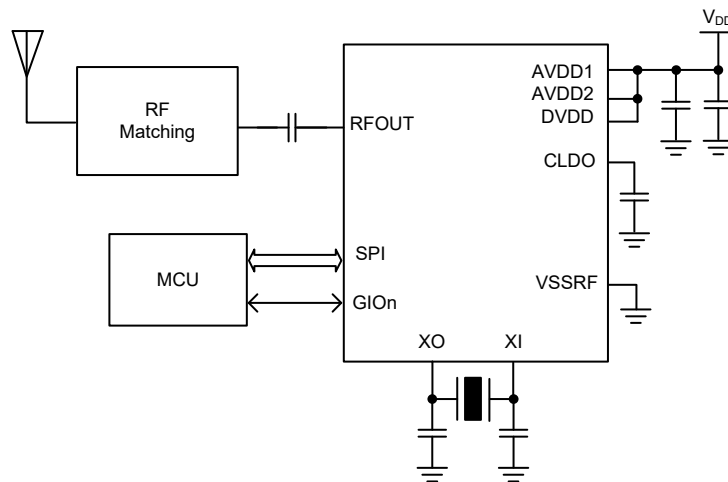
Bank	Address	Name	Value
Common Area	00h	CFG1	80h/90h
Bank 0	3Bh	PKT15	0Dh
Bank 2	33h	TX3	01h

Abbreviation

ACP: Adjacent Channel Power
ATX: Automatic-Transmit
BER: Bit Error Rate
BPF: Band Pass Filter
CFO: Carrier Frequency Offset
CP: Charge Pump
CRC: Cyclic Redundancy Check
DSM: Delta Sigma Modulator
FEC: Forward Error Correction
FIFO: First In First Out
FSK: Frequency Shift Keying
GFSK: Gaussian Frequency Shift Keying
HPF: High Pass Filter
ID: Identifier
IF: Intermedia Frequency
IIR: Infinite Impulse Response
IRQ: Interrupt Request
ISM: Industrial, Scientific and Medical
LNA: Low Noise Amplifier
LO: Local Oscillator
LPF: Low Pass Filter
MCU: Micro Controller Unit
MMD: Multi-Mode Divider
OOK: On-Off Keying
OW: Overwrite

PA: Power Amplifier
 PD: Power Down
 PFD: Phase Frequency Detector (for PLL)
 PLL: Phase Lock Loop
 POR: Power On Reset
 PVT: Process-Voltage-Temperature
 RX: Receiver
 SPI: Serial Peripheral Interface
 SX: Synthesizer
 SYCK: System Clock for digital circuit
 SYNC/SYNCWORD: Synchronization Word
 TBCLK: TX Bit Clock
 TX: Transmitter
 VCO: Voltage Controlled Oscillator
 WOT: Wake-On-TX
 WTM: Wake-up Timer Mode
 XCLK: Crystal Clock
 XO/XOSC: Crystal Oscillator
 XTAL: Crystal

Application Circuits

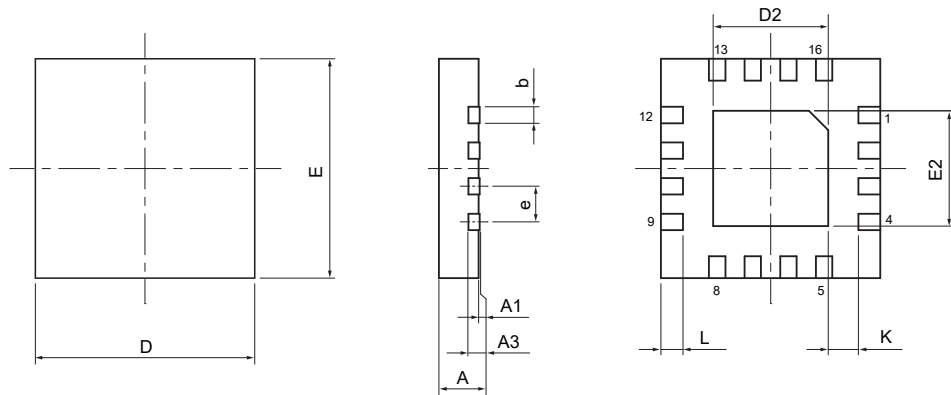


Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the [Holtek website](#) for the latest version of the [Package/Carton Information](#).

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- [Package Information \(include Outline Dimensions, Product Tape and Reel Specifications\)](#)
- [The Operation Instruction of Packing Materials](#)
- [Carton information](#)

SAW Type 16-pin QFN (3mm×3mm×0.75mm, FP0.25mm) Outline Dimensions


Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	0.008 REF		
b	0.007	0.010	0.012
D	0.118 BSC		
E	0.118 BSC		
e	0.020 BSC		
D2	0.063	—	0.071
E2	0.063	—	0.071
L	0.008	—	0.016
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.18	0.25	0.30
D	3.00 BSC		
E	3.00 BSC		
e	0.50 BSC		
D2	1.60	—	1.80
E2	1.60	—	1.80
L	0.20	—	0.40
K	0.20	—	—

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