1-Channel, 600V Half-Bridge N/N Gate-Driver

HT7K6970

Revision: V1.10 Date: September 11, 2026

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Features

- 1-channel half-bridge gate-driver: Drive 1 high-side and 1 low-side N-type MOSFETs or IGBTs
- Integrated High-Side Bootstrap Component: Supports up to 200kHz PWM operation
- Maximum motor sustainable voltage 600V
- Gate Driving Current Capability
  - 350mA Peak Source Current
  - 450mA Peak Sink Current
- Supports both CMOS/TTL Logic with up to 20V sustainable voltage
- Integrated dead time to avoid the power component shoot-through
- Protection features
  - V_{CC} Power Supply Input Under Voltage Lock-Out (VCC_UVLO)
  - Bootstrap Output Under Voltage Lock-Out (VBST_UVLO)
- Package types: 8-pin SOP, 16-pin NSOP
- Operation temperature range: -40°C to 105°C

Applications

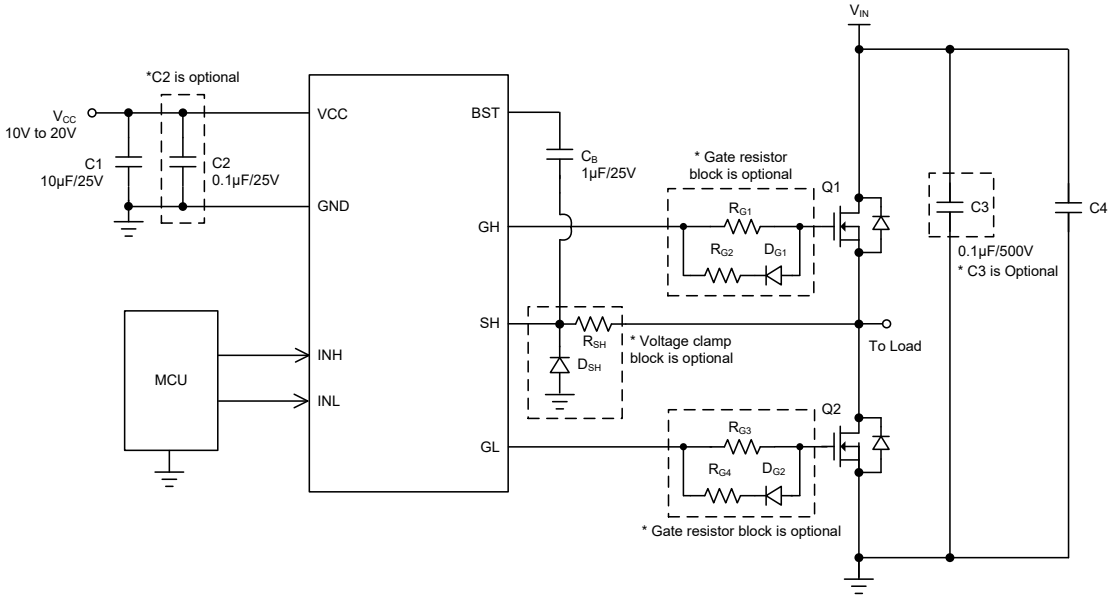
- Motor driving
- DC-AC inverters
- DC-DC converters
- AC-DC power supplies

General Description

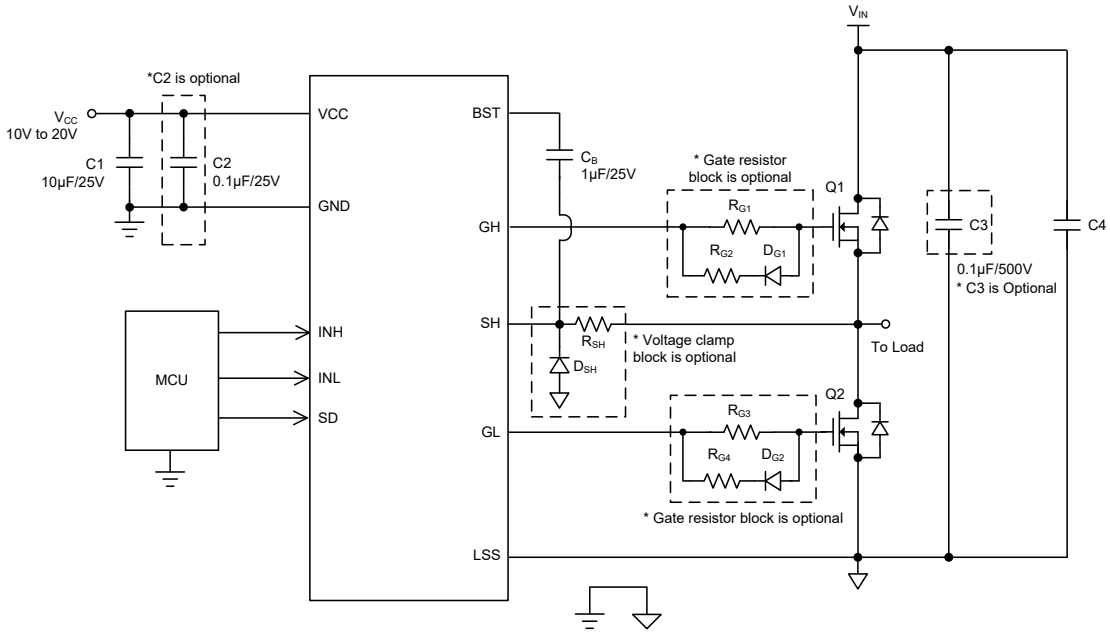
The device is a half-bridge gate-driver for driving power components such as N-type MOSFETs or IGBTs. The high-side gate-driver is suitable for design with a bus voltage up to 600V. The recommended V_{CC} operating voltage is 10V to 20V for power components. The logic inputs are compatible with standard CMOS or TTL down to 3.3V for easy interfacing control units such as microcontrollers or DSP. The device also integrates two internal protection functions: V_{CC} Power Supply Input Under Voltage Lock-Out and Bootstrap Output Under Voltage Lock-Out. The protection functions can prevent the power components from operating in low efficiency or dangerous conditions.

Typical Application Circuit

8-pin SOP Package

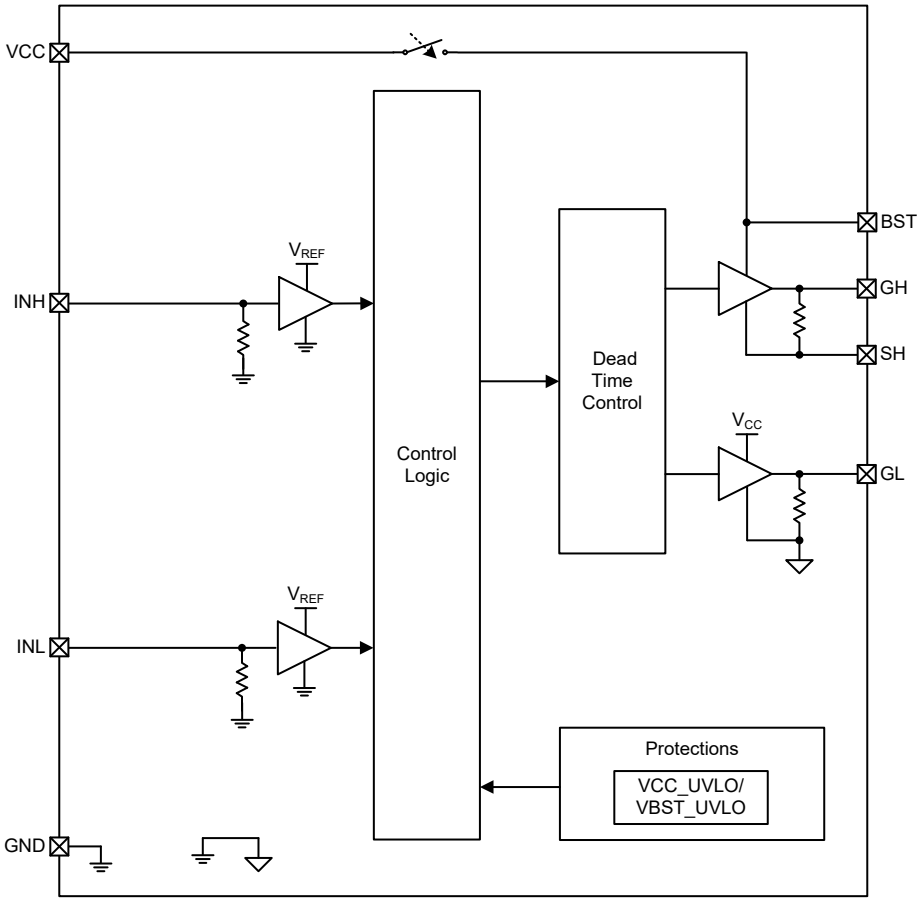


16-pin NSOP Package

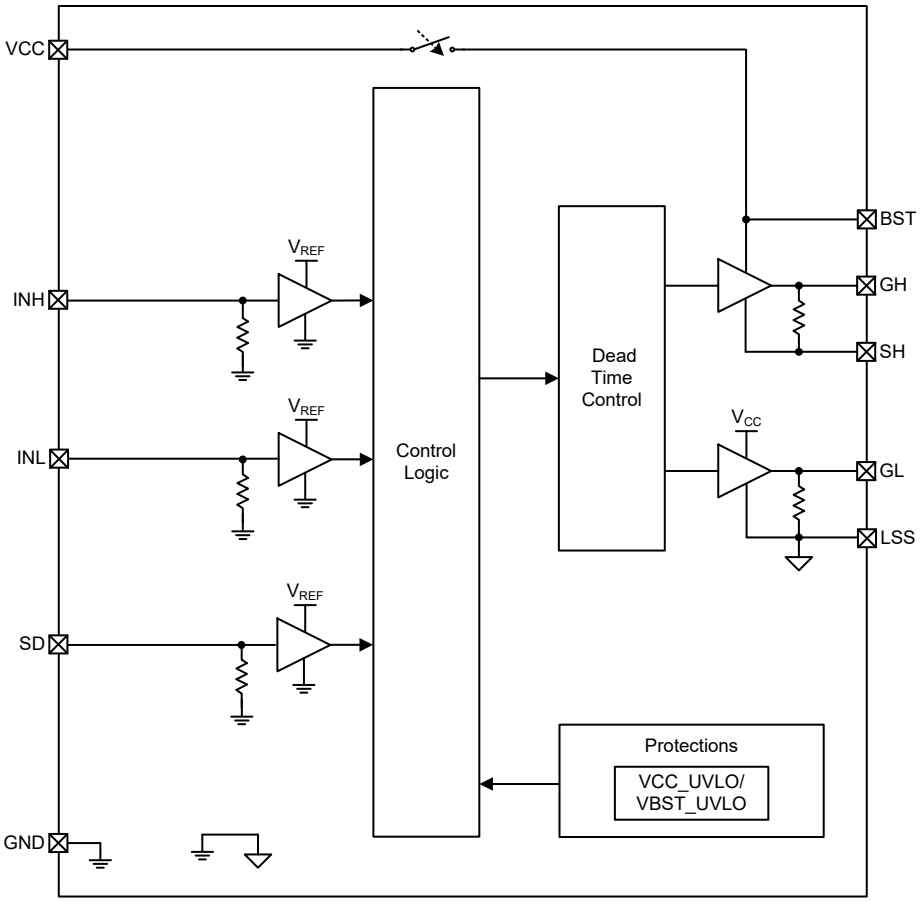


Block Diagram

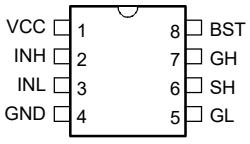
8-pin SOP Package



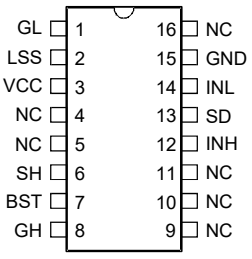
16-pin NSOP Package



Pin Assignment



HT7K6970
8 SOP-A



HT7K6970
16 NSOP-A

Pin Description

Pin No.		Name	Type	Pin Description
8SOP	16NSOP			
5	1	GL	O	Low-side gate drive
	2	LSS	I	Power ground terminal. Connect to ground of power stage
1	3	VCC	P	Power supply
	4	NC	—	No connected
	5	NC	—	No connected
6	6	SH	I	High-side source connection
8	7	BST	O	Bootstrap output
7	8	GH	O	High-side gate drive
	9	NC	—	No connected
	10	NC	—	No connected
	11	NC	—	No connected
2	12	INH	I	Control input for high-side gate drive. High active
	13	SD	I	Control input for shutdown
3	14	INL	I	Control input for low-side gate drive. High active
4	15	GND	G	Signal ground terminal
	16	NC	—	No connected

Legend: I: Input; O: Output; G: Ground; P: Power.

Absolute Maximum Ratings

Parameter			Value	Unit
BST			-0.3 to 600	V
SH			-10 (<150ns) to BST+0.3	V
			-8 to BST+0.3	
GH			SH-0.3 to BST+0.3	V
V_{CC}			-0.3 to 26	V
GL, INH, INL, IN, SD			-0.3 to V_{CC}+0.3	V
Operating Ambient Temperature Range			-40 to 105	°C
Maximum Junction Temperature			150	°C
Storage Temperature Range			-60 to 150	°C
Lead Temperature (Soldering 10sec)			260	°C
ESD Susceptibility	Human Body Model	BST, GH Pins	±1000	V
		Other Pins	±2000	V
	Machine Model		±200	V
Junction-to-Ambient Thermal Resistance, θ_{JA}	8SOP		130	°C/W
	16NSOP		100	°C/W

Recommended Operating Ranges

Parameter	Value	Unit
V_{IN}	5 to 550	V
V_{CC}	10 to 20	V

Note: Absolute Maximum Ratings indicate limitations beyond which damage to the device may occur. Recommended Operating Ranges indicate conditions for which the device is intended to be functional, but do not guarantee specified performance limits.

Electrical Characteristics

V_{CC}=15V, C_{VCC}=10μF, C_B=1μF, T_A=25°C, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Power Supply						
V_{CC}	V_{CC} Supply Voltage	—	10	—	20	V
I_{CC}	V_{CC} Standby Current	VBST_UVLO Protection has been released once (V_{SH}=0V)	—	—	200	μA
Bootstrap						
I_{BST}	Bootstrap Current Consumption	INH='1' and INL='0'. Force $V_{(BST,SH)}$=15V. Measure BST pin current	—	70	—	μA
		INH='1' and INL='0'. Force V_{BST}=615V and V_{SH}=600V. Measure BST pin current	—	75	—	μA
Gate-Driver (GH, SH, GL)						
I_{SO}	High/Low Side Peak Source Gate Current	C_L=200nF	—	350	—	mA
I_{SI}	High/Low Side Peak Sink Gate Current	C_L=200nF	—	450	—	mA
t_{DT}	High/Low Side Dead Time	GL turn-off to GH turn-on (t_{DTLH}) & GH turn-off to GL turn-on (t_{DTHL})	—	350	—	ns
t_{DT_MIS}	Dead Time Mismatch	t_{DT_MIS}=|t_{DTLH}-t_{DTHL}|	—	30	—	ns
t_{PDLH}	Output 'L' to 'H' Propagation Delay Time	INH, INL to GH or GL transition	—	650	—	ns
t_{PDHL}	Output 'H' to 'L' Propagation Delay Time	INH, INL to GH or GL transition	—	650	—	ns
t_{PD_MIS}	High/Low Side Propagation Delay Mismatch	t_{PD_MIS}=|t_{PDLH}-t_{PDHL}|	—	50	—	ns
R_{GL}	GL Pull-down Resistor	GL-to-LSS	—	200	—	kΩ
R_{GH}	GH Pull-down Resistor	GH-to-SH	—	400	—	kΩ
Control Logic						
V_{IH}	Input Logic High Voltage	INH, INL, SD	2.7	—	—	V
V_{IL}	Input Logic Low Voltage	INH, INL, SD	—	—	0.6	V
t_{ON_MIN}	Minimum Input Pulse Width	INH, INL	—	350	—	ns
t_{PDSD}	Shutdown Propagation Delay Time	SD to GH or GL transition	—	650	—	ns
R_{PD}	Input Logic Pull-down Resistor	INH, INL, SD to GND	—	100	—	kΩ
Protections						
V_{CC_UVLO+}	V_{CC} Turn-on Threshold Voltage	V_{CC} rises	—	7.5	—	V
V_{CC_UVLO-}	V_{CC} Turn-off Threshold Voltage	V_{CC} falls	—	7.0	—	V
V_{BST_UVLO+}	$V_{(BST,SH)}$ Turn-on Threshold Voltage	$V_{(BST,SH)}$ rises. INH='1'	—	7.3	—	V
V_{BST_UVLO-}	$V_{(BST,SH)}$ Turn-off Threshold Voltage	$V_{(BST,SH)}$ falls. INH='1'	—	6.5	—	V

Functional Description

Overview

The device is a 1-channel gate-driver, which can be used for external high-side and low-side N-channel MOSFET or IGBT driving. The device includes a 1-channel high-side and low-side gate-driver circuit, and has two protection functions, which are V_{CC} Power Supply Input Under Voltage Lock-Out and Bootstrap Output Under Voltage Lock-Out Protection, to avoid abnormal output situations.

The INH and INL pin input signals of the device are input to the control logic which will determine the high-side and low-side gate-driver outputs. The INH and INL pins each have an internal pull-down resistor. Additionally, there is a fixed dead time insertion when switching between the high-side and low-side gate driving to avoid short-circuit between V_{CC} and ground.

The gate-driver output voltage will vary with the power supply. The gate-driver provides a 350mA peak source current and a 450mA peak sink current when V_{CC} is 15V. Both high-side and low-side gate have an internal hold-off resistor in order to avoid misconduct of external power component due to interference when the power is off.

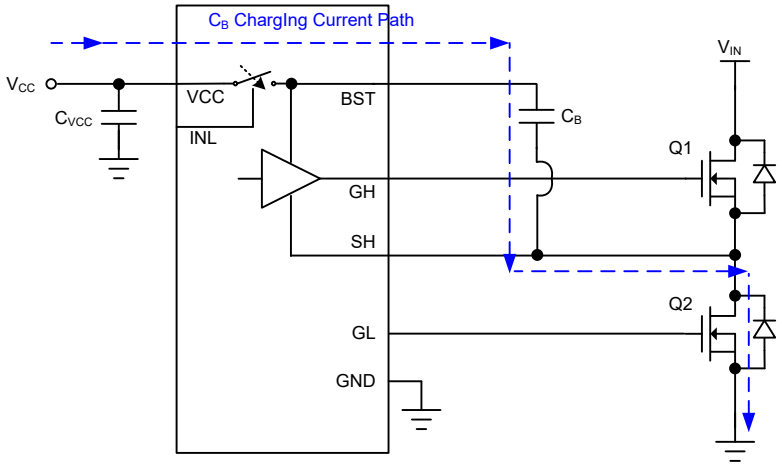
Bootstrap Circuit Operation

The device uses one set of bootstrap circuit as floating power supply to power the high-side gate-driver circuit. The bootstrap circuit is composed of an external bootstrap capacitor, C_B, and an internal bootstrap component. The charging current path of the bootstrap capacitor in common applications is shown in the following first figure. The bootstrap capacitor is charged after the low-side power component is turned on. After the device is enabled, an input command of INH='0' and INL='1' for the device should be arranged before switching to the high-side power component for the first time, so that the low-side power component will be turned on for a period of time to charge the bootstrap capacitor. As shown in the following second figure, the high-side gate-driver output could not be controlled by inputs until the bootstrap capacitor has been charged exceeding the bootstrap under voltage lock-out threshold, V_{BST_UVLO+}. It is recommended to charge the bootstrap capacitor to the steady-state voltage of V1 before proceeding. The equation for estimating the charging time t_{BST} of the bootstrap capacitor is as follows:

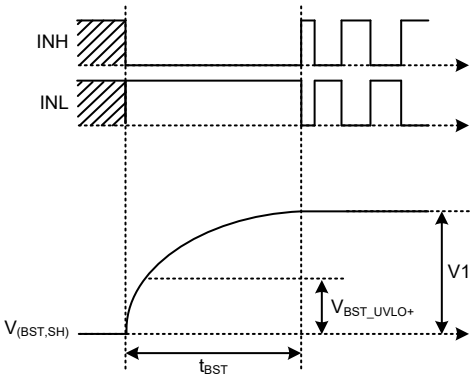
$$t_{BST}\,(ms) > 1.1 \times C_B(\mu F) \div 2.2$$

Where C_B is the bootstrap capacitance. The larger the capacitance, the longer it will take to charge. For example, the charging time t_{BST} should be at least 0.5ms for a capacitance of 1μF. After the charging is completed, the bootstrap voltage will reach the steady-state voltage V1, as shown in the following second figure. The V1 will change along with power supply V_{CC}, and the V1 is calculated as follows:

$$V1 = V_{CC}\text{-}1.5V$$

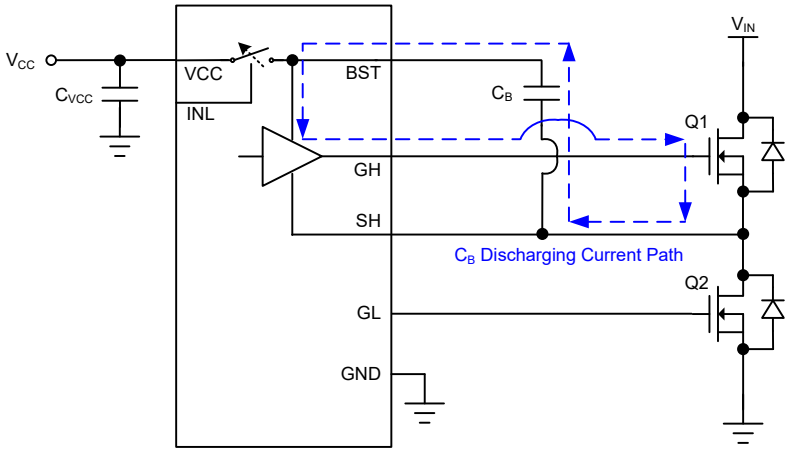


Bootstrap Capacitor (C_B) Charging Current Path



Bootstrap Capacitor Charging Time (t_{BST})

The charge stored in the bootstrap capacitor, C_B, is discharged during the high-side gate-driver output and the internal bootstrap component is used to avoid current backflow, as shown in the following figure. When discharging, pay attention to whether the bootstrap capacitance value is sufficient. If the bootstrap capacitance value is too small, it will affect the high-side gate driving capability. Refer to the "Component Selections" chapter for the bootstrap capacitance recommendation.



Bootstrap Capacitor (C_B) Discharging Current Path

When V_{CC} is greater than or equal to 6V, the bootstrap component is controlled by the INL pin input signal. The on/off true table is shown as follows.

When V_{CC} is less than 6V, during normal V_{CC} power-down operation, if the motor is still spinning, the motor back-EMF may temporarily recharge V_{CC} through internal high-impedance structures. Under this condition, the motor supply voltage, V_{IN}, does not back-feed into V_{CC}. As the motor comes to a complete stop, the back-fed current ceases and V_{CC} naturally discharges to 0V.

V_{CC}	INH	INL	Bootstrap Component
V_{CC}<6V	x	x	ON
V_{CC}≥6V	x	0	OFF
	x	1	ON

Bootstrap Component Control Truth Table

Bootstrap Component Safe Operating Area

After selecting the high-side driver and the bootstrap capacitor, C_B, different application conditions, such as V_{CC} voltage, switching frequency, low-side duty cycle, operating temperature and the forward voltage of the bootstrap component, may cause excessive voltage drop across C_B, thereby triggering the bootstrap output under voltage lock-out, VBST_UVLO.

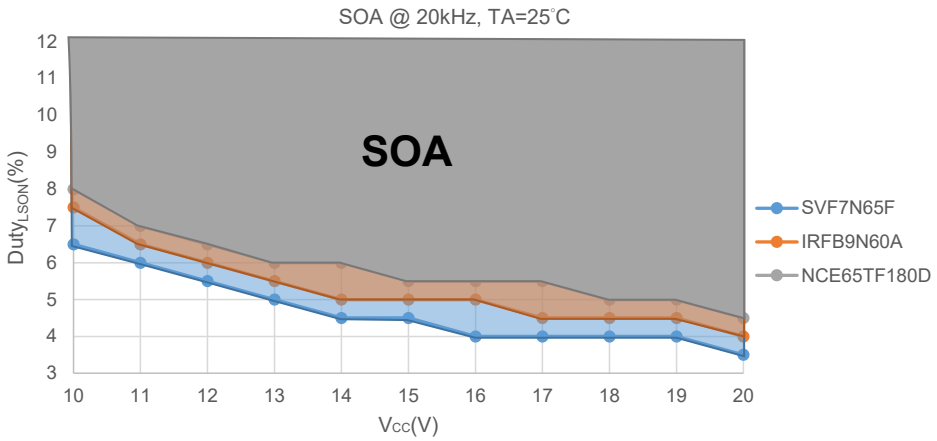
Therefore, it is necessary to evaluate ΔV_{BST}, which represents the maximum allowable voltage drop across the bootstrap capacitor within a switching period. The following equation can be given by the charging current path of the bootstrap capacitor:

$$\Delta V_{BST} \leq V_{CC}\text{-}V_F\text{-}V_{BST\_UVLO}\text{-}V_{DS\_LS}$$

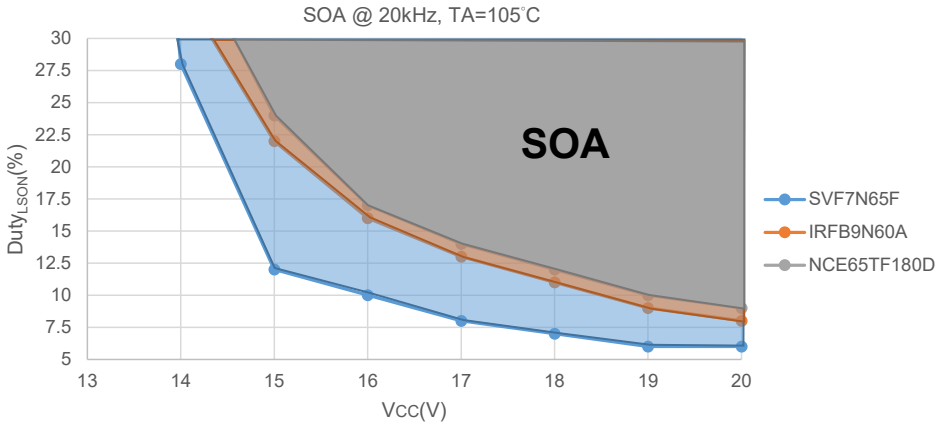
Where:

- ΔV_{BST} is the maximum allowable voltage drop across the bootstrap capacitor.
- V_F is the bootstrap component forward voltage.
- V_{DS_LS} is the drain-source voltage of the low-side MOSFET or IGBT.

To help users quickly verify the Safe Operating Area (SOA) of the bootstrap component, three different MOSFET specifications are provided as reference. As shown in the following figures, the SOA of the HT7K6970 at T_A=25°C & 105°C, C_B=1μF and f_{SW}=20kHz is defined by the maximum allowable voltage drop across the bootstrap capacitor, ΔV_{BST}. When ΔV_{BST} remains within the SOA (colored area), the device operates reliably without functional anomalies. However, if ΔV_{BST} falls outside the SOA (white area), functional anomalies may occur.



Bootstrap Component SOA – T_A=25°C



Bootstrap Component SOA – T_A=105°C

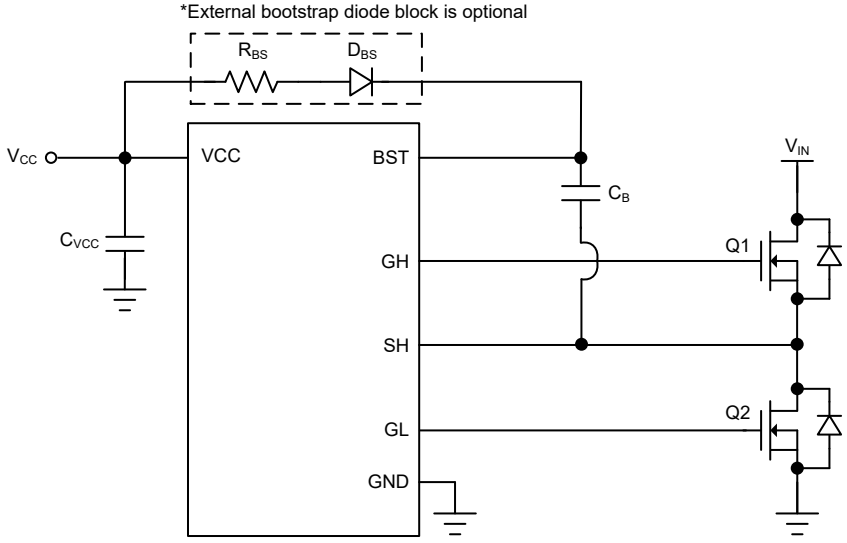
Where:

- f_{SW} is the switching frequency.
- $Duty_{LSON}$ is the low-side on duty cycle.

Part Number	Description	Ciss (pF)
SVF7N65F	650V/7A	918
IRFB9N60A	600V/9.2A	1400
NCE65TF180D	650V/21A	2580

Three MOSFET Specifications

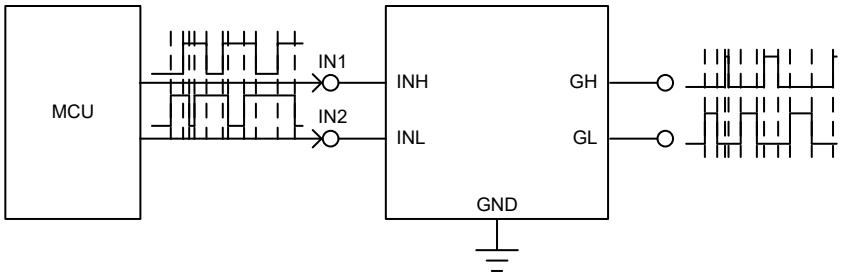
In such cases, it is recommended to add an external diode, D_{BS}, such as the 1N4007, between VCC and BST. When an external diode is used, it is further recommended to add a bootstrap resistor, R_{BS}, with a typical value of 10Ω in series with C_B to limit the bootstrap capacitor charging current, as shown below.



External Bootstrap Diode Circuit

Gate-Driver Control Logic

As a gate-driver for driving high-side and low-side power components, the device control signals are input on the INH and INL pins. Usually a 2-wire input control method as shown in the figure below is used, where the dead time width is determined by the control signals but has a minimum value equal to the fixed dead time designed in the device.



2-Wire Control

Both high-side and low-side gate-driver outputs are controlled by the INH, INL and SD pin input signals, the on/off true table is shown as follows.

INH	INL	GH-to-SH	GL-to-GND	External H/S Power Component	External L/S Power Component
0	0	L	L	OFF	OFF
0	1	L	H	OFF	ON
1	1	L	L	OFF	OFF
1	0	H	L	ON	OFF

Note: H/S indicates High-Side, L/S indicates Low-Side.

Operation Truth Table – 8SOP

SD	INH	INL	GH-to-SH	GL-to-LSS	External H/S Power Component	External L/S Power Component
1	x	x	L	L	OFF	OFF
0	0	0	L	L	OFF	OFF
0	0	1	L	H	OFF	ON
0	1	1	L	L	OFF	OFF
0	1	0	H	L	ON	OFF

Note: H/S indicates High-Side, L/S indicates Low-Side.

Operation Truth Table – 16NSOP

Protection Function Operation

When the device operates in an abnormal situation, such as when a V_{CC} Power Supply Input Under Voltage Lock-Out or Bootstrap Output Under Voltage Lock-Out has occurred, it will activate the corresponding protection mechanism to turn off the affected power component. The protection mechanisms are summarized below.

Protection	Protection Entry Condition	Protection Reaction			Release Condition
		GH-to-SH	GL-to-GND	Bootstrap Function	
VCC_UVLO	$V_{CC}<V_{CC\_UVLO-}$	L	L	Disable	$V_{CC}\geq V_{CC\_UVLO+}$
VBST_UVLO	$V_{(BST,SH)}<V_{BST\_UVLO-}$	L	—	Keep Active	$V_{(BST,SH)}\geq V_{BST\_UVLO+}$

Protection Function Conditions

V_{CC} Power Supply Input Under Voltage Lock-Out – VCC_UVLO

This integrated protection function is designed to avoid unstable gate-driver output when the power supply voltage falls to a certain low level. During the power-on period, both high-side and low-side power components are turned off before the power supply voltage reaching the threshold V_{CC_UVLO+}. When the power supply voltage is greater than V_{CC_UVLO+}, the gate-driver outputs are determined by the input signals. If the power supply voltage falls below the under voltage lock-out threshold V_{CC_UVLO-}, both high-side and low-side power components will remain off.

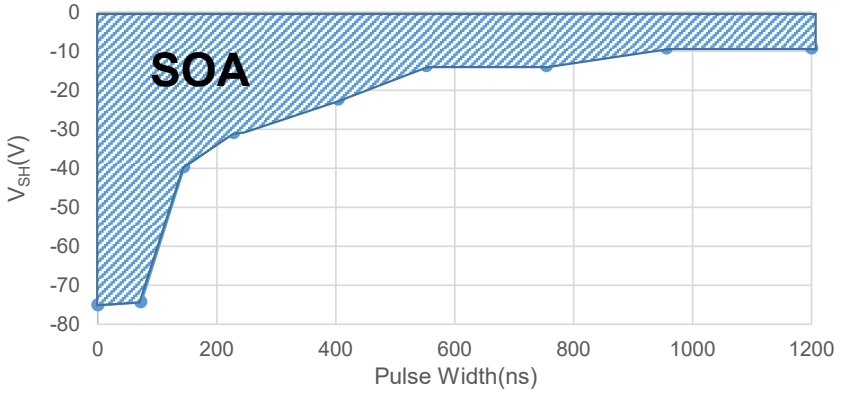
Bootstrap Output Under Voltage Lock-Out – VBST_UVLO

This integrated protection function is designed to avoid that when the bootstrap capacitor is insufficiently charged, the output voltage of the high-side gate-driver will be insufficient making the high-side power component fully turned on. When the bootstrap output voltage is larger than the threshold V_{BST_UVLO+}, the high-side gate-driver output is determined by the input signals. If the bootstrap output voltage falls below the under voltage lock-out threshold V_{BST_UVLO-}, the high-side power component will remain off.

Negative Transient Voltage Tolerance of SH Pin

In a typical motor drive system, the dv/dt is usually designed within the range of 3V~5V/ns. However, during abnormal events such as a short circuit or the load current momentarily, the resulting di/dt can be much higher than during normal operation, causing the negative V_{SH} transient voltage to exceed this range.

As shown in the following figure, the Safe Operating Area (SOA) of the HT7K6970 at V_{CC}=15V is defined based on repetitive negative V_{SH} transients. If a negative transient voltage falls within the SOA (blue area), the device operates reliably without functional anomalies or permanent damage. Conversely, if the transient voltage falls outside the SOA (white area), it may result in permanent damage to the device. Refer to the “Component Selections” chapter for voltage clamp circuit to suppress negative transient voltage of SH pin.



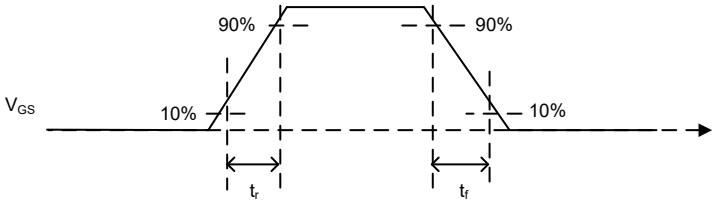
Negative Transient Voltage Tolerance SOA of SH Pin

Component Selections

Gate Resistor Circuit

The main function of the gate resistors, R_{G1}, R_{G2}, R_{G3} and R_{G4}, is to reduce the vibration of output voltages and reduce the EMI noise generation. Adjusting R_{G1} and R_{G3} controls the on time of the high-side and low-side switches, adjusting R_{G2} and R_{G4} controls the off time of the high-side and low-side switches. The gate resistors are optional and can be used according to the requirements.

It is recommended to select the gate resistance value according to the desired gate voltage rising time (t_r) or falling time (t_f), which are shown in the following figure. R_{G1}, R_{G2}, R_{G3} and R_{G4}, if used, are recommended to have a typical value of 10Ω~200Ω. It is recommended to use a 1N4148 switch diode for both D_{G1} and D_{G2}.



Gate Voltage (V_{GS}) Rising Time (t_r) and Falling Time (t_f)

Bootstrap Capacitor

The power stored in the bootstrap capacitor, C_B, services as a floating power supply for the high-side gate-driver circuit. For reliable operation, C_B must be low ESR, placed close to the device and sized according to the switching frequency and high-side driver requirements.

The minimum size of the bootstrap capacitor is given by:

$$C_B \geq \frac{Q_{GT}}{\Delta V_{BST}} = \frac{Q_g + (I_{BST} + I_{LK\_CAP} + I_{LK\_MOS}) \times t_{HSON}}{V_{CC} - V_F - V_{BST\_UVLO-} - V_{DS\_LS}}$$

Where:

- Q_{GT} is the total gate charge of the MOSFET or IGBT.
- ΔV_{BST} is the maximum allowable voltage drop across the bootstrap capacitor.
- Q_g is the MOSFET or IGBT turning on required gate charge.
- I_{BST} is the bootstrap current consumption.
- I_{LK_CAP} is the bootstrap capacitor leakage current.
- I_{LK_MOS} is the MOSFET or IGBT gate-source leakage current.
- t_{HSON} is the high-side on time.
- V_F is the bootstrap component forward voltage.
- V_{DS_LS} is the drain-source voltage of the low-side MOSFET or IGBT.

Generally speaking, the bootstrap capacitance value is recommended to be more than 50 times the input power capacitance value of the high-side power switch, and is recommended to be at least 1μF.

Gate-Driver Supply Capacitor

The power supply regulator capacitor, C1, can reduce input voltage fluctuation. It is recommended to use at least a 10μF capacitor.

Power Supply Bypass Capacitors

When the board power supply is mains, the power supply bypass capacitors, C2 and C3, can filter out the high-frequency noise input from the power supply. It is recommended to use a 0.1μF capacitor. These capacitors are optional and can be used according to the requirements.

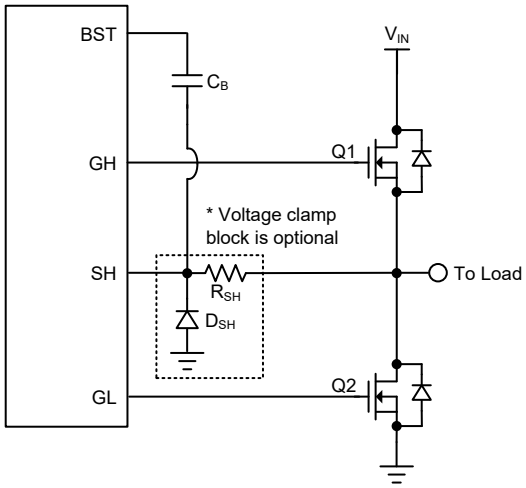
Input Supply Capacitor

The input power supply capacitor, C4, can absorb the current that is fed back to the power supply and can also provide a transient power to compensate for the power response speed or the influence of external wire length.

Voltage Clamp Circuit to Suppress Negative Transient Voltage of SH Pin

When the negative transient voltage falls outside the SOA (white area) in the negative transient voltage tolerance SOA of SH pin, a voltage clamp circuit can be used to suppress the negative V_{SH} transient voltage, as shown in the following figure.

To ensure reliable protection against device damage or malfunction, it is recommended to use an R_{SH} resistor with a typical value of 2.2Ω, and a D_{SH} diode such as the FR107 fast recovery diode.



Voltage Clamp Circuit of SH Pin

Layout Consideration Guide

To reduce the influence caused by parasitic components on the board, there are some important points to note on the PCB layout.

1. The power supply bypass capacitor C2 must be placed close to the VCC pin and closer to VCC than C1.
2. The power supply regulator capacitor C1 must be placed close to the VCC pin.
3. The input power supply capacitor C4 and power supply bypass capacitor C3 must be placed close to the high-side power component Q1.
4. The bootstrap capacitor C_B must be placed close to the BST and SH pins.
5. The power components Q1 and Q2 must be close to the GH and GL pins.
6. The source electrode of the high-side power component Q1 should be close to the drain electrode of the low-side power component Q2.
7. The gate-driver control circuits R_{G1}, R_{G2} and D_{G1}, R_{G3}, R_{G4} and D_{G2}, should be close to the high-side power component Q1 and low-side switches Q2 respectively.
8. The copper foil from the board positive power supply through Q1 and Q2 to the negative power supply should be widened.
9. It is recommended that C1, C2, C3, C4 and the gate-driver GND pin ground terminal are laid copper together. Finally connect the copper to the negative power supply node of the board.

Thermal Consideration

The maximum power dissipation depends upon the thermal resistance of the device package, PCB layout, rate of surrounding airflow and difference between the junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)}=(T_{J(MAX)}-T_A)/\theta_{JA} \quad (W)$$

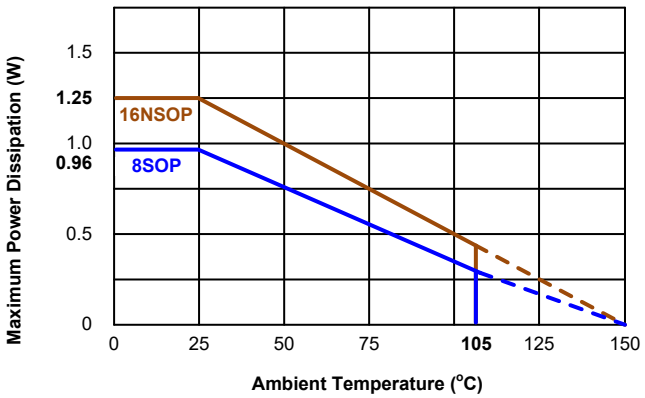
Where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature and θ_{JA} is the junction-to-ambient thermal resistance of device package.

For maximum operating rating conditions, the maximum junction temperature is 150˚C. However, it is recommended that the maximum junction temperature does not exceed 125˚C during normal operation to maintain high reliability. The de-rating curve of the maximum power dissipation is show below:

$P_{D(MAX)}=(150˚C-25˚C)/(130˚C/W)=0.96W$ (8SOP)

$P_{D(MAX)}=(150˚C-25˚C)/(100˚C/W)=1.25W$ (16NSOP)

For a fixed $T_{J(MAX)}$ of 150˚C, the maximum power dissipation depends upon the operating ambient temperature and the package's thermal resistance, θ_{JA}. The de-rating curve below shows the effect of rising ambient temperature on the maximum recommended power dissipation.



In addition to the package thermal dissipation, the total power dissipation of the device, P_D, is calculated as follows:

$$P_D=P_{D1}+P_{D2}$$

Where P_{D1} indicates the power dissipation of the bootstrap circuit and P_{D2} indicates the power dissipation of the low-side gate driving loss, which are calculated as follows:

$$P_{D1}=(V_{CC}-V_{BST})\times V_{BST}\times C_{iss}\times f_{SW}$$

$$P_{D2}=V_{GL}\times V_{GL}\times C_{iss}\times f_{SW}$$

Where V_{CC} is the power supply, V_{BST} is the bootstrap voltage, V_{GL} is the voltage of the GL pin; f_{SW} is the switching frequency; C_{iss} is power component input power capacitance.

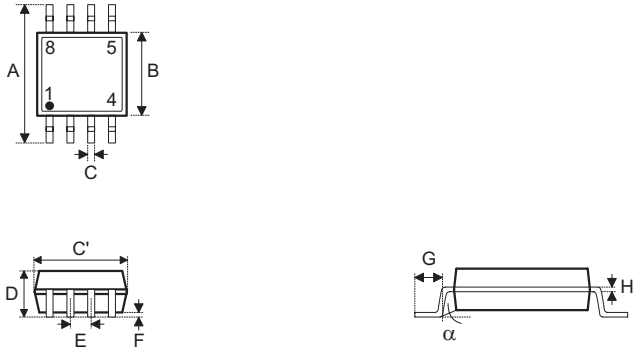
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

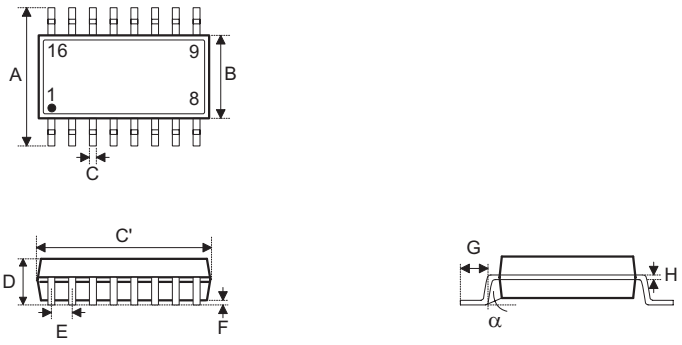
8-pin SOP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.236 BSC	
B		0.154 BSC	
C	0.012	—	0.020
C′		0.193 BSC	
D	—	—	0.069
E		0.050 BSC	
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		6.00 BSC	
B		3.90 BSC	
C	0.31	—	0.51
C′		4.90 BSC	
D	—	—	1.75
E		1.27 BSC	
F	0.10	—	0.25
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°

16-pin NSOP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.236 BSC	
B		0.154 BSC	
C	0.012	—	0.020
C’		0.390 BSC	
D	—	—	0.069
E		0.050 BSC	
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		6.00 BSC	
B		3.90 BSC	
C	0.31	—	0.51
C’		9.90 BSC	
D	—	—	1.75
E		1.27 BSC	
F	0.10	—	0.25
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°